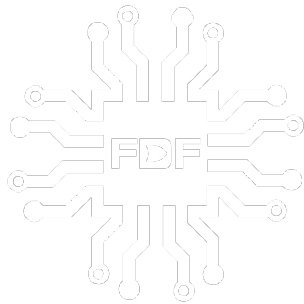


Session Program

27-29 May 2026



FPGA
DEVELOPERS'
FORUM

3rd FPGA Developers' Forum (FDF) meeting

***Solutions to everyday digital design
problems***

CERN, 500/1-001 - Main Auditorium

Friday 29 May

09:00

Solutions to everyday digital design problems: 1

Session | **Location:** CERN, 500/1-001 - Main Auditorium | **Convener:** Dr Paschalis Vichoudis

09:00–09:25

The CERN Open Hardware Licence for FPGA Designs

Speaker

Javier Serrano

09:25–09:45

Kyokko2: a portable multi-gigabit serial communication controller

Speaker

Sou Tanaka

09:45–10:10

A Multigigabit Link Layer Protocol for Single Picosecond Latency Determinism Using AMD Ultrascale+ GTH and GTY Transceivers

Speaker

Paul Bachek

10:10

10:40

Solutions to everyday digital design problems: 2

Session | **Location:** CERN, 500/1-001 - Main Auditorium | **Convener:** Evangelia Gousiou

10:40–11:05

Latency analysis of the CPU-FPGA interface in the Zynq UltraScale+ SoC

Speaker

Valerio Nappi

11:05–11:30

Recovered Clock Phase Monitoring on AMD Transceivers for Deterministic Timing

Speaker

Nikitas Loukas

11:30–11:50

SystemVerilog Hacks: Circumventing the Limitations of SystemVerilog

Speaker

Yair Linn

11:50–12:15

CDCs, FIFOs, and Width Converters: How to Combine Open Logic Building Blocks Correctly

Speaker

Oliver Bründler

12:20