Session Program

27–29 May 2026

3rd FPGA Developers' Forum (FDF) meeting

Poster Session and Welcome Reception

CERN, 500/1-001 - Main Auditorium

Wednesday 27 May

19:00

Poster Session and Welcome Reception: Posters are on display throughout the workshop. During the poster session, participants are free to browse at their own pace (no dedicated timeslot per poster; listed in Indico for reference only).

Session | **Location:** CERN, 500/1-001 - Main Auditorium

19:00–19:01 **RoCE-Stream -- offloading (debug) data over 100Gbit RoCE RDMA**

Speaker
Alexander Daum

19:01–19:02

CI-Driven FPGA ML Experimentation: Unified Results from HLS, Implementation, and On-Hardware Testing

Speaker
Georgios Flengas

19:02–19:03

XiBIF: A Python tool and hardware platform for streamlined FPGA development

Speakers
Mr Janik Witzig, Lukas Leuenberger

19:03–19:04

Progressive Arithmetic Optimizations : Tensor and DSP Kernels to Synthesizable Datapaths

Speaker
Louis Ledoux

19:04–19:05 **Emulation of classic CPUs - a SoC-centric hybrid approach**

Speaker
Volker Urban

19:05–19:06

Benchmarking Neural Network Inference on Versal ACAP AI Engines for Real-Time Detector Alignment

Speaker
Haider Abidi

19:06–19:07

Leveraging HBM for accelerating arbitrary Quantum Simulation on AMD Alveo platforms

Speaker
Marwin Kirchhofs

19:07–19:08

Towards a predictable toolchain dedicated to the generation of FPGA circuits for control algorithms

Speaker
Inès Winandy

19:08–19:09 **Qualifying FPGAs for Radiation-Tolerant Applications**

Speaker
Patrick Urban

19:09–19:10 **An Hardware Emulator for the ATLAS Phase-II L0MDT Trigger System**

Speaker
Marcel Marques Boonen

19:10–19:11
Deep Memory for the Data Acquisition of the IceCube-Gen2 Surface Array

Speaker
Frederik Schmitt

19:11–19:12
Practical Implementation of Lightweight Cryptography on FPGAs: Design Trade-offs, Side-Channel Considerations, and Integration Lessons

Speaker
Pradeep Kumar Mohanty

19:12–19:13
POEMMA Balloon with Radio experiment as a use case for RFSoC in Astroparticle Physics

Speaker
Alexander Novikov

19:13–19:14
Transitioning to Modern FPGA Architectures in a High-Throughput Research Facility

Speaker
Mr Bruno Fernandes

19:14–19:15
Geant4-driven realistic waveform generation for FPGA algorithm verification in radiation detector readout

Speaker
Ms Handan YILMAZ

19:15–19:16
Resource-Efficient Streaming Beam Reconstruction on an Intel Max 10 FPGA

Speaker
Liqing Qin

19:16–19:17
JEDI-linear: Fast and Efficient Graph Neural Networks for Jet Tagging on FPGAs

Speaker
Zhiqiang Que

19:17–19:18
Reconciling Fixed-Frequency Clocking and Variable Sampling-Rate Data: Real-Time Arbitrary Resampling for Stream Processing

Speaker
Javier Galindo Guarch

19:18–19:19
Low-Complexity Median Algorithm in FPGA for AMS-02 Layer-0 Upgrade

Speaker
Luca Russo

19:19–19:20
AI Inference in FPGAs for both Standard and Safe & Dependable Applications

Speaker
David Ganz

19:20–19:21 **SVN is better than GIT for FPGA development: I will die on this hill**

Speaker
Yair Linn

19:21–19:22 **Using native libraries functions from VHDL with VHPIDIRECT**

Speaker
Augusto Fraga Giachero

19:22–19:23
MONO: Enhancing Bit-Flip Resilience With Bit Homogeneity for Neural Networks

Speaker
Maryam Eslami

19:23–19:24 **PandA-Bambu Backend for hls4ml**

Speaker
Nicolo Ghielmetti

19:24–19:25
From C/C++ to Hardware with Bambu: An Open-Source HLS Research Tool

Speaker
Mr Tommaso Fellegara

19:25–19:26 **ARTEMIS: FPGA-based AD in the ATLAS Level-1 Trigger**

Speaker
Paula Martinez Suarez

19:26–19:27
Implementation of Elias deterministic extractor for true random number generation

Speaker
Lorenzo Borella

19:27–19:28 **The Firmware Development Kit (FDK)**

Speaker
Adam Lee Barcock

19:28–19:29
Frame Buffering Design Strategies for Boosting Mobipix 15D X-Ray Imaging Rates

Speaker
Mr Allan Borgato

20:00