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RadTol RISC-V forum

Tuesday, 23 September 2025 11:00 (2 hours)

This forum will focus on methodologies and challenges in developing radiation-tolerant RISC-V SoCs. Each topic will be discussed for 30-45 minutes, based on questionnaires and optional slides submitted in advance. Topic conveners will prepare short introductions to frame the discussion.

Agenda:

SoC Design –architecture choice, use of generators, and toolchain aspects.

Radiation Tolerance Techniques –approaches for core, memory, and interconnect robustness.

Verification –core-level and environment verification, fault tolerance validation, and emulation (e.g., FPGA).

The aim is to identify promising techniques, share best practices, and guide collaborative progress on rad-hard RISC-V solutions.

Presenters: JENIHHIN, Maksim (Tallinn University of Technology (EE)); JENIHHIN, Maksim; ANDORNO, Marco (CERN); KARAGOUNIS, Michael (Fachhochschule Dortmund Univ. of Applied Sciences and Arts (DE))

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