Oxford contributions to CTF3-002

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Work programme

- **Design drive-beam phase FF system for CLIC**

CLIC Drive Beam Requirements

Schulte

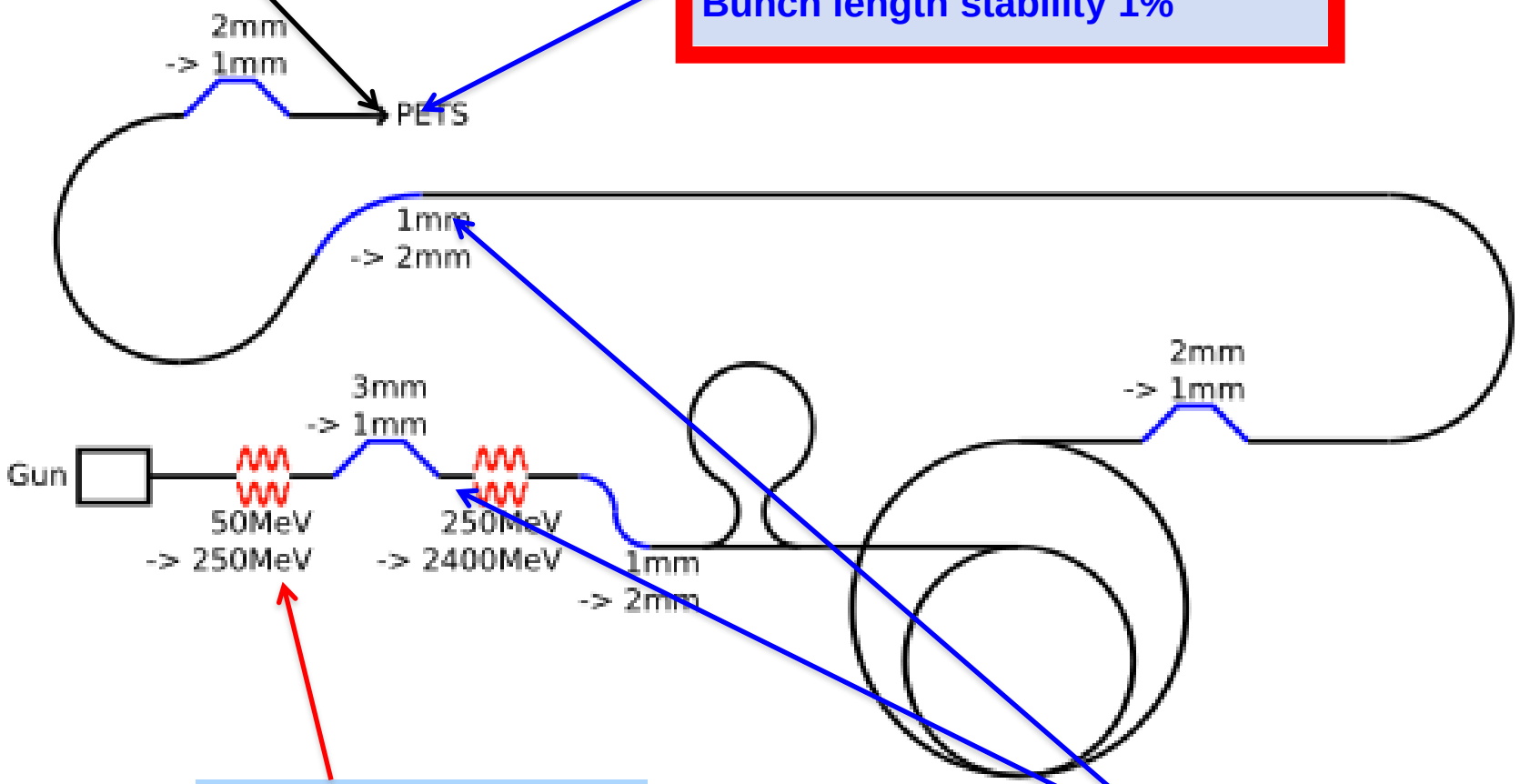
Emittance $\varepsilon_{x,y} \leq 150\mu m$

Transverse jitter $\leq 0.3\sigma$

Current stability $0.75 \cdot 10^{-3}$

Phase stability 0.2° @ 12GHz

Bunch length stability 1%



RF power stability 0.2%

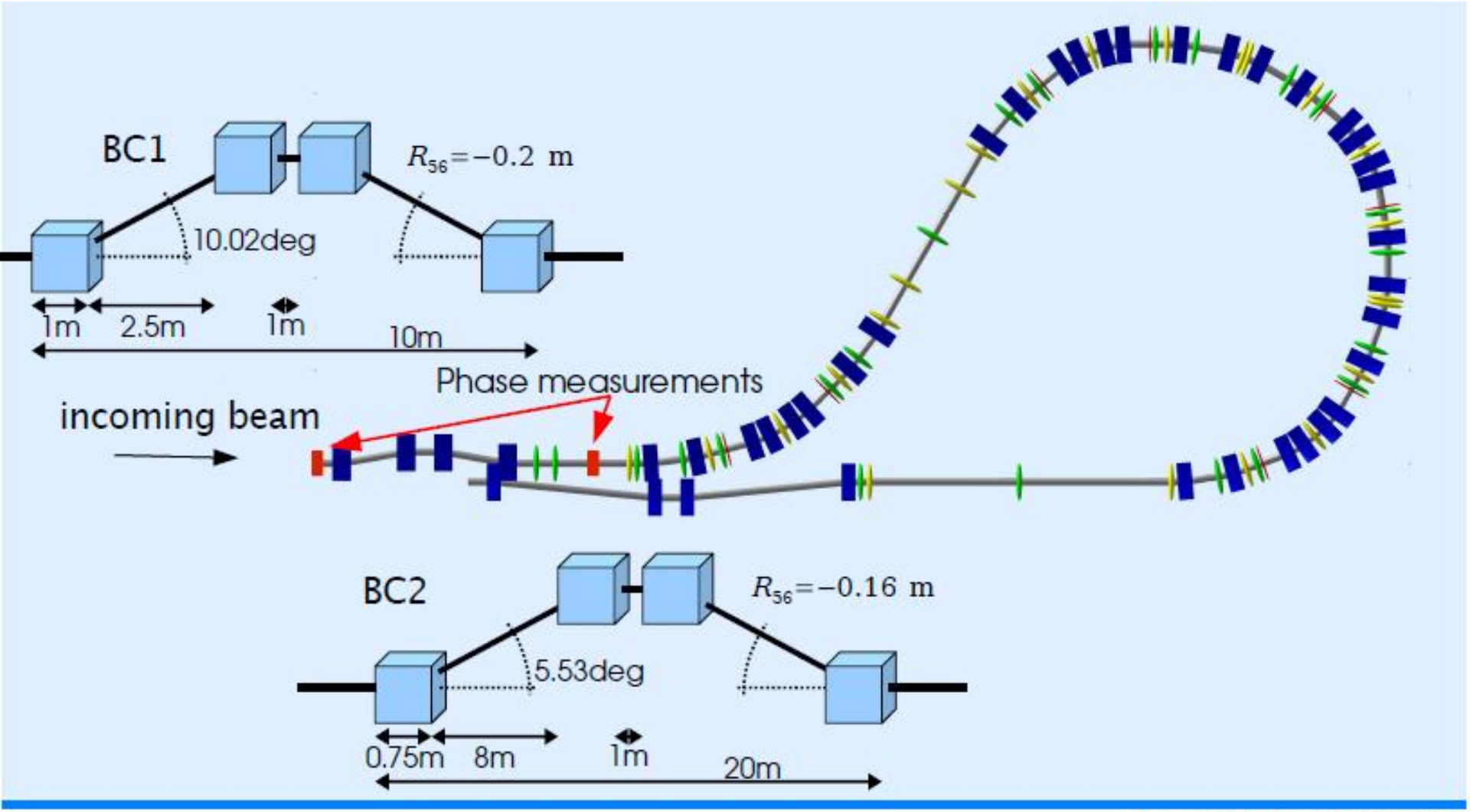
RF phase stability 0.05°

Current stability 0.1%

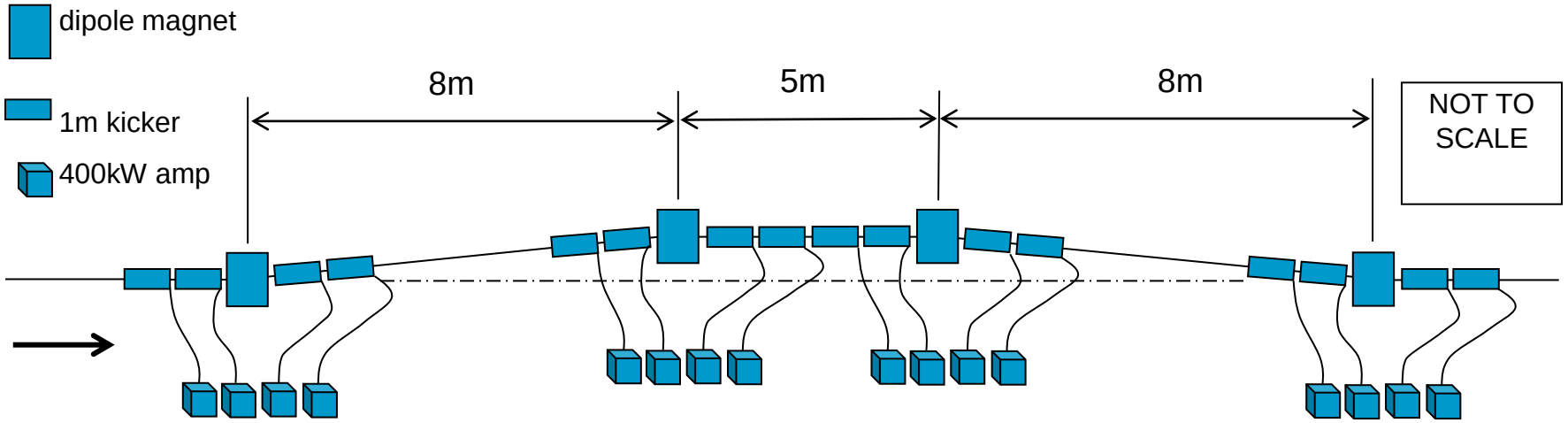
Phase stability 2.5° @ 12GHz

0.2° @ 1GHz

Phase feed-forward concept



A Preliminary System Concept



- **+- 375 urad kick at each bend**
- **0.5% energy spread, 1m dispersion -> 5mm rms**
- **beam pipe diameter >> 50mm**
- **4 kickers at each bend**
- **> 400kW peak power amplifier to each kicker**

A rough estimate

16 amplifiers & kickers / drive beam

→ 768 amplifiers total

→ 300MW total peak power

assume*:* £100K per 400kW amplifier

→ £75M for the whole system

This is all very very approximate

- **it makes no allowance for technological progress**
- **lot of details to be worked out**
- **very dependent on high-volume costs: no sound basis for these**
- **depends on system design: kick dynamic range**

Work programme

- **Design drive-beam phase FF system for CLIC**
- **Investigating amplifier component technologies:**

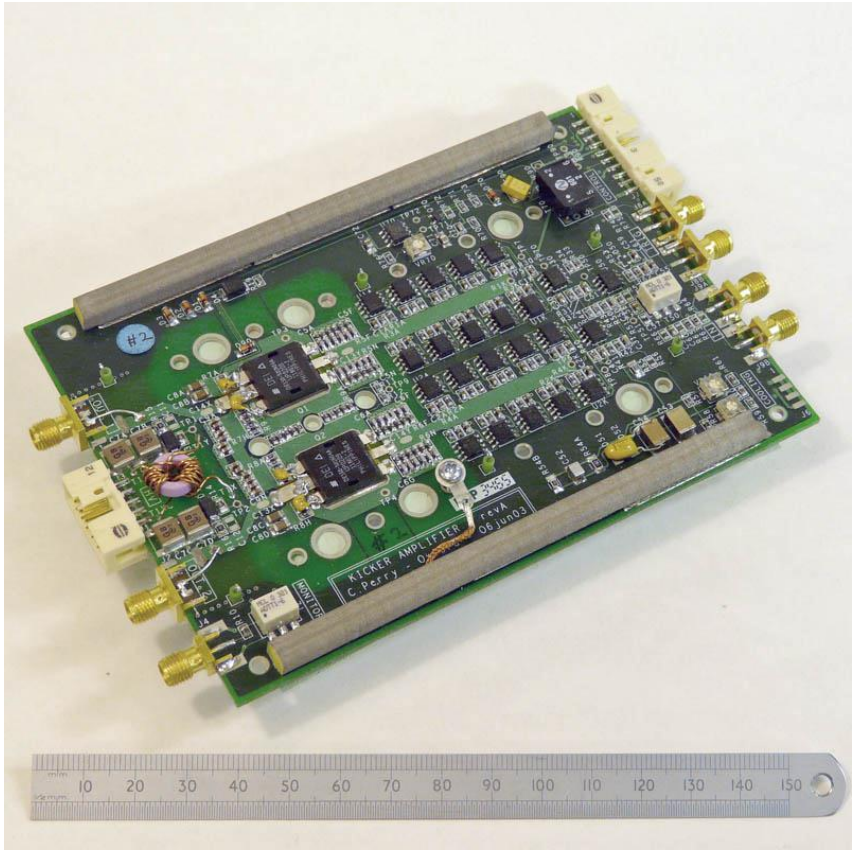
  HV silicon MOSFETs

  Silicon LDMOS FETs

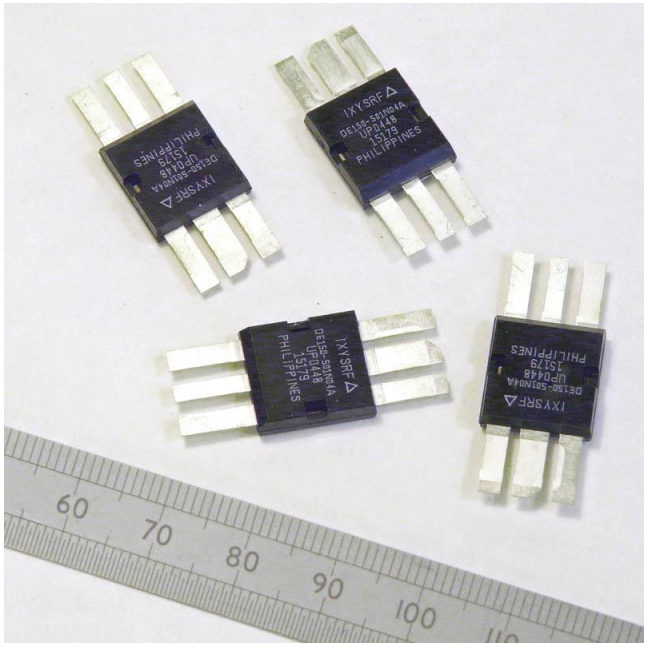
  Silicon carbide FETs

  (vacuum tubes)

FONT3 amplifier module



➢ 2kW peak output
10ns amplifier module



➢ typical fast, high voltage MOSFETs (DE150-501N)

Work programme

- **Design drive-beam phase FF system for CLIC**
- **Investigating amplifier component technologies:**

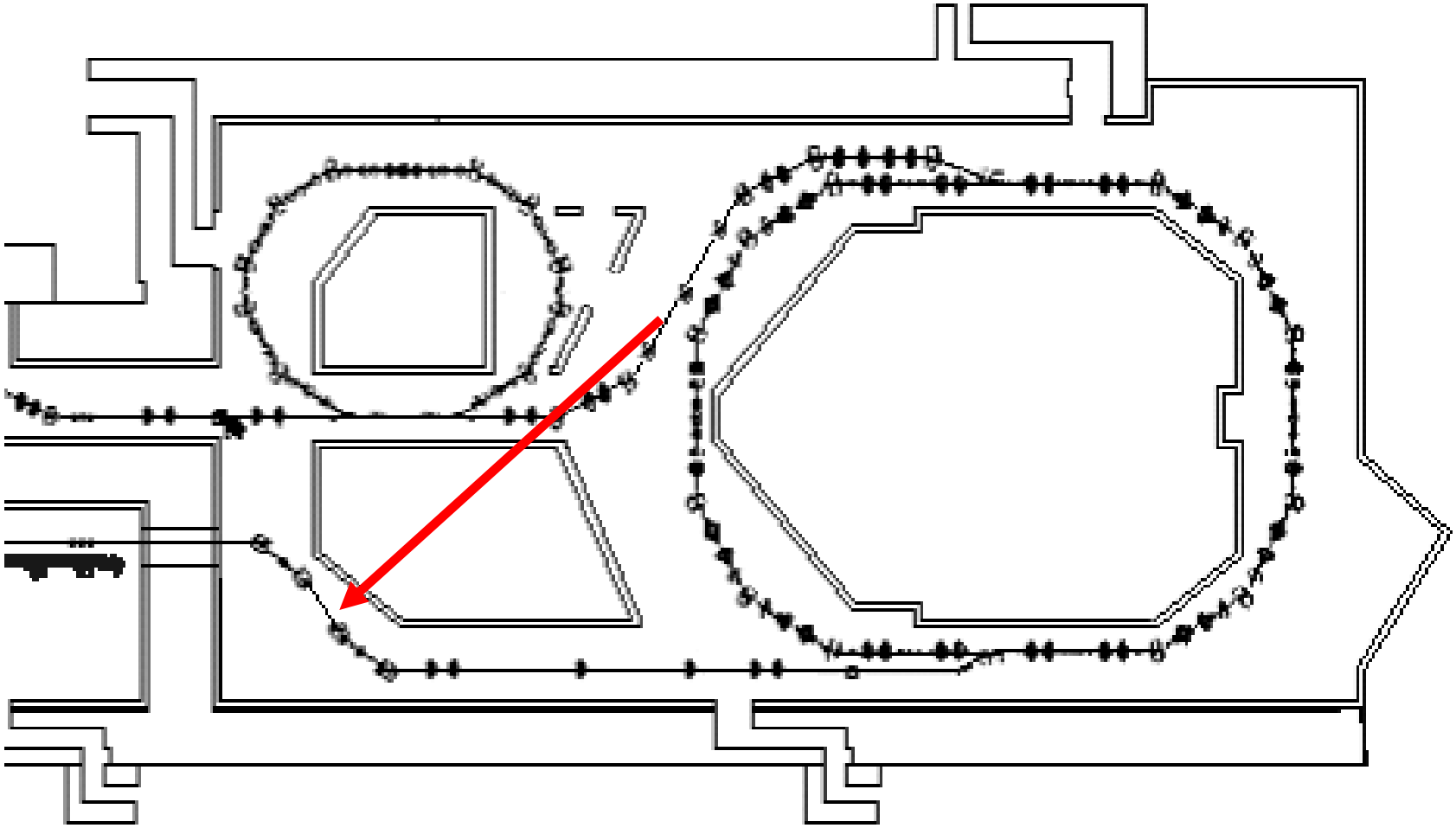
  HV silicon MOSFETs

  Silicon LDMOS FETs

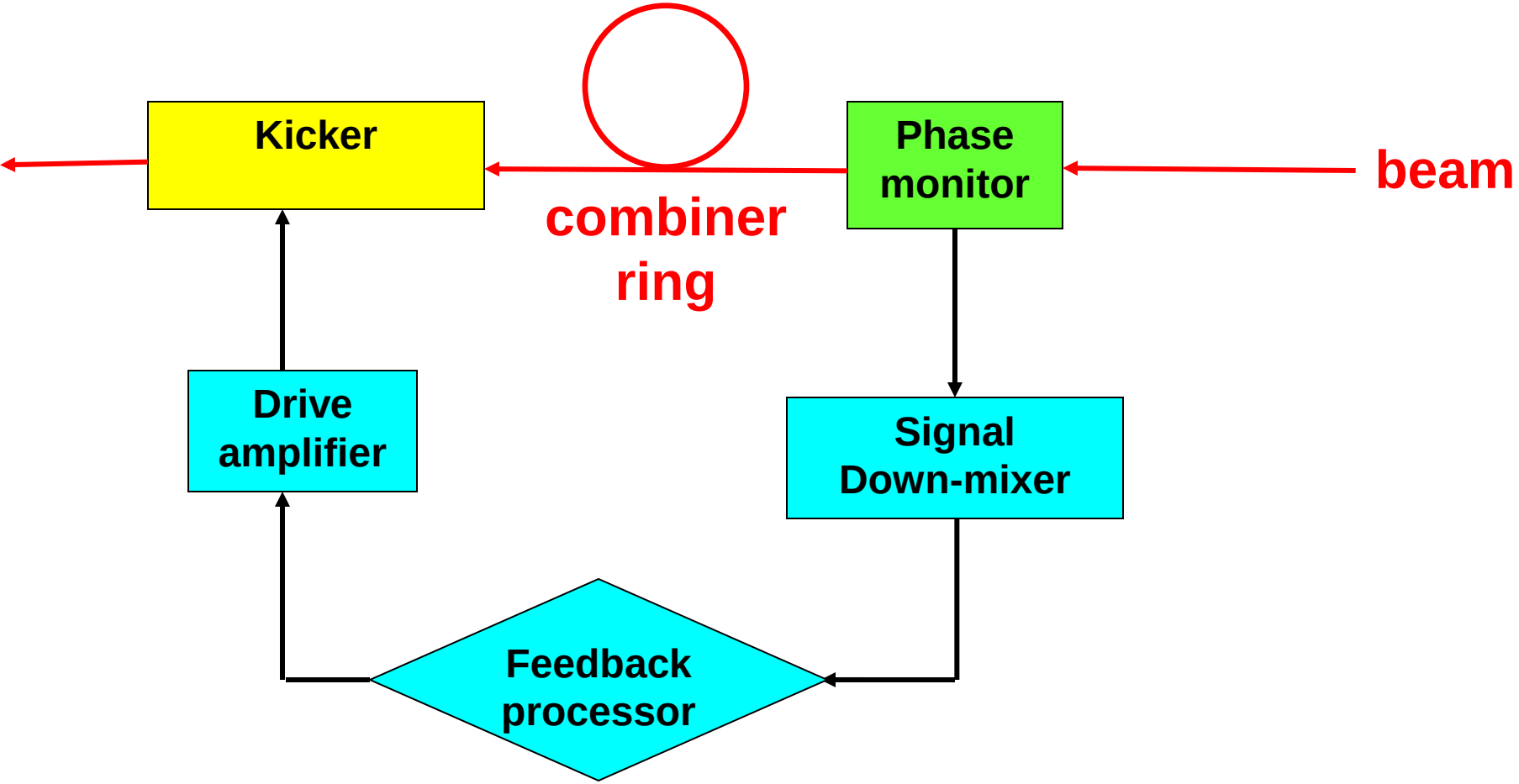
  Silicon carbide FETs

  (vacuum tubes)
- **Design and tests of prototype phase FF system at CTF3**

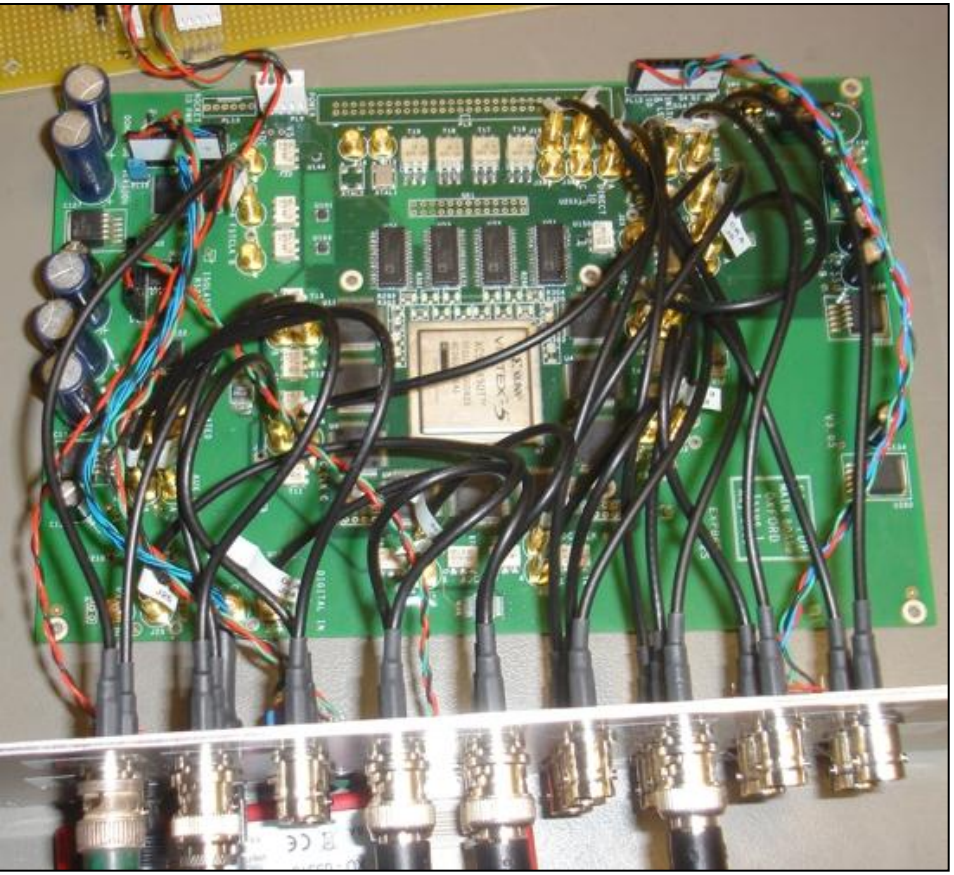
CTF3 phase FF prototype



CTF3 FF loop layout



FONT5 digital FB board



Xilinx Virtex5 FPGA

9 ADC input channels (TI ADS5474)

4 DAC output channels (AD9744)

Clocked at 357 MHz phase-locked to beam

Strategy for correction

Consider separate corrections for ‘slow’ + ‘fast’ components:

Either:

Combine drives before sending to kicker

or

Use dipole corrector for slow correction – preferred?

Amplifier strategy for CTF3

1. deliver a minimal spec system to CTF3 at an early date
2. upgrade this to a performance level approximating CLIC requirements
3. develop & prototype a design for CLIC capable of being costed

There are four main problem areas:
- the power amplifier modules (solid state systems contain many output modules)
- broadband transformers (and other magnetics)
- combining scheme for power module outputs
- system protection, packaging, control etc.

Will concentrate on each of these areas in turn

Proposed CTF3 amp design

First Stage:

- drive kickers as single-turn coils with one end grounded
- magnetic deflection only: needs double the drive current
- low drive voltage, so no (potentially difficult) broadband transformers
- sufficient to correct broad phase variations over 140ns
will not correct eg. the observed phase 'ripples' at ~20MHz

Second Stage:

- fix and/or improve the amplifier design (!)
- build more amplifiers (otherwise unchanged)
- drive the kickers from 2 and then all 4 ports
- drive principle remains the same
- with same voltage from each amplifier, total kicker drive V is x 2 or x4
this increases speed sufficiently to correct the 20MHz phase 'ripples'

Proposed CTF3 amp design

Third Stage:

- need to combine and transform the outputs to match the kicker

- system response should be flat to at least 30MHz; target is 60MHz

- system then will be close to CLIC requirements in all but power level

Resources

- **CLIC-UK agreement: 1/4/11 – 31/3/14**

  1.6 FTE/year (faculty, engineer, postdoc)

  250 kChF (materials + travel)
- **Continue this activity 2014-2016**
- **Providing additional resources from JAI/Oxford + CERN:**

  PhD student until end 2012

  could add another PhD student > 2012