JRA1 Design Review Summary

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Sensor development (Mark)

Demonstrator telescope sensor (Mimo-3M):

- AMS 0.35 um OPTO process, now with 12 or 17um epitaxial layer, 4 sub-arrays, 10 MHz, engineering run in summer 06, available February 07
- High density sensor, 512x512, 4 sub-arrays, 10-20 MHZ, available spring 07

Final telescope device:

- On pixel CDS and discriminator at end of column, good results from Mimosa-8, translation into AMS 0.35 OPTO ongoing
- Next step: 4-5 bit ADC, several designs, to replace discriminator

Summary of Mimo-2 WS(Gilles)

- USB Imager board + Software + lots of information
- Rate 1 board: 13 MB/s, limited by dead time on PC side,, max probably 20 MB/s
- Rate 6 boards: 60 MB/s total
- Interrupt handling: PC parallel port ACK line, commercial soft, 10 kHz, 0.1% IRQ lost
- USB overhead: event control over parallel port
- Full set up with 6 boards: 40 Hz, ok for demonstrator
- Interface to TLU board: NIM trigger, reset, busy, + interrupt request output to PC
- To be done: CDS check, trigger logic check, 6 board synch
- With zero suppression on board: expect 100 to 250 Hz (max Mimo-3M is 300 Hz), not for demonstrator
- DAQ ideas: RRPC, implemented via central file for commands and distributed files for data?

EUDRB Status (Angelo)

- VME64 format board for CDS and zero suppression, no dead time
- Digital daughter card, IEEE-1386 PMC to FPGA, outward USB 2.0 link, sequencing I/F for Mimo®-3M, Mimosa-5, Mimo-Roma
- Analogue daughter card (PMC format) for analogue input from sensor, voltage generation from common 12V
- Altera FPGA EP2C79F896C8 plus aux
- Trigger port on front panel, and/or trigger bus on back plane
- Full frame mode or sparsified mode
- Milestones: fitting FPGA ok, set-up of VME crate ok, mother board schematics almost ready, layout + daughter boards (outsourced) + VMS code end of May, prototype end of June 06
- Testing in fall of 2006, results in time with 2nd JRA1 review

Bonn/Mannheim DAQ (Peter)

- Existing DAQ, producer(s), event building, reader/writing, monitoring
- Communication based on shared dual port memory on single system
- Error checking, but no recovery
- All (connected) detectors must give data (at least dummy) for all triggers
- Needs shared memory communication across systems and process control
- DEPFET easy to integrate; other DUT like CCD?

JRA1 DAQ (Daniel)

- Based on Bonn/Mannheim DAQ + Strasbourg DAQ
- SOAP slow control protocol, I2O binary data protocol (attention: byte order)
- Alternative: custom solution based on TCP/IP sockets
- Central process control and run control
- Monitoring on full events, common event repository for monitoring or buffer ?
- Stable metadata to be kept in BOREvent
- Producers for monitoring data (e.g. position, temperature, time, TLU) so be attached to each event
- Initially, producer provides CDS and sparsification, must be able to provide raw and reduced data
- Clusterization and tracking in monitoring task: write event output in addition to histogram output (or use play-back) ?
- Windows is 1^{rst} implementation baseline

TLU Status (David)

- Demonstrator prototype based on commercial FPGA prototyping board, Orange Tree ZestSC1, USB 2 i/f to DAQ
- Six detector interfaces: 4xLVDS/RJ45, 2xLVDS/RJ45 or TTL/Lemo
- Four PMT inputs for beam trigger
- Event number (optional) as 100 Mbit/s serial on spare line, with de-serialiser provided
- EUDRB interface via VME backplane
- Strasbourg board interface: passive VME carrier board, with LVDS-NIM converter
- Schematics complete, PCB after easter, firmware design with synchronous logic, first prototype end of May 06.

sucimaPix Data Analysis (Antonio)

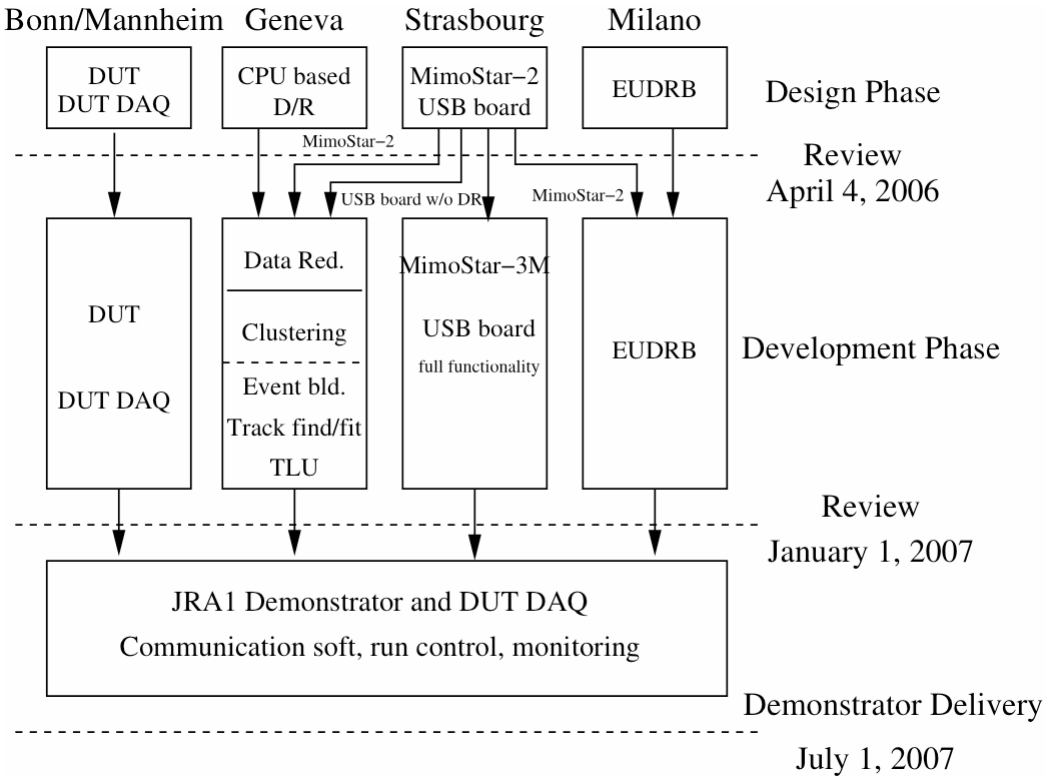
- Framework for pixel detector characterization only
- C++ coded, imbedded in root as shared libraries
- Available now, used with Mimosa family
- Requires root >3.5, Linux, Windows, MacOS
- THtml documentation, including root classes
- Internal data format, root Ttree TPixelMatrix
- Some detector specific data formats supported (e.g. LEPSI DAQ), otherwise converter is needed
- Sensor specs adjustable
- Modules: init, pedestal/noise, data reduction, histogram
- Clusterisation: fixed frame or recursive
- Standard histos for standard properties provided
- Basis for monitoring tasks and offline analysis

DESY Infrastructure (Ingrid)

- Testbeam area 24 re-built, container available
- Mechanics:
  - ingoing arm in fixed box, sensors on optical bench,
  - DUT on x-y-Φ-table in box with removable walls
  - outgoing arm in extra box,
  - same or different thermal enclosures
  - can be in B-field (except x-y-table)
- 2 PCs ordered, DAQ and analysis
- Solenoid magnet from KEK middle of 2006, operation needs expert, supported on movable stand

Where do we go from here?

- Next design review: January 1, 2007
- Need intermediate review with prototype milestones:
  - TLU prototype
  - DAQ multi-system prototype
  - EUDRB prototype
  - Producers for Mimo‰-2/3M, DEPFET, EUDRB
  - Monitor based on sucimaPix
- September 28/29, northern Italy
- Integration exercise with 1 Mimo‰-2 in fall of 2006, delivering integrated prototype system by Jan 07



Open technical issues

- High pixel density plane: probably worth doing, to be verified by simulation
- ADC or discriminator on final chip, to be verified by comparison
- Data format at various stages: intermediate TTree
- Interfaces to TLU: VME and/or LVDS/TTL/NIM, specified by device side
- Slow control monitoring: how and what (T, x/y, beam)
- Size and alignment of trigger counters

Conclusion:

- First milestone has been fulfilled, congratulations
- Need an intermediate milestone, September 28-29, 2006
- Deliverables: prototype of all demonstrator elements
- New deliverable: integrated proto-DAQ chain by January design review
- Regular Telecons only when needed