INFN-EUDRB

A VME based DAQ card for MAPS sensors to be used on test beam experiments.
STATUS REPORT

This note outlines the basic features and the status of the VME based card being developed at INFN Ferrara for the acquisition of data from Monolithic Active Pixel Sensors (MAPS) to be characterized or employed in a test beam foreseen for June 2006.

Its first application will be to readout the MIMO-Roma MAPS in a test beam foreseen for next June and thus the development is being carried out in collaboration with INFN-Roma3 and University of Insubria.

The board could also be a candidate for reading out the MAPS in the EUDET telescope and in this view its main features are presented here.

Acknowledgments:

While some of the features presented here are quite novel, the general outline of the card is inspired by previous works by the People and Institutions involved with the SUCIMA project. The recent workshop at IRES in Strasbourg also has provided valuable contribution in the development of the board

Basic features:

a) the card carries daughter cards with a standard interface to the motherboard and different flavours of input connectors and implemented functions, to adopt to different type of sensors.

b) The amplifier and A/D converter daughter card will be based on SUCIMA's design

c) VME64x slave bus interface with MBLT capability (VME64-2e block transfer mode)(*).

d) Interface to a simple trigger protocol (trigger request, event number, busy, holdoff) on cable segments accessible via the user-defined rows of the VME P2 connector

e) Zero suppressed readout mode to minimize the readout dead-time while in normal data taking.

f) Full frame readout mode for debugging or off-line pedestal and noise calculations

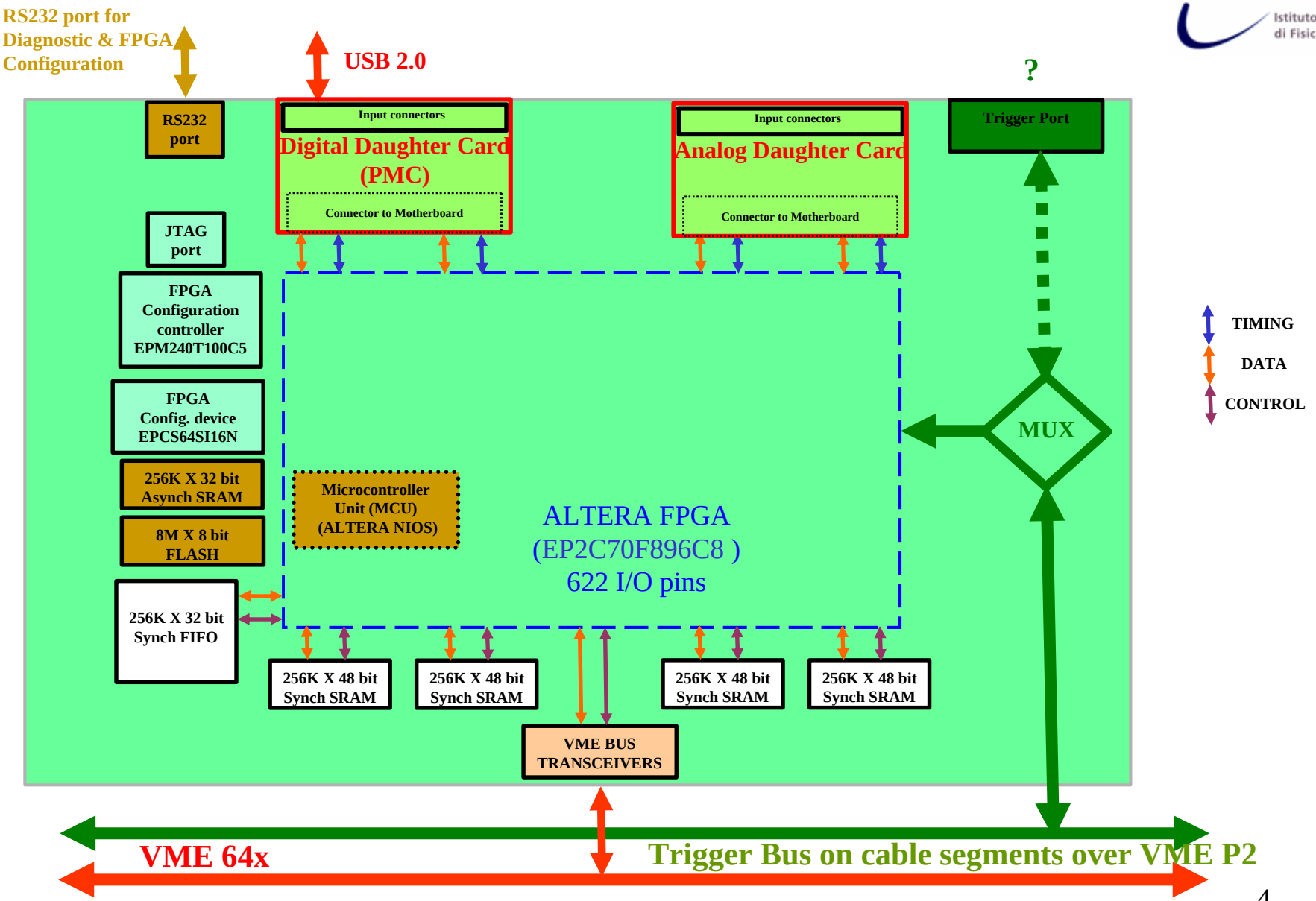
g) USB2.0 interface for stand-alone operation of the board

h) NIOSII-32, 32 bit "soft" microcontroller implemented in the CycloneII FPGA. It handles tasks like:

- a) on-line calculation of pixel pedestal and noise by tapping data samples as they are read from the sensors
- b) remote configuration of the FPGA via RS-232, VME, USB2.0
- c) on board diagnostic

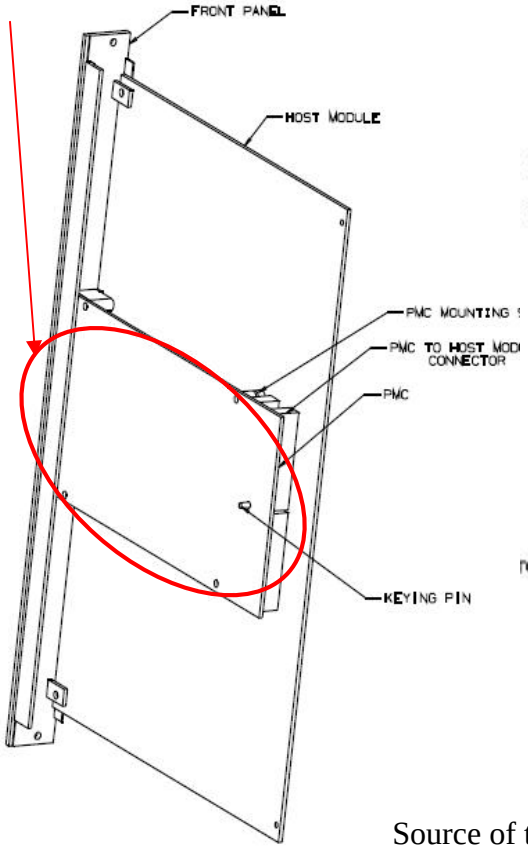
(*) burst transfer rate of 160MB/s. Sustained bandwidth to be detemined with the CPU being purchased for the test setup, a Motorola MVME6100-0163

A VME based DAQ card for MAPS sensors to be used on test beam experiments



The sockets for the Digital daughter card comply to the PCI MEZZANINE CARD (PMC) Standard

IEEE-1386 PMC



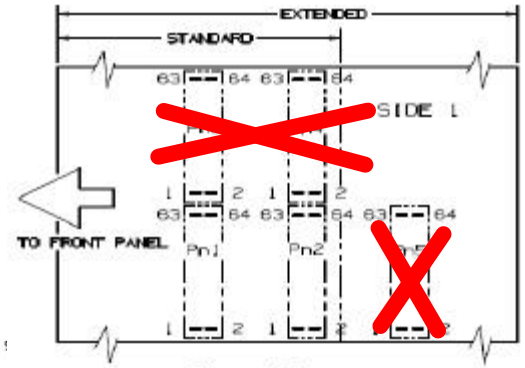


Figure 5-1
Connector Orientation on PMC, Side 1

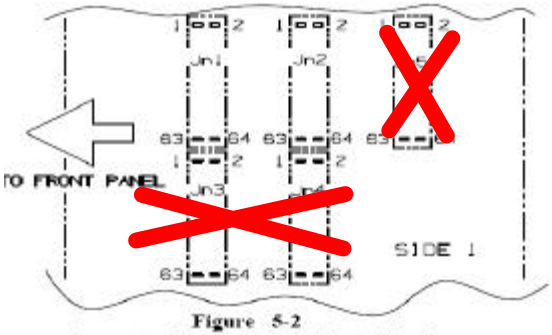


Figure 5-2
Connector Orientation on Host, Side 1

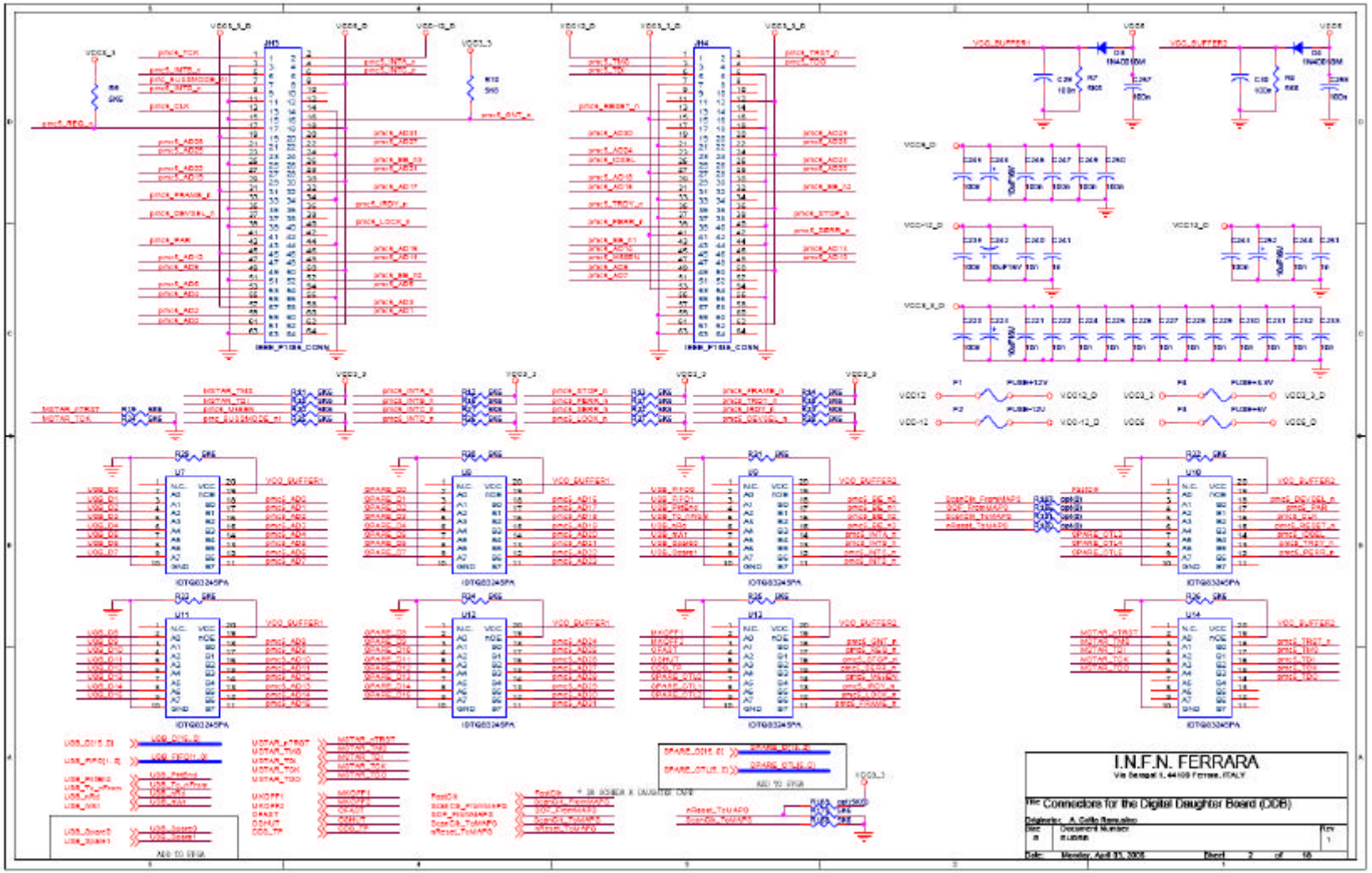
Source of the drawings:
" Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC"
Sponsored by the Bus Architecture Standards Committee
of the IEEE Computer Society P1386.1/Draft 2.0, April 4, 1995

32 bit bus width

PMC/PPMC 32 Bit Connector Pin Outs and Signal Names

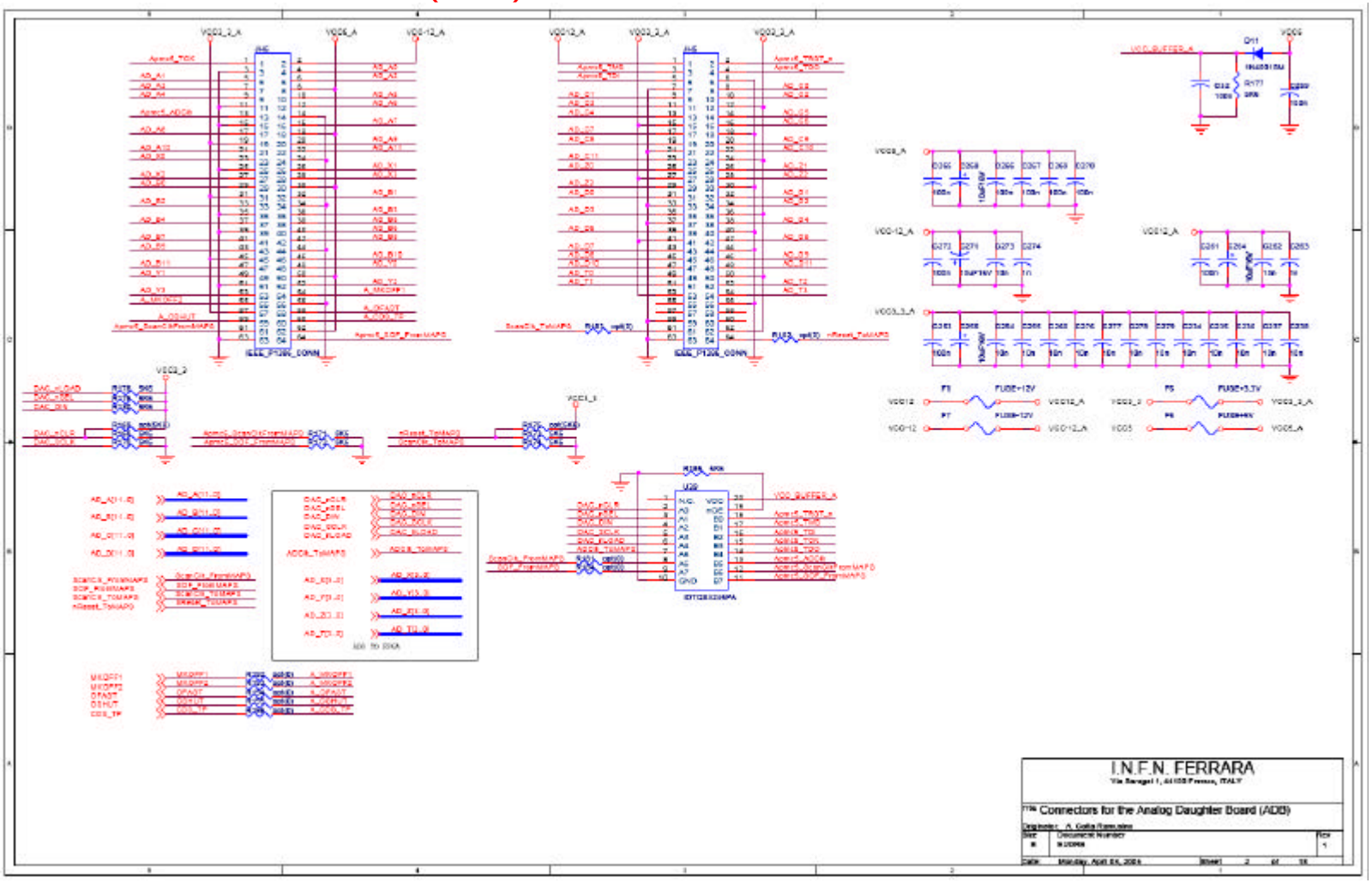
PN1 Connector				PN2 Connector			
Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	TCK	2	-12v	1	+12v	2	TRST#
3	Ground	4	INTA#	3	TMS	4	TDO
5	INTB#	6	INTC#	5	TDI	6	Ground
7	PRESENT#	8	+5v	7	Ground	8	PCI-A9
9	INTD#	10	PCI-B14	9	PCI-B10	10	PCI-A11
11	Ground	12	3.3Vaux	11	PUP	12	+3.3v
13	PCICLK	14	Ground	13	RST#	14	PDN
15	Ground	16	GNT#	15	+3.3v	16	PDN
17	REQ#	18	+5v	17	PME#	18	Ground
19	V{I/O}	20	AD[31]	19	AD[30]	20	AD[29]
21	AD[28]	22	AD[27]	21	Ground	22	AD[26]
23	AD[25]	24	Ground	23	AD[24]	24	+3.3v
25	Ground	26	C/BE[3]#	25	IDSEL	26	AD[23]
27	AD[22]	28	AD[21]	27	+3.3v	28	AD[20]
29	AD[19]	30	+5v	29	AD[18]	30	Ground
31	V[I/O]	32	AD[17]	31	AD[16]	32	C/BE[2]#
33	FRAME#	34	Ground	33	Ground	34	IDSELB
35	Ground	36	IRDY#	35	TRDY#	36	+3.3v
37	DEVSEL#	38	+5v	37	Ground	38	STOP#
39	Ground	40	LOCK#	39	PERR#	40	Ground
41	PCI-A40	42	PCI-A41	41	+3.3v	42	SERR#
43	PAR	44	Ground	43	C/BE[1]#	44	Ground
45	V[I/O]	46	AD[15]	45	AD[14]	46	AD[13]
47	AD[12]	48	AD[11]	47	M66EN	48	AD[10]
49	AD[09]	50	+5v	49	AD[08]	50	+3.3v
51	Ground	52	C/BE[0]#	51	AD[07]	52	REQB#
53	AD[06]	54	AD[05]	53	+3.3v	54	GNTB#
55	AD[04]	56	Ground	55	PMC-RSVD	56	Ground
57	V[I/O]	58	AD[03]	57	PMC-RSVD	58	EREADY
59	AD[02]	60	AD[01]	59	Ground	60	RESETOUT#
61	AD[00]	62	+5v	61	ACK64#	62	+3.3v
63	Ground	64	REQ64#	63	Ground	64	MONARCH#

The interface to the Digital daughter card complies to the PCI MEZZANINE CARD (PMC) Standard



The USB 2.0 link has been moved to the Digital Daughter card for added flexibility

The interface to the Analog daughter card has power supply pins compatible with the PCI MEZZANINE CARD (PMC) Standard



The data paths from A/D converters have been made 16 bit wide for added flexibility

Daughter cards pinout at the front panel

PRELIMINARY DIGITAL DAUGHTER CARD connector pinout
PRELIMINARY DIMENSIONS 75 x 120 mm

ALTERNATE PINOUT OF CONNECTOR D_J1 (RJ-45)
FOR MIMOSTAR / MIMOSA 5

RJ-45 conductor no.	Signal Name	Type	Standard
1	MSTAR_TCK / MKOFF1	O/O	3.3V TTL
2	GND		
3	MSTAR_TMS / MKOFF2	O/O	3.3V TTL
4	MSTAR_TDI / OFAST	O/O	3.3V TTL
5	GND		
6	MSTAR_TDO / OSHUT	I/O	3.3V TTL
7	GND		
8	MSTART_Ntrst / CDS_TP	O/O	3.3V TTL

ALTERNATE PINOUT OF CONNECTOR D_J2 (RJ-45)
FOR MIMOSTAR / MIMOSA 5

RJ-45 conductor no.	Signal Name	Type	Standard
1	MSTAR_CLKRDn / M5_CLKRDn	O/O	LVDS
2	MSTAR_CLKRDp / M5_CLKRDp	O/O	LVDS
3	GND		
4	GND		
5	MSTAR_CLK10Xp / ----------	O/O	LVDS
6	MSTAR_CLK10Xn / ----------	O/O	LVDS
7	MSTAR_SYNCp / M5_nRSTp	O/O	LVDS
8	MSTAR_SYNCn / M5_nRSTn	O/O	LVDS

ALTERNATE PINOUT OF CONNECTOR D_J3 (RJ-45)
FOR MIMOSTAR / MIMOSA 5 / MIMO-ROMA

RJ-45 conductor no.	Signal Name	Type	Standard
1	LVDSOUT4n / LVDSOUT4n / MR_CLKOUTn	I / I	LVDS
2	LVDSOUT4p / LVDSOUT4p / MR_CLKOUTp	I / I	LVDS
3	LVDSOUT3n / LVDSOUT3n / ----------	I / I	LVDS
4	LVDSOUT3p / LVDSOUT3p / ----------	I / I	LVDS
5	LVDSOUT2n / LVDSOUT2n / ----------	I / I	LVDS
6	LVDSOUT2p / LVDSOUT2p / ----------	I / I	LVDS
7	LVDSOUT1n / LVDSOUT1n / MR_SOF_OUTn	I / I	LVDS
8	LVDSOUT1p / LVDSOUT1p / MR_SOF_OUTp	I / I	LVDS

PINOUT OF CONNECTOR D_J4 (USB-B)
FOR MIMOSTAR / MIMOSA 5 / MIMO-ROMA

USB-B conductor no.	Signal Name	Type	Standard
1	+ 5V		
2	- DATA		
3	+ DATA		
4	GND		

PRELIMINARY ANALOG DAUGHTER CARD connector pinout
PRELIMINARY DIMENSIONS 75 x 120 mm

PINOUT OF CONNECTOR A_J1 (RJ-45)

RJ-45 conductor no.	Signal Name	Type	Standard
1	ASG3p	In	
2	ASGL3n	In	
3	ASGL1p	In	
4	ASGL1n	In	
5	ASGL2p	In	
6	ASGL2n	In	
7	ASGL0p	In	
8	ASGL0n	In	

PINOUT OF CONNECTOR A_J2 (RJ-45)

RJ-45 conductor no.	Signal Name	Type	Standard
1	DAC_OUT1	Out	
2	GND		
3	DAC_OUT2	Out	
4	GND		
5	DAC_OUT3	Out	
6	GND		
7	DAC_OUT4	Out	
8	GND		

PINOUT OF CONNECTOR A_J3 (LEMO)

LEMOconductor no.	Signal Name	Type	Standard
1	ASGL0p	In	
2	GND		

PINOUT OF CONNECTOR A_J4 (LEMO)

LEMOconductor no.	Signal Name	Type	Standard
1	ASGL1p	In	
2	GND		

PINOUT OF CONNECTOR A_J5 (LEMO)

LEMOconductor no.	Signal Name	Type	Standard
1	ASGL2p	In	
2	GND		

PINOUT OF CONNECTOR A_J6 (LEMO)

LEMOconductor no.	Signal Name	Type	Standard
1	ASGL3p	In	
2	GND		

PINOUT OF CONNECTOR A_J7 (LEMO)

LEMOconductor no.	Signal Name	Type	Standard
1	External Pixel Scan Clock (MIMO-ROMA)	In	
2	GND		

PINOUT OF CONNECTOR A_J8 (LEMO)

LEMOconductor no.	Signal Name	Type	Standard
1	External "Start Of Frame" (MIMO-ROMA)	In	
2	GND		

Overview of the operation of the EUDRB card:

- A/D converter clock rate (for the daughter cards whit analog input from the sensors): at the moment up to 15MHz.

- frame acquisition time: for a MIMOSA-V 1Mpixel sensor with 4 independent outputs sampled @15MHz:
262.144 * 66.6 ns = 17,476 ms (four quadrants work simultaneously)

-readout modes and trigger processing times

- "Full Frame" readout mode:

In this operating mode the card responds to a trigger by sending out ALL pixel readings (12bits+padding to 16bits) for at least 3 frames: the frame being acquired at trigger time, the preceding one and the following one, a total of about 6MB per event.

It is assumed that in this "development" mode the MAPS-DAQ it is allowed to stop the recording of new data from the MAPSs until the three frames selected by the trigger have been sent to the data acquisition CPU.

Also, assuming an average data bandwidth of 120MB/s (somewhat less than the peak bandwidth) on the VME backplane each event will be acquired by the VME CPU in about 1/20s per sensor.

The total trigger processing time at the crate level will then depend from the total number of MAPS to be read out.

The latency in the response can be no less than a frame acquisition time.

The total trigger processing time includes the time to reset and restart the detectors at the end of the lengthy readout phase.

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- "Sparsified" (zero suppressed) readout mode:

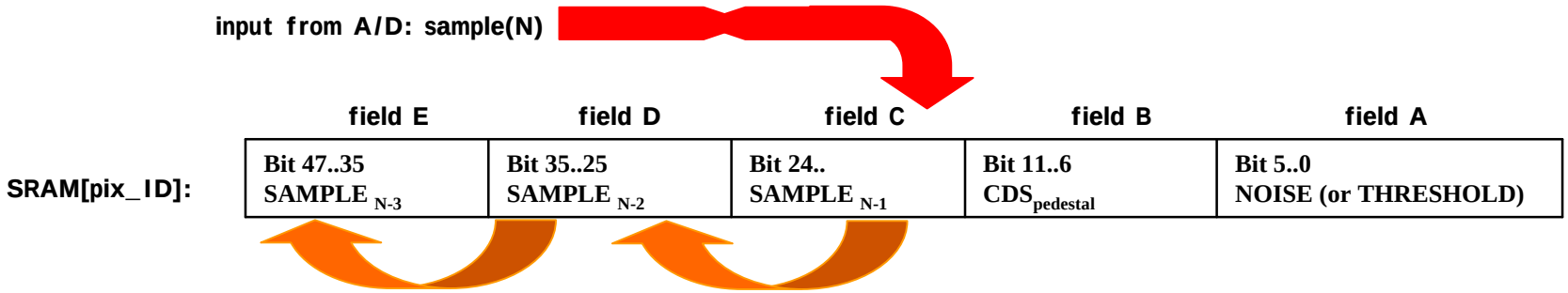
In this operating mode the card responds to a trigger by sending out a packet that could be formatted as follows (for 64 bits VME transfers):
(*) this last data would be meaningless in case the total HitCount were odd

"COMPACT" MODE packet structure					
Packet Header	Bit63..56 "H"	Bit55..48 Event Counter (from trigger scaler)	Bit47..40 Frame Counter	Bit39..32 Empty	Bit31..0 Empty
Data 1, Data0	Bit 63..52 Pixel Data	Bit 51..32 Pixel Address	Bit 31..20 Pixel Data	Bit 19..0 Pixel Address	
...					
DataN, Data N-1	Bit 63..52 Pixel Data (*)	Bit 51..32 Pixel Address(*)	Bit 31..20 Pixel Data	Bit 19..0 Pixel Address	
Packet Trailer	Bit63..56 "T"	Bit55..48 Event Counter (from trigger scaler)	Bit47..40 Frame Counter	Bit39..32 Empty	Bit31..0 HitCount

Or, alternatively,
we could send out the two raw data from which CDS can be calculated off-line:

"Extended information" MODE packet structure						
Packet Header	Bit63..56 "H"	Bit55..48 Event Counter (from trigger scaler)		Bit47..40 Frame Counter	Bit39..32 Empty	Bit31..0 Empty
Data0	Bit 63..56 0	Bit 55..44 Pixel After	Bit 43..32 Pixel Before	Bit 31..26 Pixel pedestal	Bit 25..20 Pixel noise	Bit 19..0 Pixel Address
...						
Packet Trailer	Bit63..56 "T"	Bit55..48 Event Counter (from trigger scaler)		Bit47..40 Frame Counter	Bit39..32 Empty	Bit31..0 HitCount

The packet contains the data only for those pixels whose signal was found above threshold after ON-LINE CDS and (pedestal+noise) subtraction.
I am assuming that each SRAM location for pixel data is organized as follows
(the graphics shows the data flow for updating the pixel data with Frame(N)'s new sample):



I am assuming that in the "sparsified" mode the CDS (correlated double sampling) is made according to the following rule:
"

1) When the trigger signal arrives, let's say in the middle of sampling Frame N's data, the sampling controller on the FPGA latches the address of the pixel whose data is currently being updated, lets' say: pix_ID_{Trig}.
2) Then it evaluates the pedestal subtracted CDS as follows:

$$CDS_{ped\_sub} = sample_N(pix\_ID) - sample_{N-1}(pix\_ID) - CDS_{pedestal}$$

storing the result to an embedded FIFO if the pedestal subtracted CDS is above threshold. $Sample_{N-1}(pix\_ID)$ is fetched from field C of the SRAM[pix_ID] contents
3) Step 2 is repeated for all pixels until:

$$pix\_ID_{Last} = pix\_ID_{Trig} - 1$$

Eventually pix_ID has overflowed and restarted from 0. By then, the contents of the field C at all locations of the SRAMs have been updated to $sample_N(pix\_ID)$.
This is OK, since after the rollover, the quantity to evaluate is:

$$CDS_{ped\_sub} = sample_{N+1}(pix\_ID) - sample_N(pix\_ID) - CDS_{pedestal}$$

i.e. again the new sample from the A/D converter minus the content of field C in the active location pointed by pix_ID
"

continues....

.... continuing

Assuming all of the above it follows that, in "sparsified" acquisition mode, **the preparation of the output data packet in response to a trigger can start as soon as the trigger is received and that it only needs to last a number of cycles of detector clock after the trigger equal to the size of a quadrant** (plus some overhead and plus the data transfer time toward the data acquisition CPU).

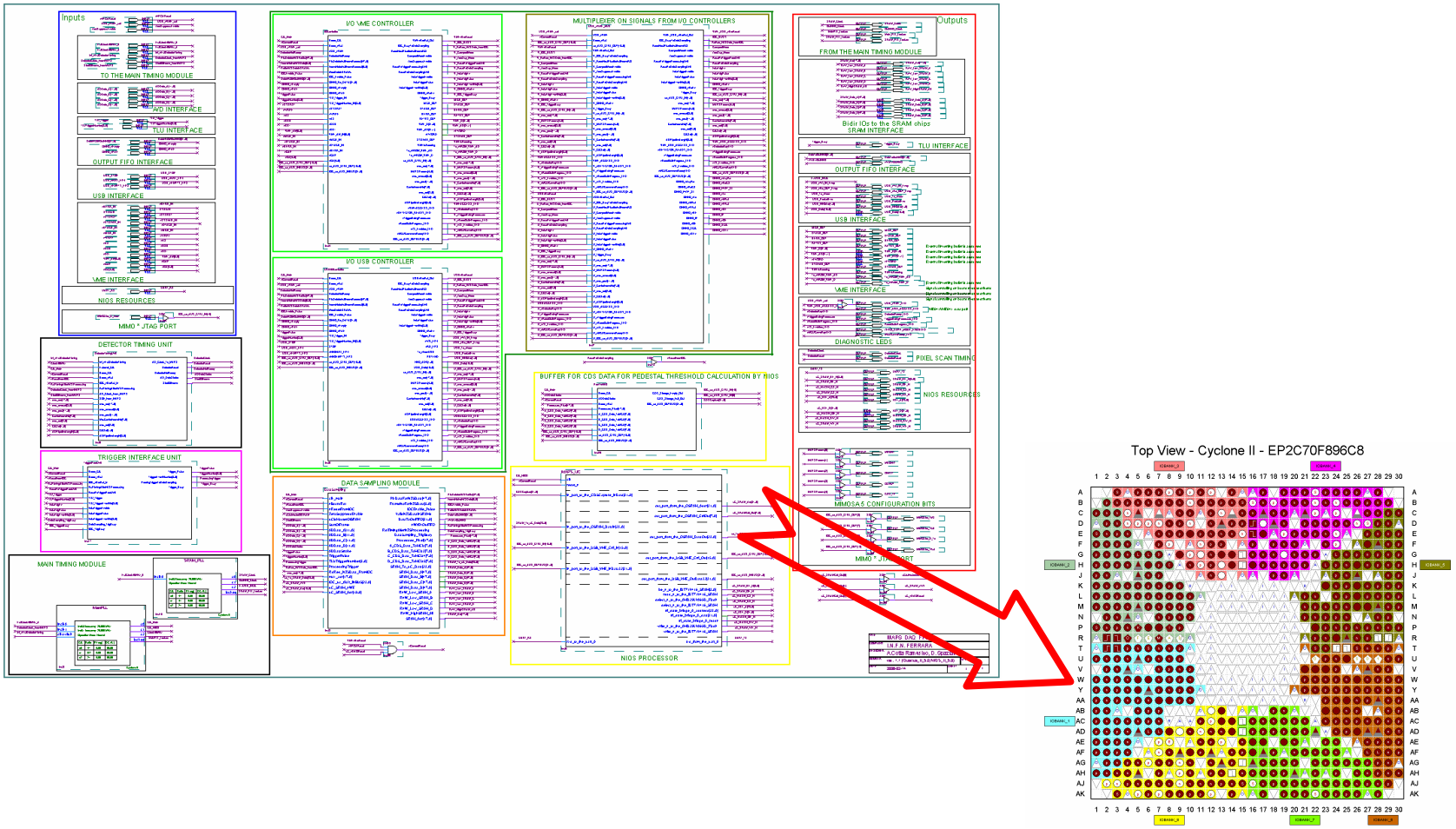
Processing of ONE trigger needs not to interrupt the sampling of pixel data at the input port.

The DAQ card issues an XOFF signal while processing a trigger request.

An XOFF signal could also be generated at the crate level by a suitable "Trigger-Interface" card, which would distribute the trigger signals over a private backplane built on the free pins of the VME J2 connector and monitor the collection of data from the DAQ cards by the crate's CPU.

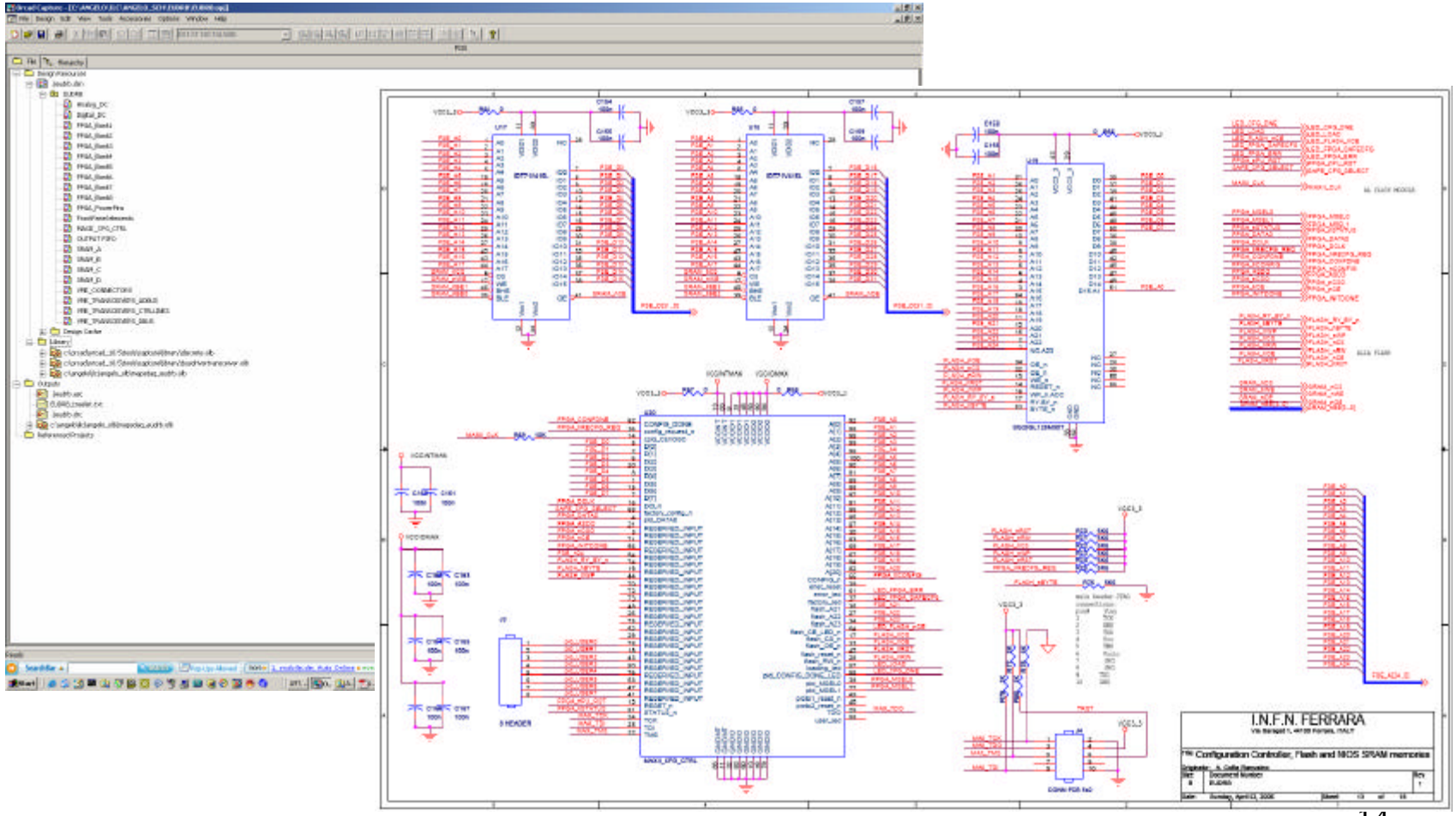
Milestones:

1) Fitting of FPGA design: beginning of March 2006 (thesis work by Davide Spazian)



2) Setup of a MVME6100 VME CPU in a VME64x crate: end of March 2006
(with ackowledgements to Dr. Paolo Branchini of INFN-ROMA 3)

3) Schematic of mother board: almost done (2nd week of April 2006)
(missing: output FIFO, power regulator, front panel elements)



Work in progress:

- Schematic of daughter cards: end of April 2006
- Layout of mother board at INFN-ROMA 3 by Domenico Riondino: end of May 2006
- Layout of daughter cards (outsourced): end of May 2006
- VME DAQ code : end of May 2006 (thesis work by Lorenzo Chiarelli)
- Prototypes to be tested: end of June 2006

Repository of project files:

http://www.fe.infn.it/electron/protetta/

(user and password upon request)