ASIX: A Prototype ASIC with Cluster-Based Readout for X-ray Hybrid Pixel Detectors

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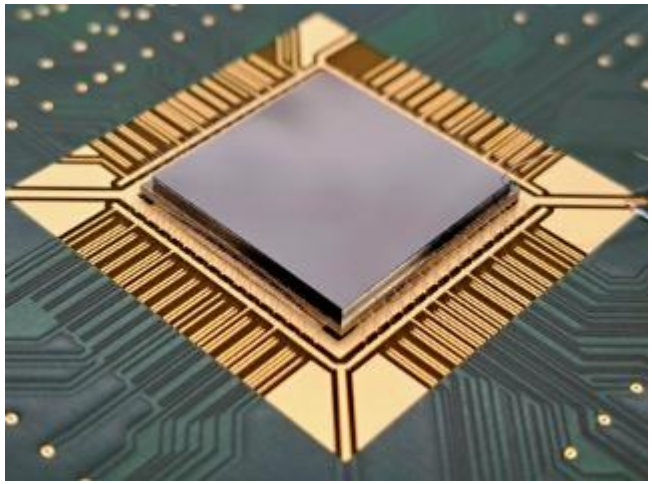
Analog Spectral Imager for X-rays

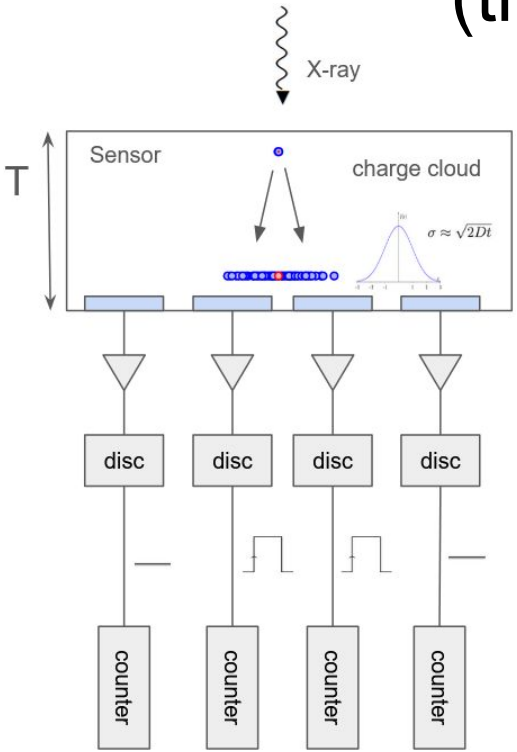


We plan to develop a new **Hybrid Pixel Detector** with event-driven analog read-out and single-photon sensitivity for high resolution **X-ray spectral imaging**

<u>Effective Single Photon processing</u>

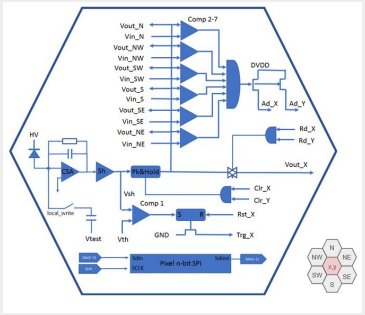
- baseline 300 um Si sensor, with the option of using different thickness and/or High-Z sensors
- 50u pixels on hexagonal arrangement
- <10 um spatial resolution
- ~300eV energy resolution (FWHM at 8 keV)
- 30 ke^- full scale linear range
- 10^8 ph/sec/cm^2

HPD resolution limit (the charge sharing issue)

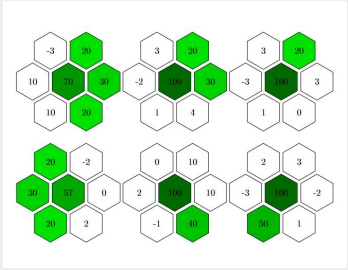


Double Counting & Energy peak distortion can be mitigated by means of complex in-pixel arbitration architectures. However, front-end (FE) noise and discriminator threshold dispersion still limit the performance of conventional sensors.

The ASIX way

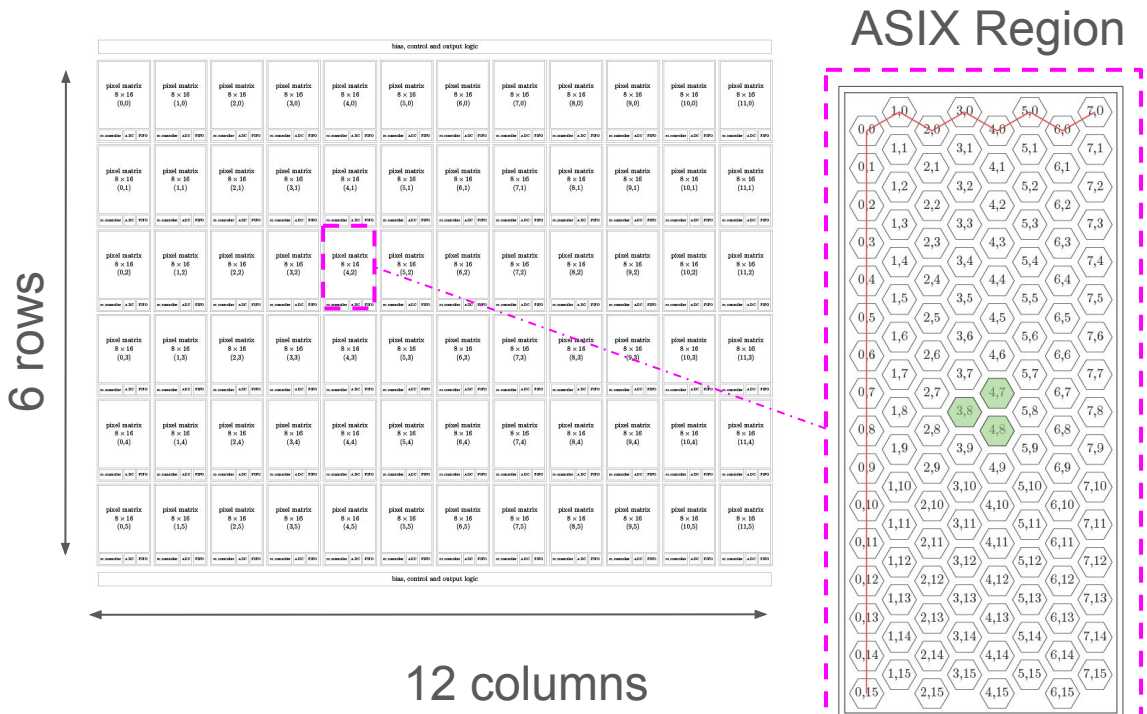


The cluster charge distribution will be precisely isolated and acquired via a highly partitioned analog readout architecture with ultra-low noise FEs and on-chip A/D conversion.

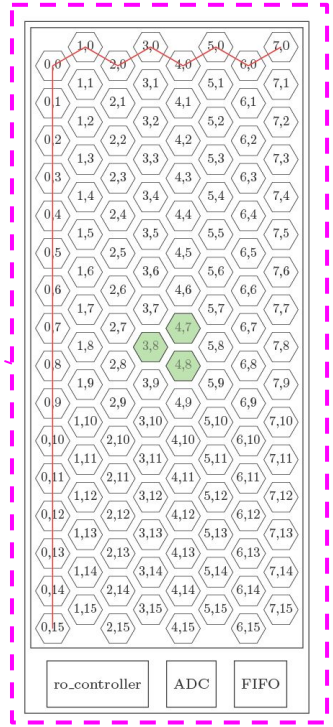


Pixels' charge data is extracted distortion-free and transmitted to the DAQ allowing for energy and position reconstruction and user-customizable offline re-binning

ASIX architecture



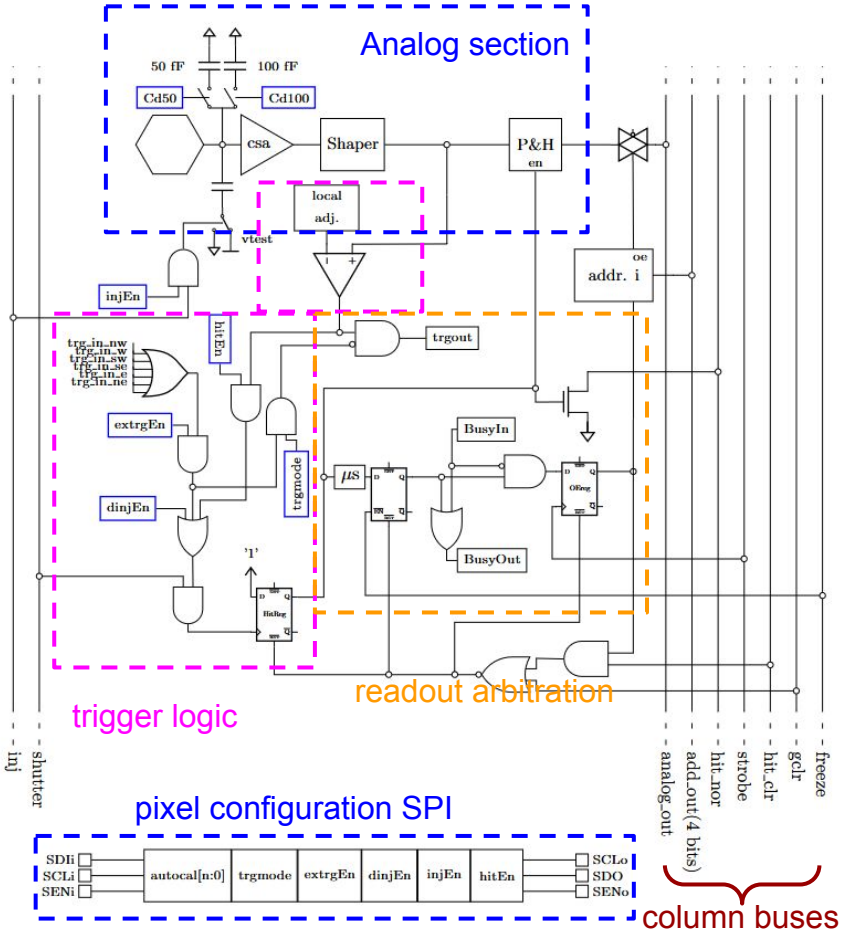
ASIX Region



The ASIX pixel matrix is subdivided into regions, each comprising an 8 × 16 pixel group and dedicated readout electronics, including a 10-bit ADC, a data-out FIFO, and the readout controller.

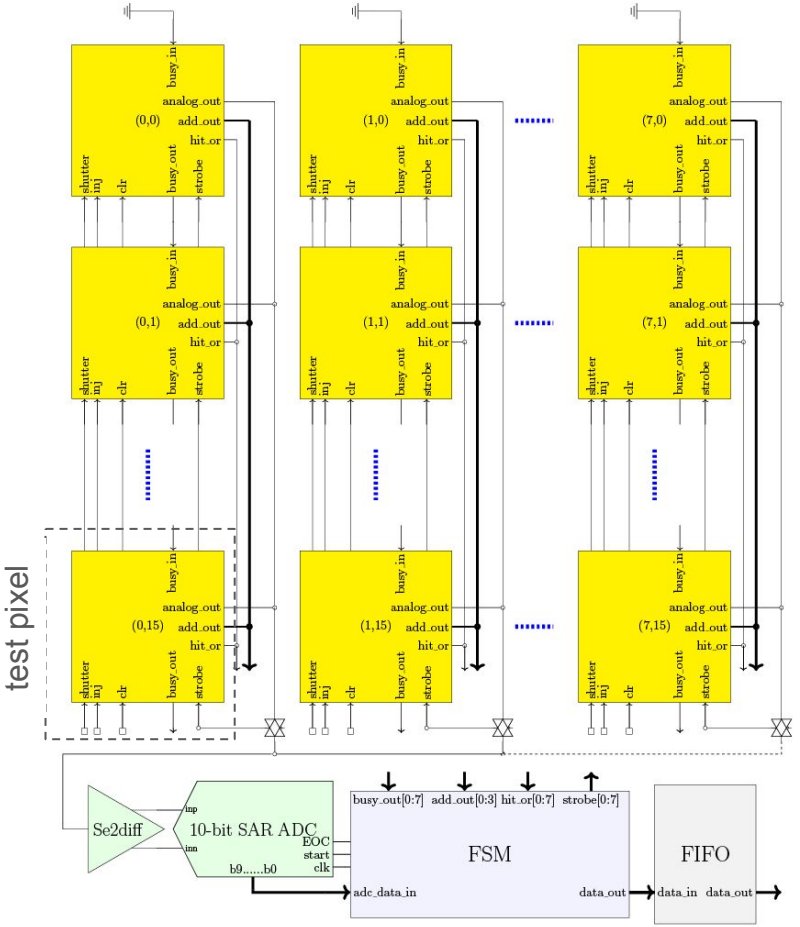
The final ASIX demonstrator will feature a 96 × 96 pixel matrix (12 × 6 regions, ~6 × 5 mm²).

In pixel electronics

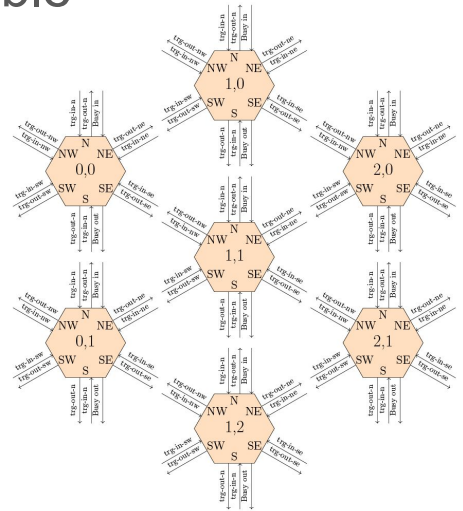


- ultra-low-noise frontend (<30e$^-$ ENC w 100fF)
  - <1us shaping time
  - peak-detector
  - precise charge injection (28e$^-$/mV)
- self-triggering logic
  - pixels exchange trigger signal with neighbours
- 5-bits local threshold correction
- column-drain readout arbitration logic
- SPI register stores the trigger and readout configuration along with local threshold correction DAC value

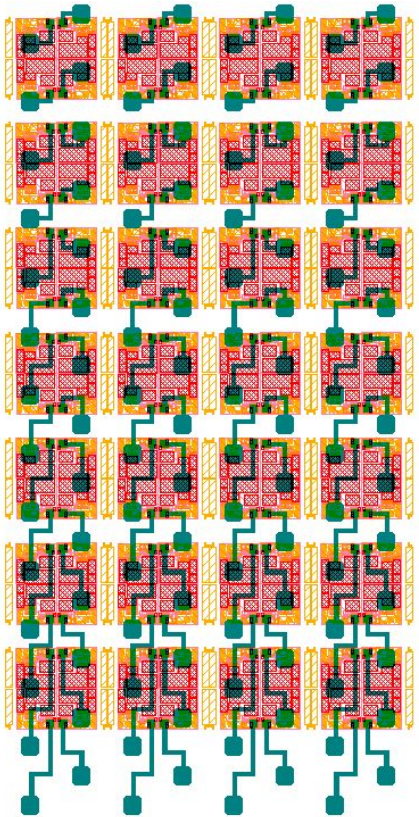
Region architecture



- 8 X 16 pixels
- readout sequencing logic
- on-chip 10-bit SAR ADC
- region data FIFO
- modular design, seamless 4-sides abuttable

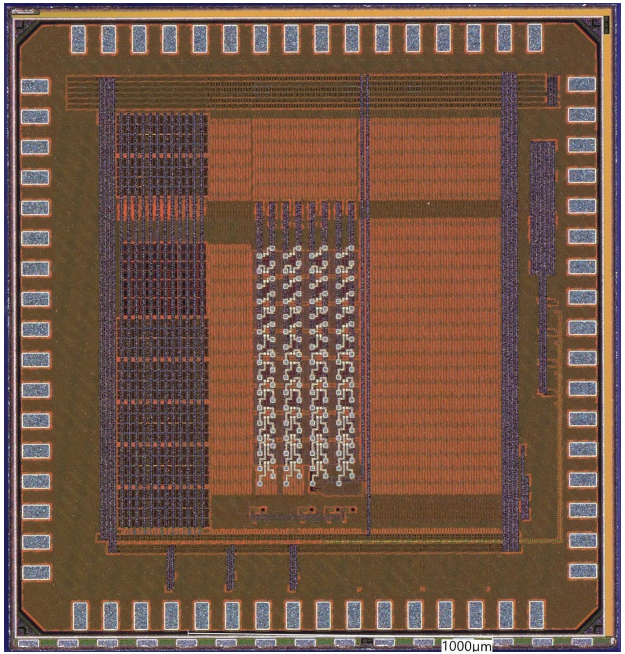


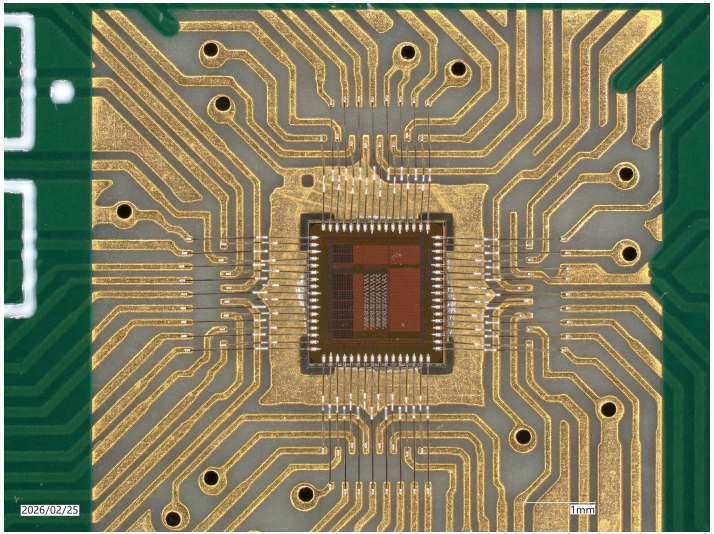
Region layout



- 45 um square pitch for pixel electronics
- sensor 50 um hexagonal pixel fanout
- 800 um X 320 um overall size
- 80 X 320 um to fit ADC, FIFO and readout sequencer
- modular design
  - seamless 4-sides abuttable

ASIX Readout chip prototype

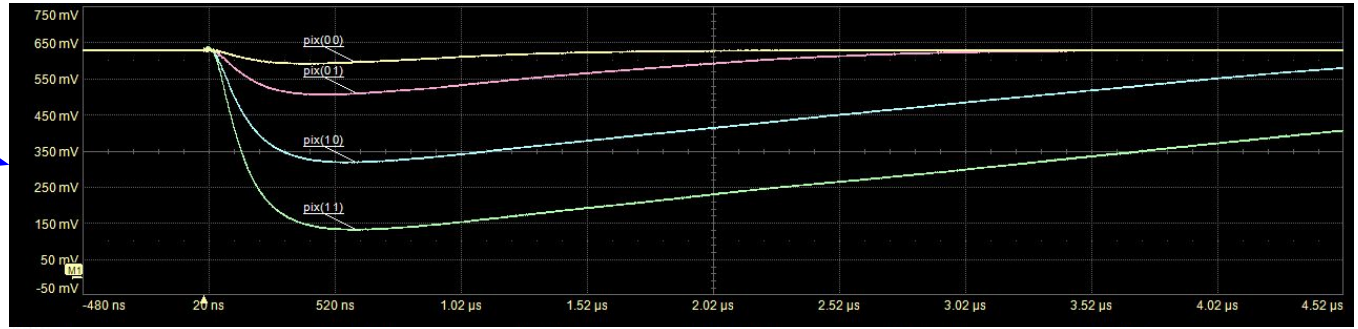


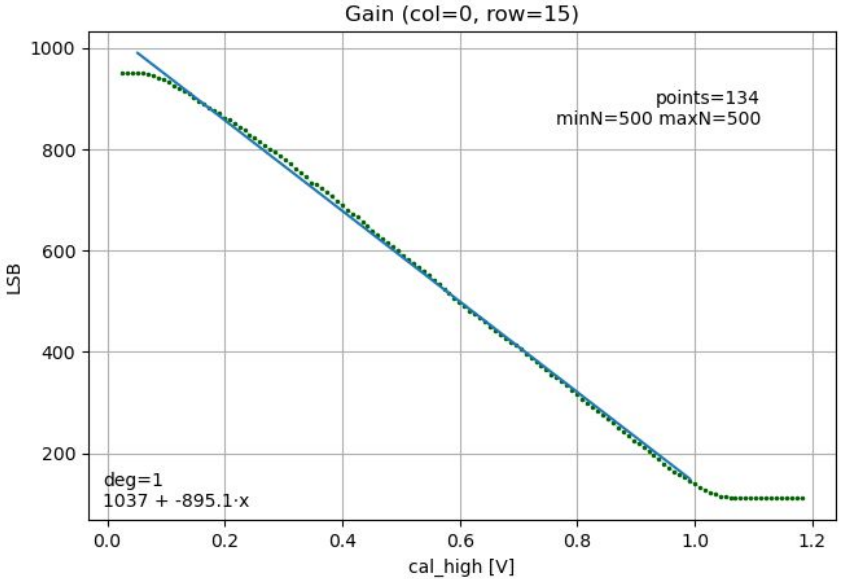


- 8 X 16 fully functional ASIX region with serial dataout
- 100 samples from MPW
- 2 samples mounted and tested for basic performance verification

Pixel electrical test - Full I/O characteristic

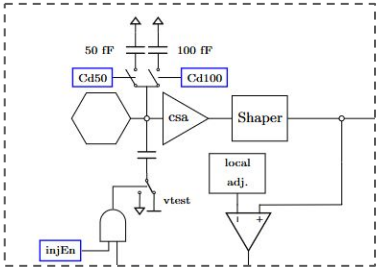
Test pixel shaper output response to injected charges of 4 ke$^-$, 8 ke$^-$, 16 ke$^-$, and 24 ke$^-$

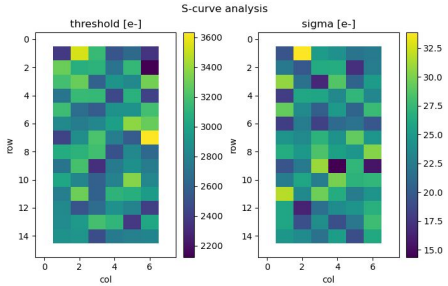




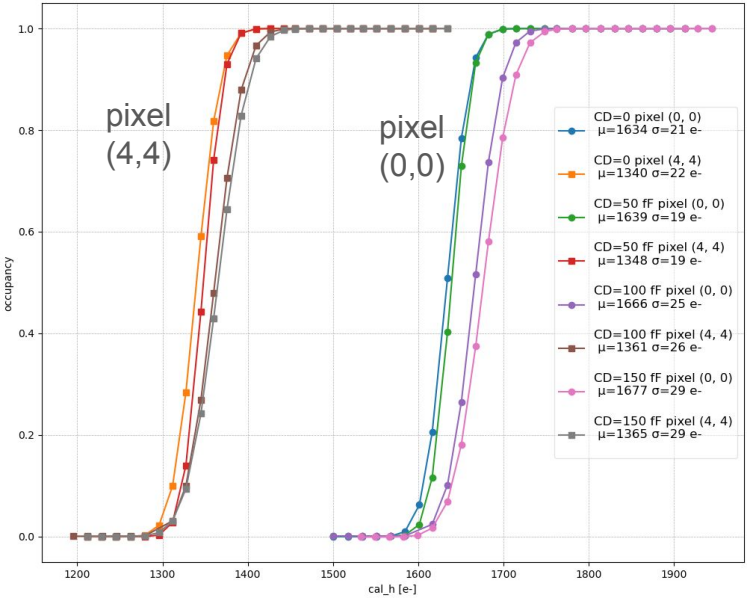
- test pixel shaper output can be probed
  - peaking time <500 ns
  - return to baseline <10us can be <1us for low energy photons
- full-chain response
  - includes readout and A/D conversion
  - early saturations, root causes identified

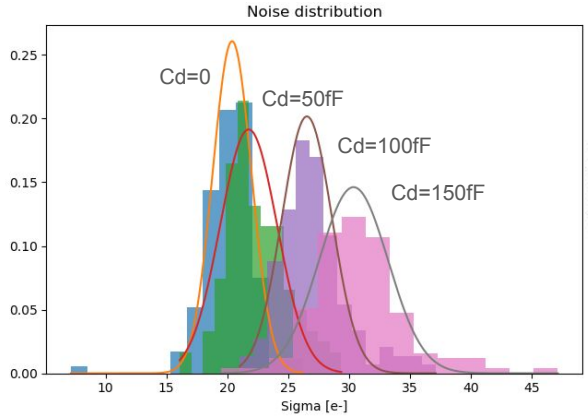
Pixel electrical test - noise performance

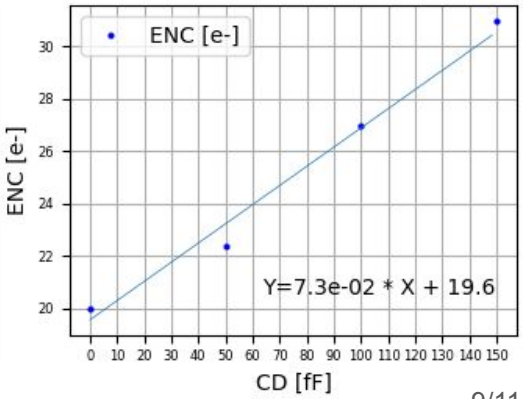




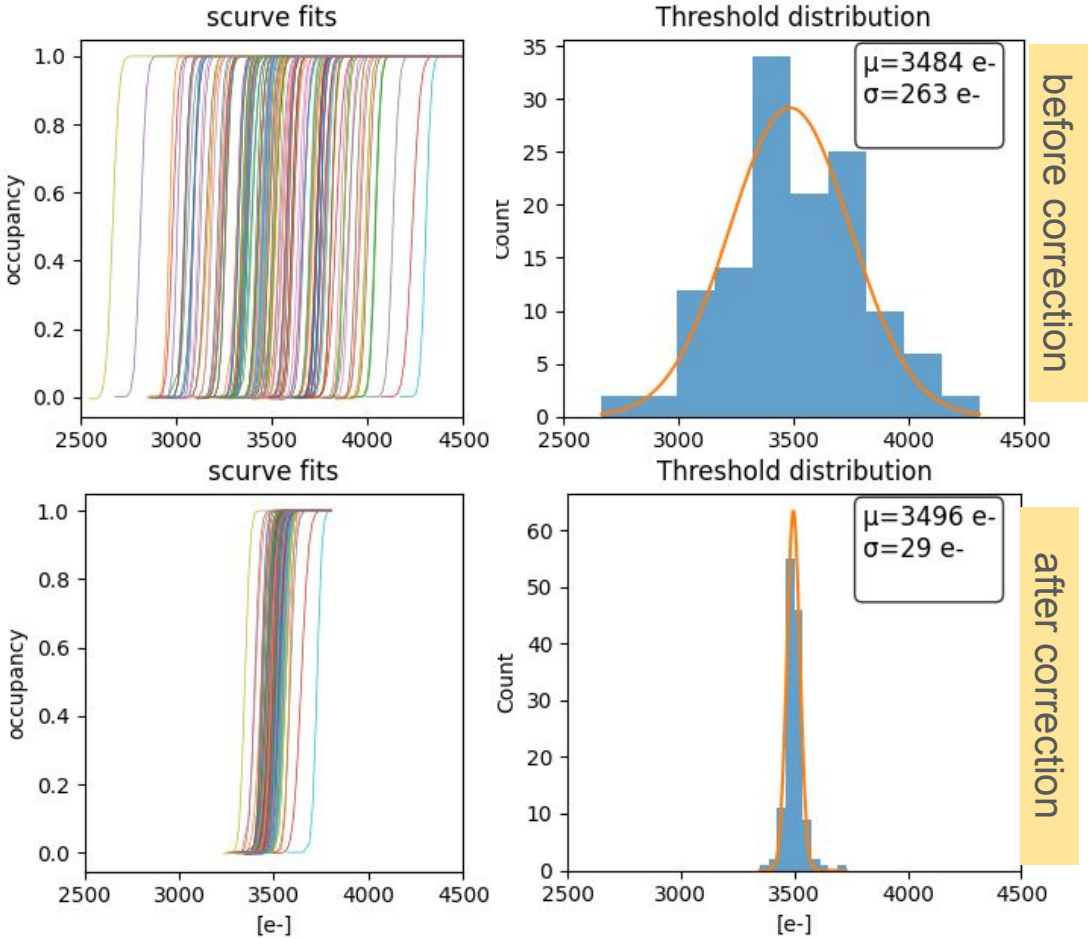
- (occupancy vs injected charge) s-curve analysis
  - provides per pixel estimation of electronics noise (ENC) and pixel effective threshold
  - performed on full matrix at 16 e^- step
  - performed at several values of the Cd (0 fF, 50 fF, 100fF, 150 fF)







Pixel electrical test - Threshold correction



- (occupancy vs injected charge) s-curve analysis
  - performed on full matrix at 16 e^- step
  - at local th DAC correction 0 to 30 with 2 LSB step
- reduces the threshold dispersion down to the pixel electronic noise level
  - can improve further exploiting the full DAC range (1 LSB step)

Conclusions

The ASIX R&D is developing a demonstrator for a new Hybrid Pixel Detector with 50 μm hexagonal pixels and a 300 μm-thick silicon sensor, targeting 10 μm spatial resolution and 300 eV FWHM energy resolution in the low energy X-ray regime.

To this end, we are developing a new readout ASIC combining ultra-low-noise analog performance with high digital integration.

A two-step ASIC development strategy has delivered a 65 nm CMOS prototype implementing a fully functional ASIX region, the basic building block for larger detector matrices.

The prototype successfully validated the ASIX architecture, demonstrating full functionality, excellent front-end noise performance and highly effective local threshold equalization.

The integration of the full-scale readout ASIC for the ASIX HPD demonstrator, approximately 6 × 5 mm², is currently ongoing

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Acknowledgment

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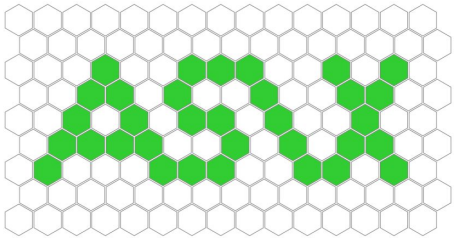

Thank you