Compact readout processor for x-ray science hybrid pixel detectors

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Challenges in frontier light sources

Offers:

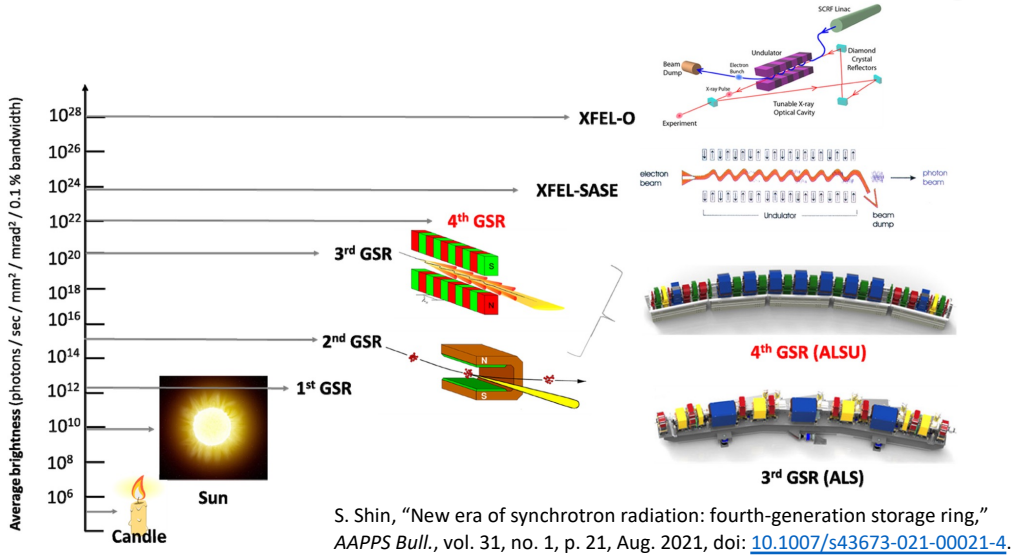
- **Higher brilliance**
- **New modulations** (i.e. continuous-wave light)

Asks:

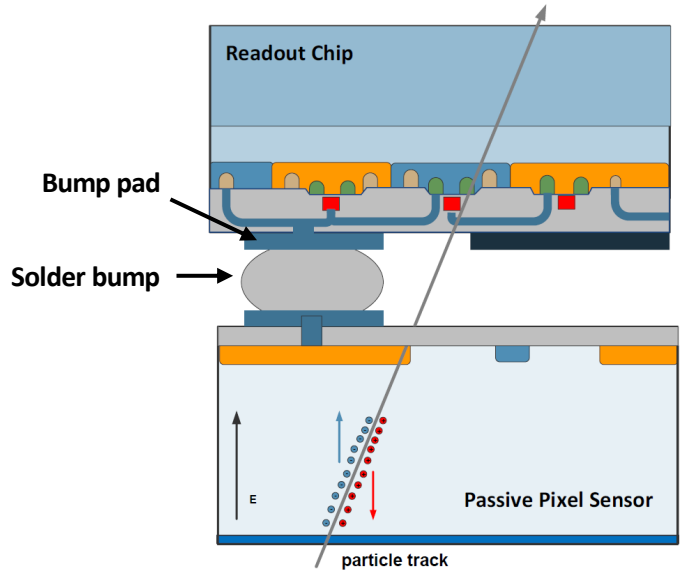
- **Nearly-zero readout dead-time**
- **Faster data acquisition** (higher bandwidth)
- **On-chip compression** strategies

Needs:

- **Modern detector concepts**
- **Compact readouts**
- **Easy ASIC calibration**



S. Shin, "New era of synchrotron radiation: fourth-generation storage ring," *AAPPS Bull.*, vol. 31, no. 1, p. 21, Aug. 2021, doi: 10.1007/s43673-021-00021-4.



T. Hemperek, "Advances in Pixel Detectors," *CERN presentation*, 2021

AlpRay project

- **Over-the-Alps collaboration** between DECTRIS AG Ltd. (Switzerland), UniBG, and UniPV (Italy)
- Development of a **compact readout processor** for applications at:
  - Fourth-generation synchrotrons
  - Free Electron Lasers (FELs)
  - Electron microscopes with pulsed electrons
- **Commercial 110 nm CMOS** technology node

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DECTRIS detecting the future

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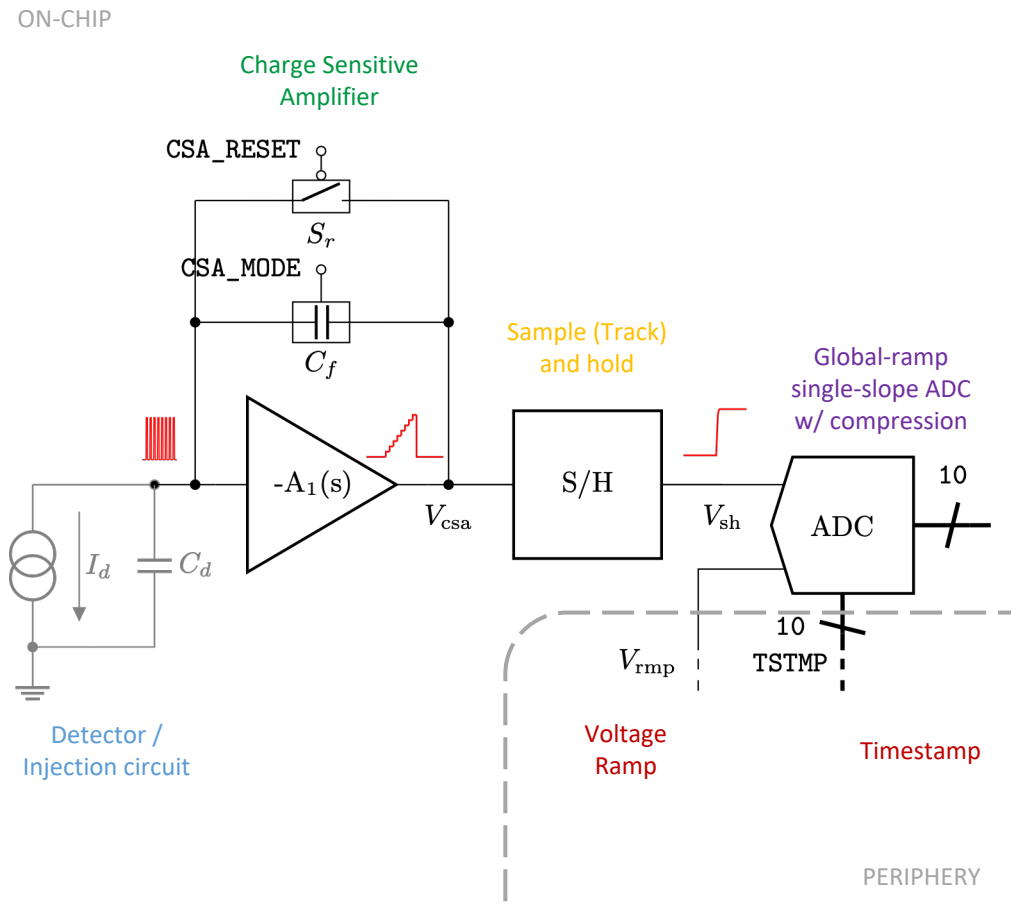
AlpRay readout channel



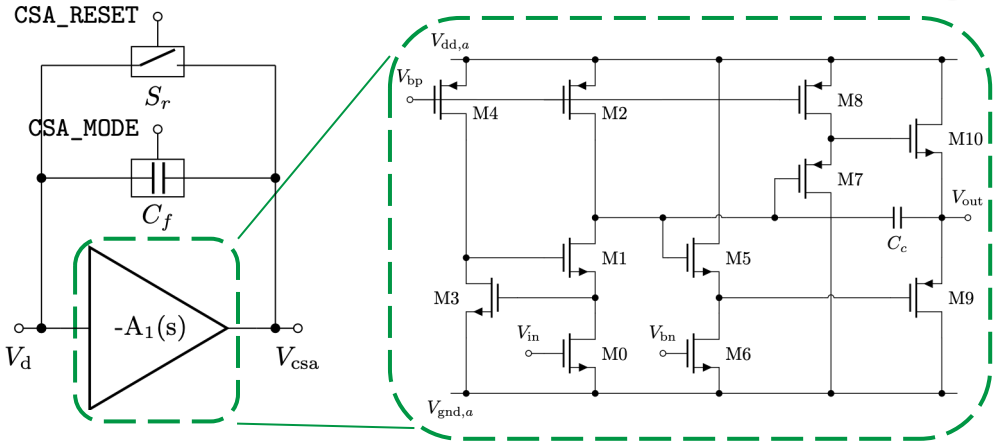
Features:

- **100 (or 1000) photons @ 8 keV**
- Signal polarity: electrons
- Signal-to-Noise Ratio: 14 (or 6)
  ENC: 155 e- rms (or 373 e- rms)
- **Single-photon resolution**
- **Compliant with continuous-waved and pulsed input**
- ADC resolution: 10 bits
- Readout rate **100 kframe/s** (scalable to 1 Mframe/s*)
- **Dead-time less or equal 1%**
- **Intrinsically pipelined:** CSA and ADC work together on different frames
- Pixel pitch 75 µm
- Target matrix 256 x 256 (20 x 20 mm^2)
- **Power density .5 W/cm^2**

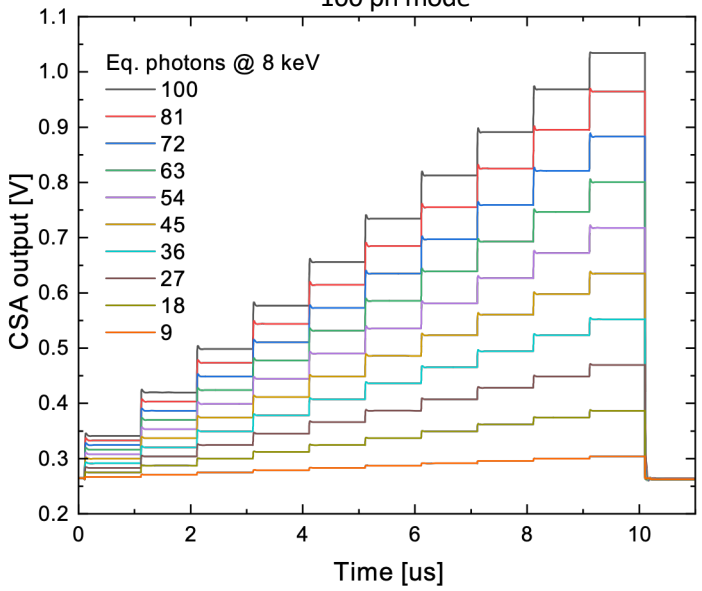
*Employing same architecture for a future iteration

Charge Sensitive Amplifier

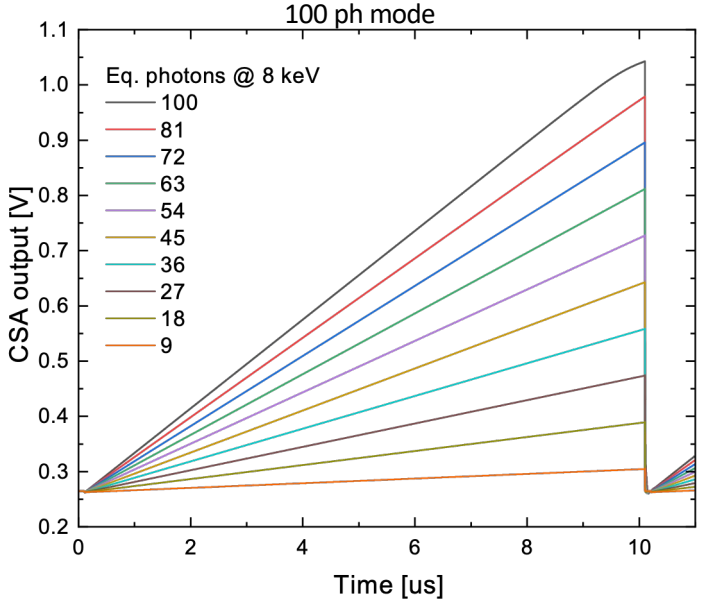
- Forward: Regulated feedback + push-pull source follower
- Type: Switch-reset CSA
- Input: **NMOS** (50 µm / 240 nm)
- Feedback cap: **44.8 fF** (or 448 fF)
- **INL: 0.49%**

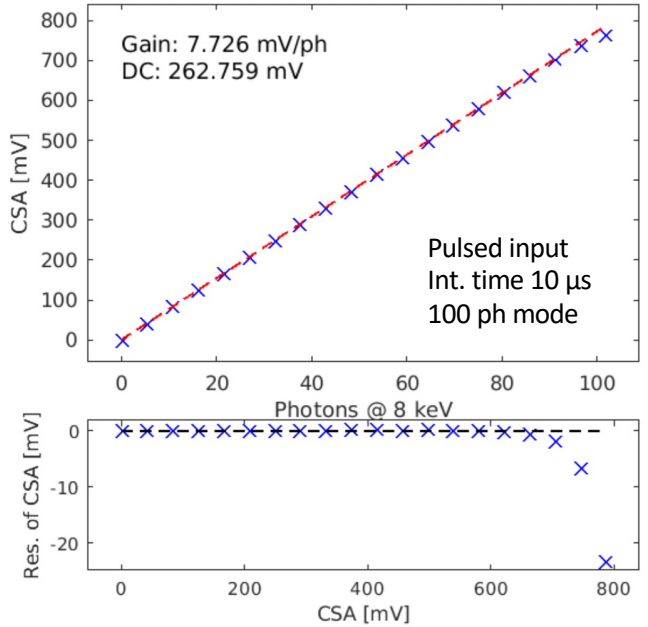


Pulsed input
Int. time 10 µs
100 ph mode



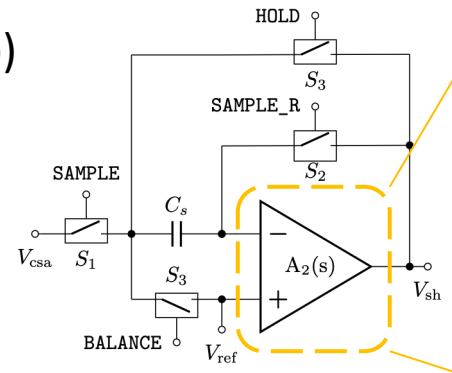
Continuous input
Int. time 10 µs
100 ph mode

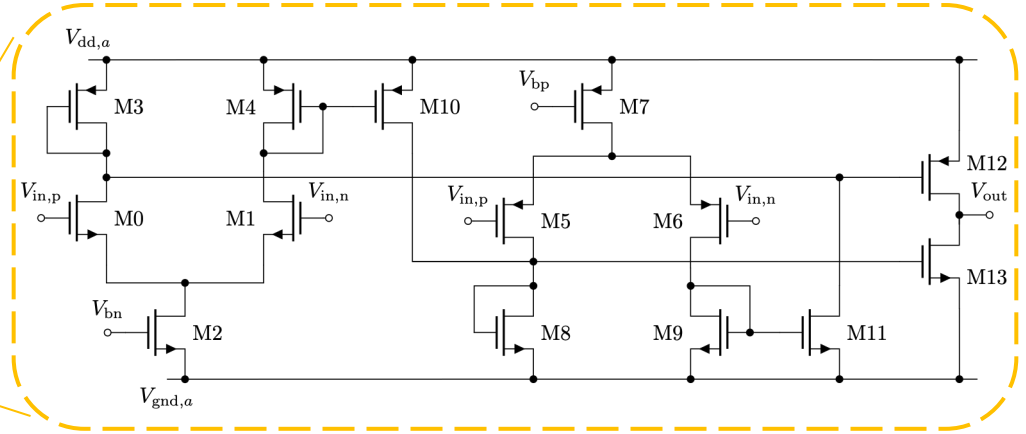




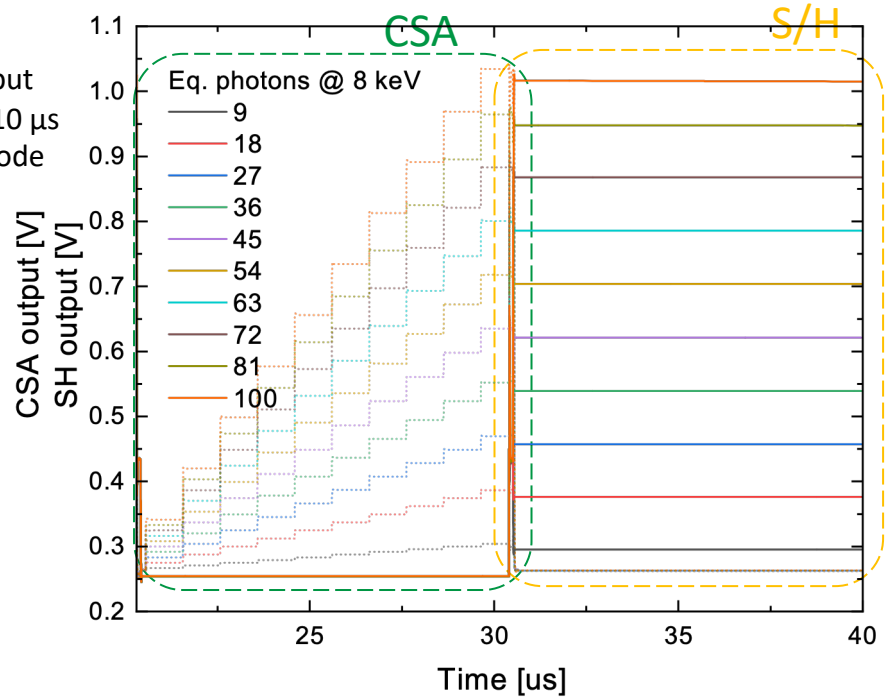
Sample and Hold

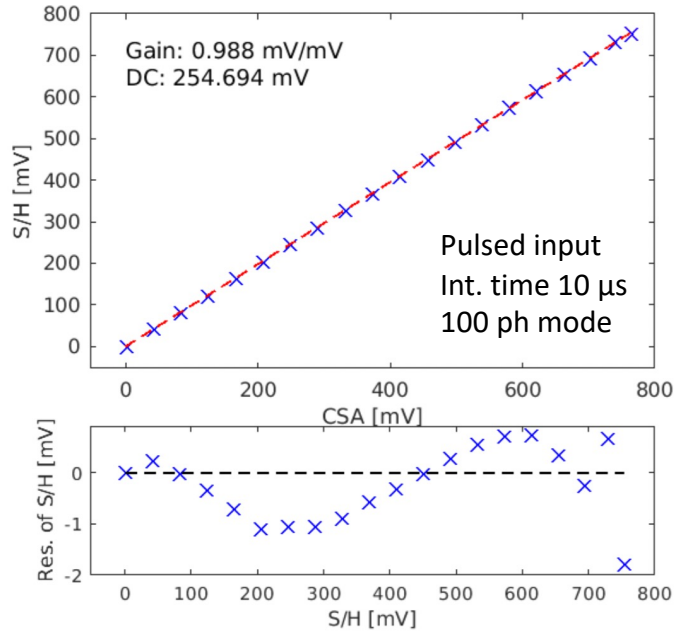
- Forward: Rail-to-rail input (dual diff amp) + push-pull gain output
- Type: Modified flip-around S/H
- Can be operated as a track and hold
- **Rise time: < 40 ns**



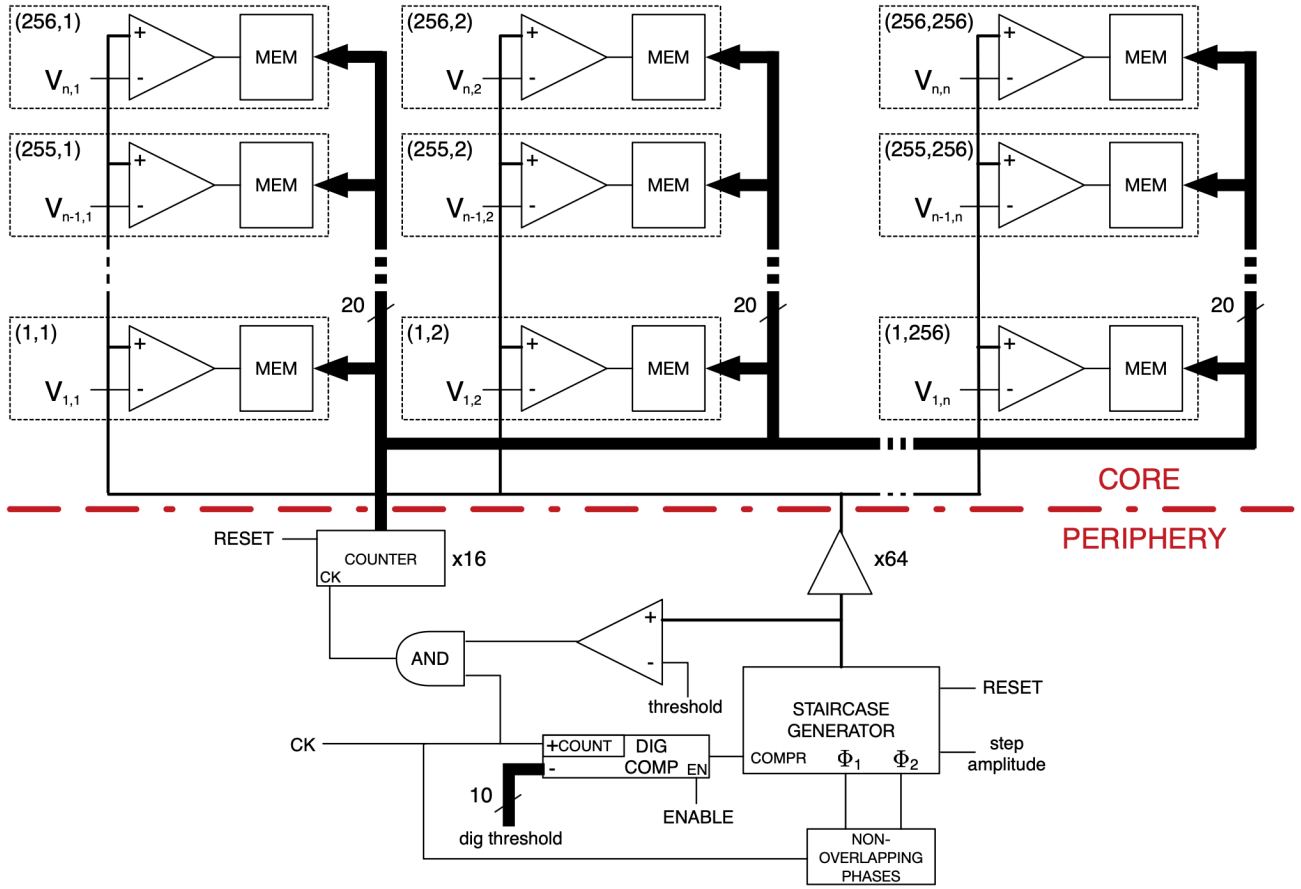


Pulsed input
Int. time 10 µs
100 ph mode





Global-ramp single slope ADC w/ compression



Periphery

- **Staircase generator** (SC integrator)
- **Analog buffers** (x 64)
- **Counters** (x16) **for Grey-code timestamp generation**

Per-pixel

- **Analog discriminator**
- **12T memory**

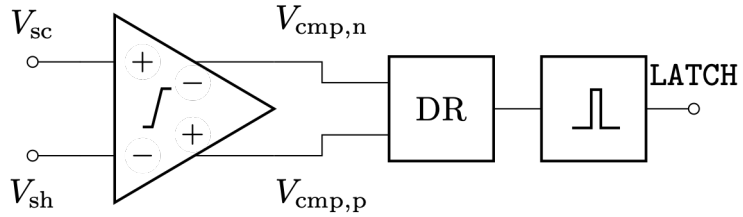
Features:

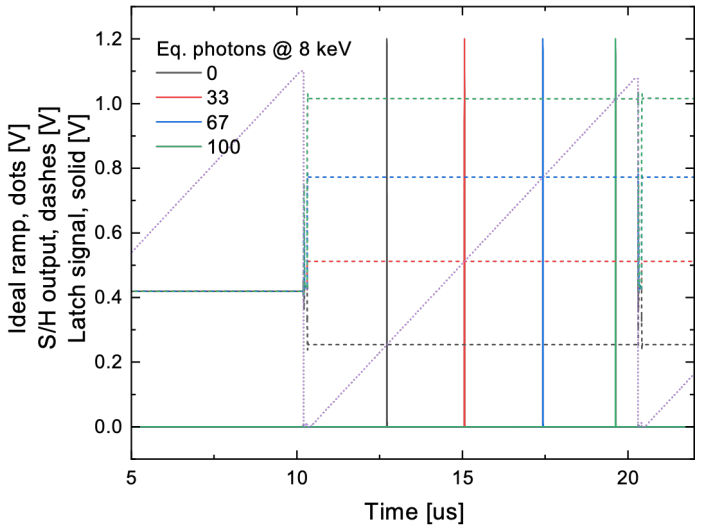
- Common clock (100 MHz)
  - → Intrinsically **insensitive to clock frequency drifts**
- **Compression** feature: Increase the staircase slope as the count increases
  - → Faster conversion, with worse resolution
  - → **No loss in conversion accuracy (relies on Possion noise)**

Other ADC in-pixel blocks

Discriminator

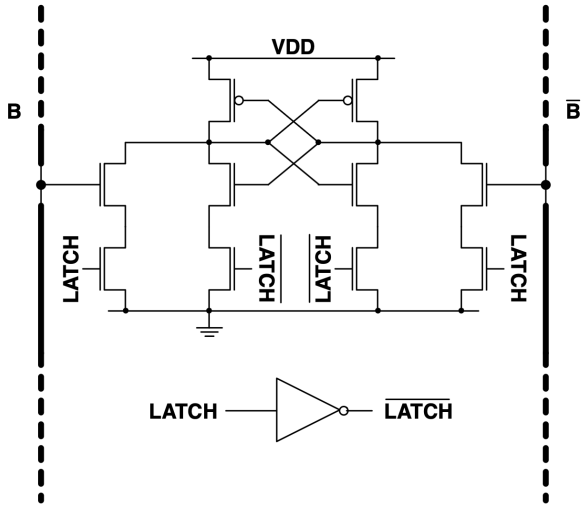
- Architecture: double differential amplifier + regeneration circuit + monostable circuit
- Design criteria: < 10 ns latching delay





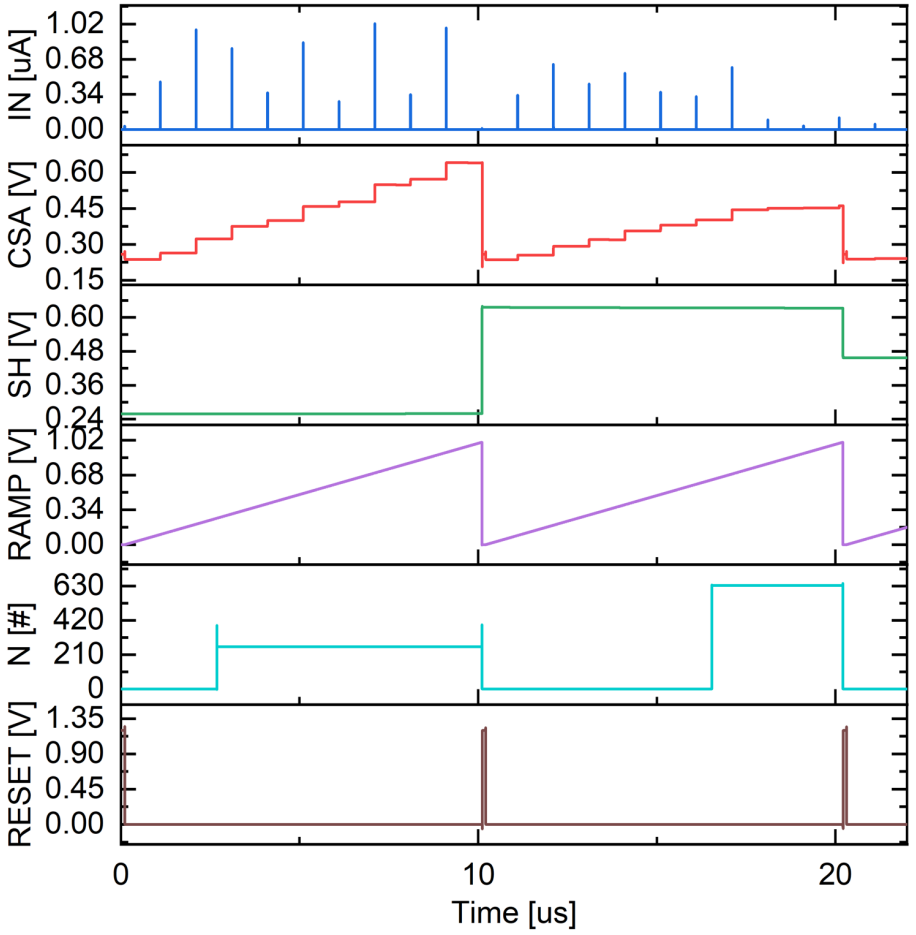
Memory cell

- Architecture: 12T memory cell
- Not the best in terms of area but most area-efficient:
  - Multi-cell programming (high impedance to column drivers)
  - If ELTs are employed (such as in this scenario)



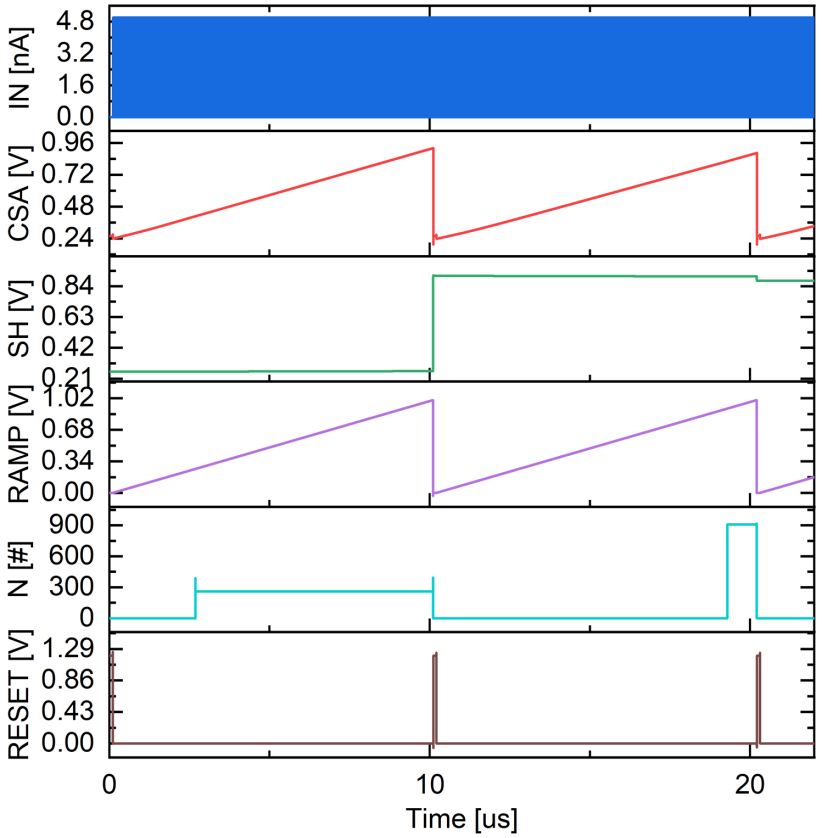
Channel working principle

- **CSA integrates** the input pulses over **an integration time** (= 10 µs)
- **S/H samples the CSA level** at the end of the integration time, before CSA is reset
- **The global staircase and the S/H level are compared** by the discriminator, which generates a **latch** signal (not reported)
- **The latch signal stores the timestamp value inside the memory** cell, per pixel
- A reset signal is employed to reset the CSA to baseline
- While the k-th frame is being processed, the channel is converting the current pulses of the (k+1)-th frame, which makes it **intrinsically pipelined**.

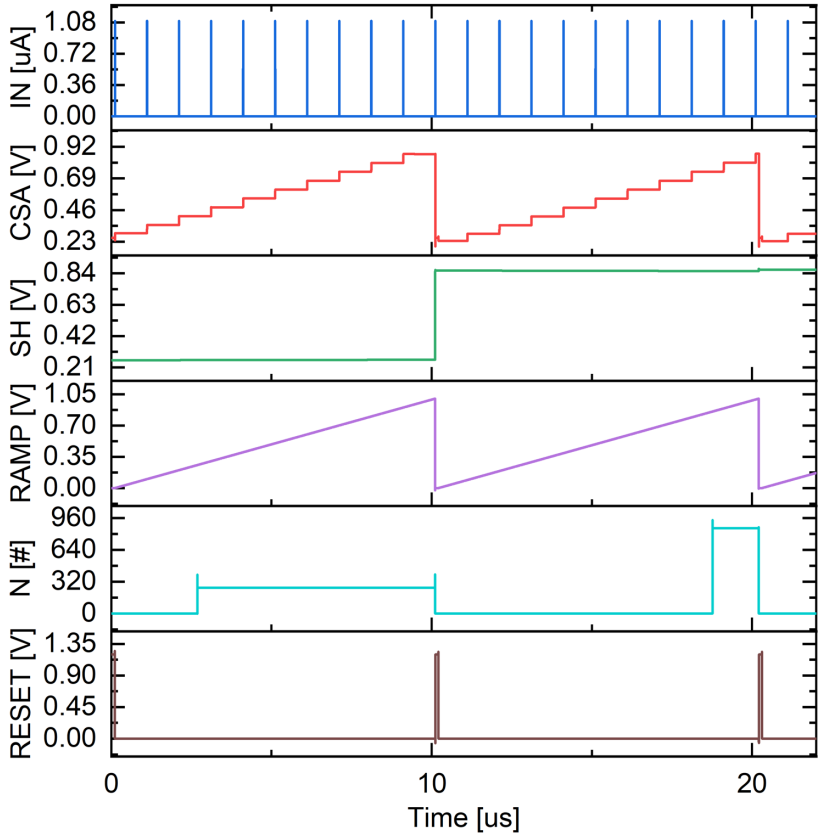


Channel transients in different operation modes

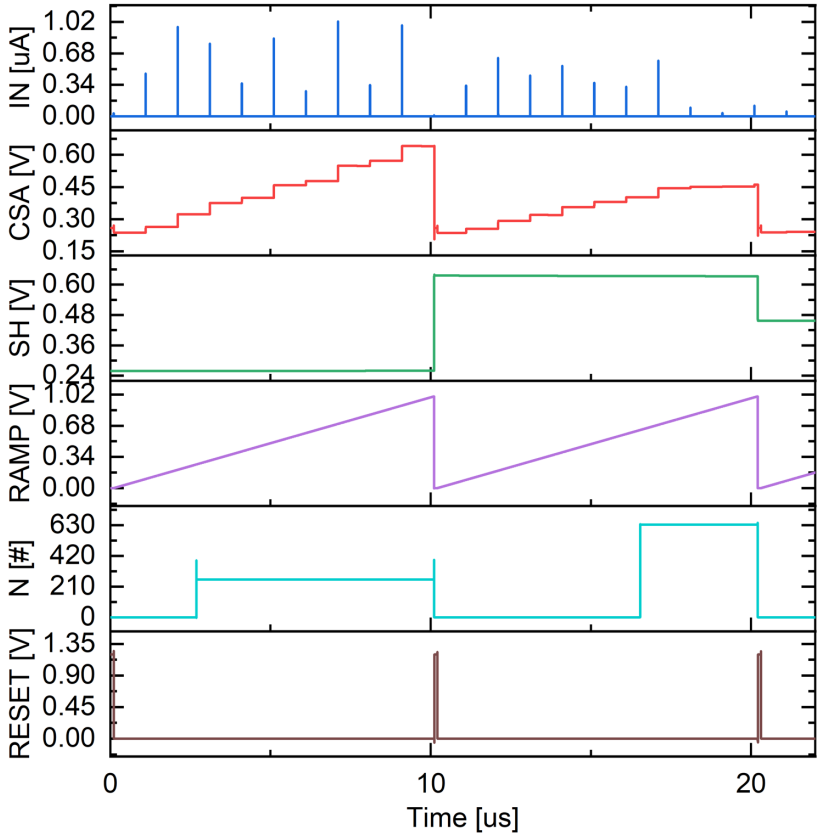
Continuous mode



Pulsed mode

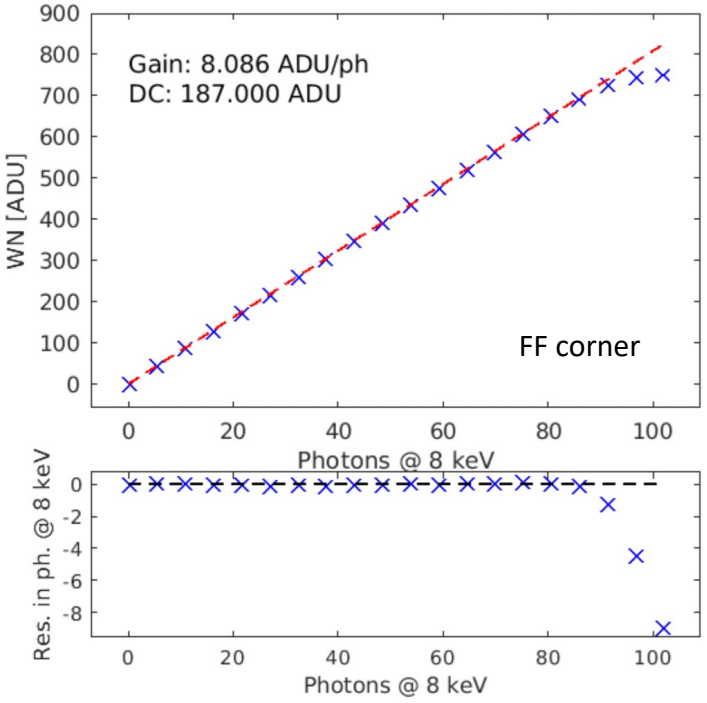


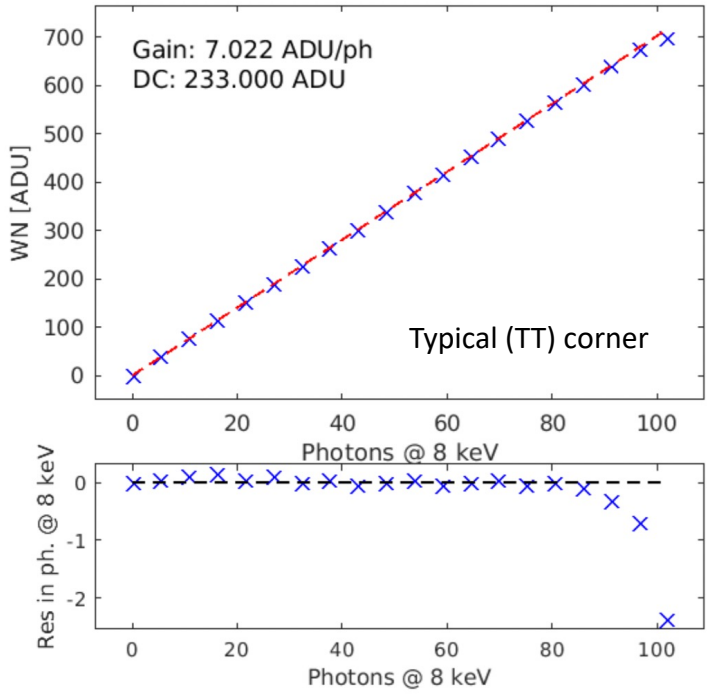
Pulsed mode (rnd)

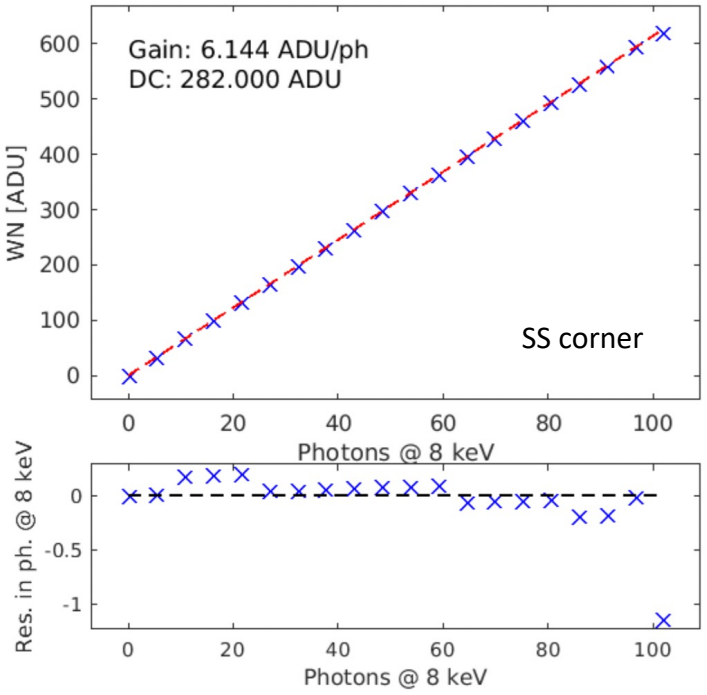


Channel I/O in corners

Pulsed input, integration time 10 µs, and employing 100 photons mode, w/ ideally-generated global ramp







- Channel shows a good response overall.
- FF corner is the least linear, but it is however up to the requirements.

Conclusions and future steps

- A **compact readout channel has been developed in a commercial 110 um CMOS technology**
- The architecture has been **simulated and verified** in **corner** simulations and through **Monte Carlo** simulations, taking also into account **IR drop** and other effects.
- Integration between the developed readout channel and DECTRIS IPs and digital back-end is expected by Q4 2026.
- An engineering run is expected by Q2 2027. It will include a fully-populated 256x256 matrix with some test structures to characterize individual blocks.

Thank you for your kind attention!
Q&A

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Backup slides

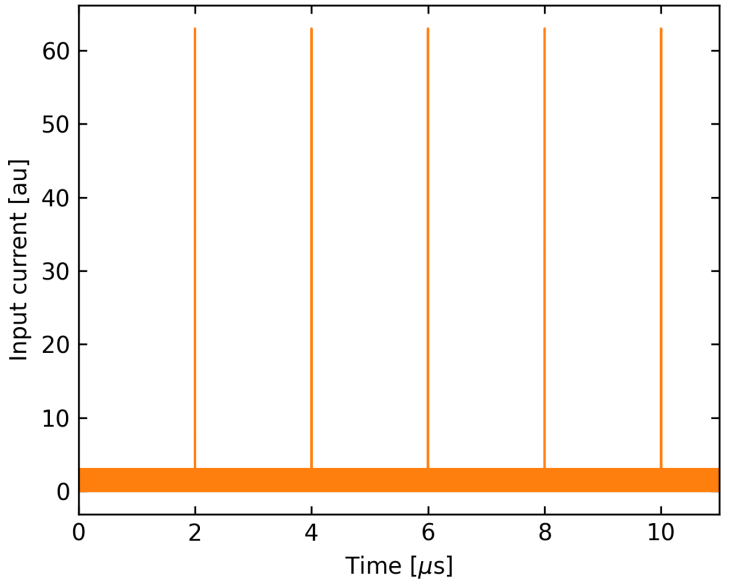
International Workshop
27th iWoRiD
on Radiation Imaging Detectors

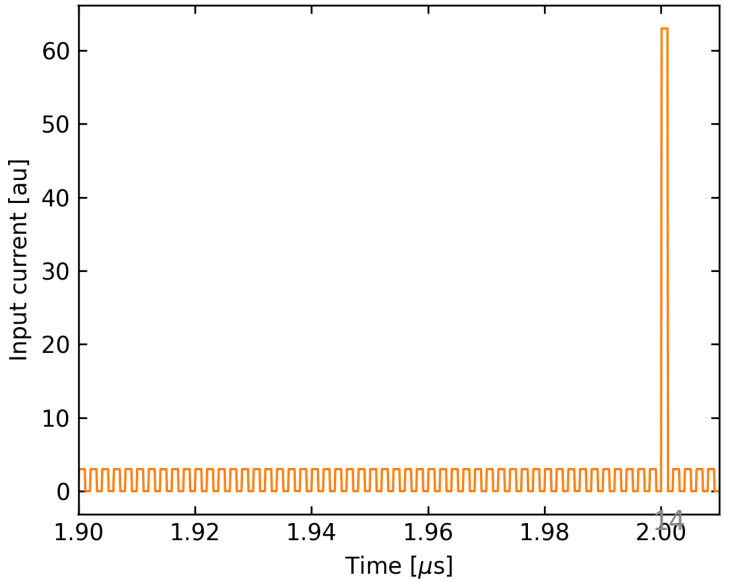
Expected synchrotron signal

- The signal from the synchrotron is modelled as the superposition of:
  - A train of continuous trapezoidal pulses with period $T_c = 2$ ns and low amplitude (few photons, 1 to 3 ph).
  - A periodic pulsed trapezoidal signal pulses with period $T_p = 2$ us and higher amplitude (50 to 70 photons).
- With a target frame rate of 100 kHz and a dead time around 1% (let's say 10 us overall), this results in

$$\#photons = \frac{10\ us}{2\ ns} \cdot 3\ ph + \frac{10\ us}{2\ us} \cdot 60\ ph = 15000 + 300 = 15300\ ph$$

- One expects this is diffracted by the target and the single pixel gets less than this amount of photons, up to a maximum of 100 to 200 photons.
- So how to model the input signal?





CSA corners

FoM	Min	Max	Worst
Gain [mV/ph, AC (T)]	6.7	8.7	SS (cap fb)
INL [%]	.07%	1.68%	SF
Fwd gain [dB]	49	53	FS
Noise [e- rms, AC (TN)]	28 (147)	42 (160)	SS
Phase Margin	69° @ 137 MHz	83° @ 121 MHz	SF
Dynamic range [mV]	693	866	SS (cap fb)
Offset [mV]	-50 mV	+50 mV	FF, SS
Comments	--		

S/H corners

FoM	Min	Max	Worst
Gain [V/V]	About 1	About 1	FF, FS
INL [%]	0.46%	1.91%	FF
Fwd gain [dB]	42	43	FF, FS
Phase Margin [loop]	48° @ 38 MHz	48° @ 41 MHz	SS
Dynamic range [mV]	693	866	SS (cap fb)
Offset CSA vs S/H [mV]	0 ph: 8 mV 100 ph: 13 mV	0 ph: 15 mV 100 ph: 30 mV	0 ph: FS 100 ph: FF
Comments	FS is a little non-monotonic at the beginning		