

16-channel amplifier for thin Low Gain Avalanche Diodes based on the FAST3 ASIC

FAST3-Amplifier

Project update

Marco Ferrero (INFN Torino)

On behalf the INFN Torino

Work performed in the framework of DRD3



The project proposal

The goal: development, design and production of a 16-channel amplifier, optimized for LGADs of thickness $\sim 50 \mu\text{m}$ and small capacitance ($\sim \text{ps}$), based on the FAST3 ASIC (analog version) package.

Main activities:

1. Design and production of FAST3 packaging
2. Design and production of the ASIC read-out board, with assembly of the packaged ASIC
3. Debug and optimization of the working condition of the 16-ch amplifier

RD50 funding request
- Date: 18.12.2023 -

Title of project: 16-channel amplifier for thin Low Gain Avalanche Diodes based on the FAST3 ASIC – FAST3-Amplifier

Contact person: M. Ferrero
INFN Torino
+39 011 670 7338
marco.ferrero@to.infn.it

Involved institutes:

1. INFN Torino, M. Ferrero – marco.ferrero@to.infn.it Supervisor of activities
2. UC Santa Cruz, V. Fadeyev - fadeyev@ucsc.edu
3. CERN, D. Dannheim - dominik.dannheim@cern.ch
4. Jozef Stefan Institute, G. Kramberger - Gregor.Kramberger@ijs.si
5. HEPHY, T. Bergauer - Thomas.Bergauer@oeaw.ac.at
6. TU Dortmund, J. Weingarten - jens.weingarten@cern.ch
7. KIT, A. Dierlamm - alexander.dierlamm@kit.edu
8. Prague Academy, P. Svihra - peter.svihra@cern.ch

Total project cost: € 44,400
Request to RD50: € 22,200

The project proposal

- **8 Institutes expressed interest in the project**
- A total of 35 amplifiers requested
- **INFN Torino provided FAST3 ASICs** necessary for the production of the preamplifier

Institute	Contact
<i>INFN Torino</i>	<i>M. Ferrero</i>
<i>UC Santa Cruz</i>	<i>V. Fadeyev</i>
<i>CERN</i>	<i>D. Dannheim</i>
<i>Jozef Stefan Institute</i>	<i>G. Kramberger</i>
<i>HEPHY</i>	<i>T. Bergauer</i>
<i>TU Dortmund</i>	<i>J. Weingarten</i>
<i>KIT</i>	<i>A. Dierlamm</i>
<i>Prague Academy</i>	<i>P. Svihra</i>

Production of the amplifiers in 2 batches:

- **1st batch (10 amplifiers)**
 - We received the 8 of the 10 board the last week of October (2 boards are on hold to complete the assembly)
 - We will use the first batch to check right operativity of the amplifier
- **2nd batch (remaining amplifier):** It will be procured at the end of the test of the first batch

Project more in detail

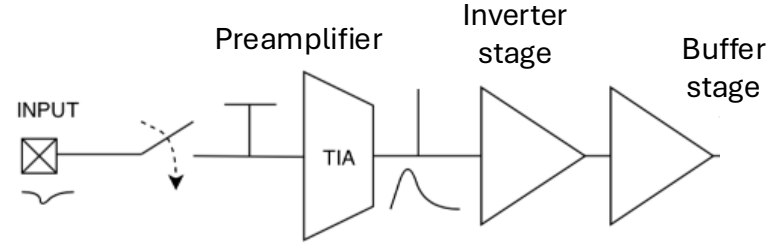
❖ FAST3 ASIC

❖ FAST3 Packaging

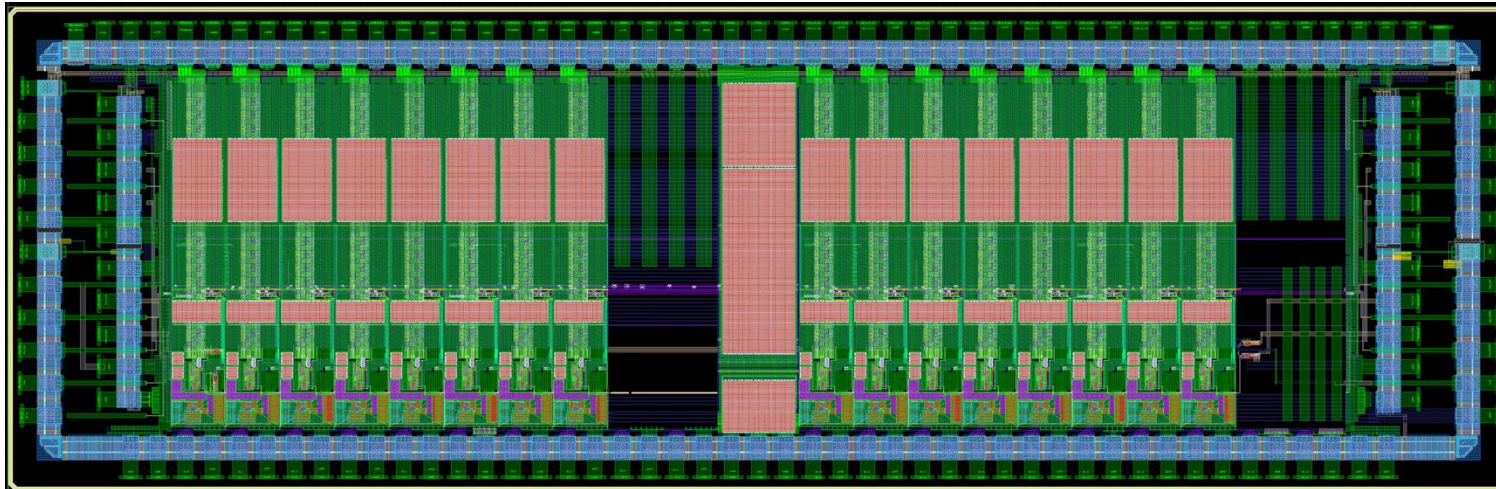
❖ Readout board

FAST3 prototype: Layout and specification

FAST3 Amplifier-only architecture (Analog version)



5 mm



- Bottom side: Input pad
- Top side: Output pad
- Lateral sides: Bias and Power input

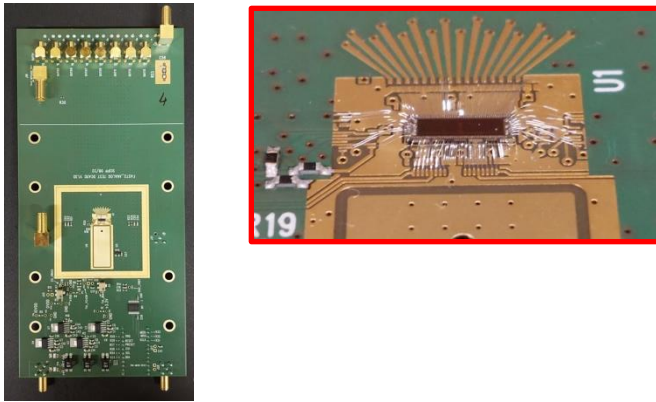
Table of specifications

Power rail	1.2 V
Number of Ch	16
Power consumption	2.3 + 7.7 mW/ch
Input dynamic range	3-40 fC
RMS Noise	1.1 mV
Output signal (@ 8 fC)	102 mV
SNR (@ 8 fC)	93
Voltage output range	~ 800 mV
Bandwidth	~ 1 GHz
Temporal Jitter (@ 8 fC)	20 ps
Programmable gain	8 different gains

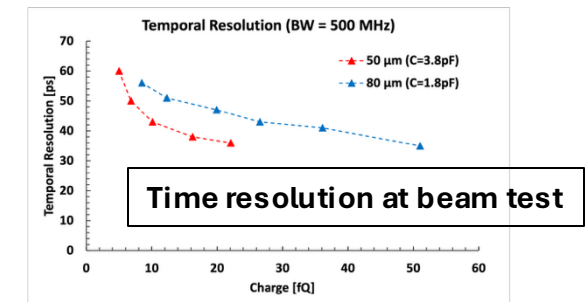
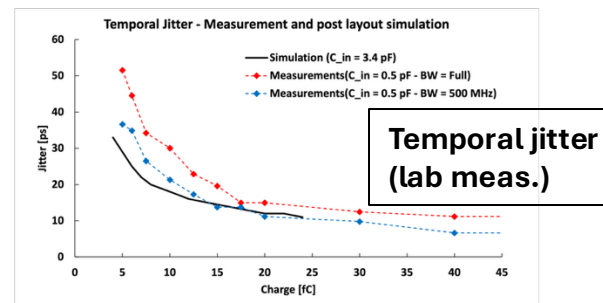
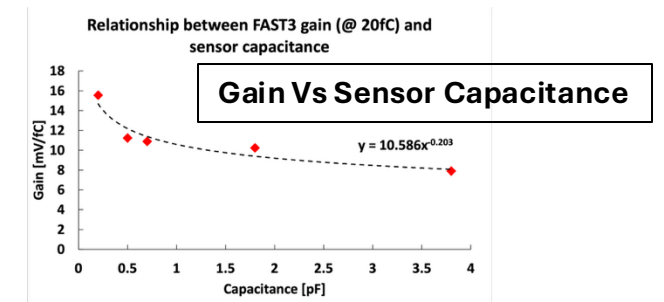
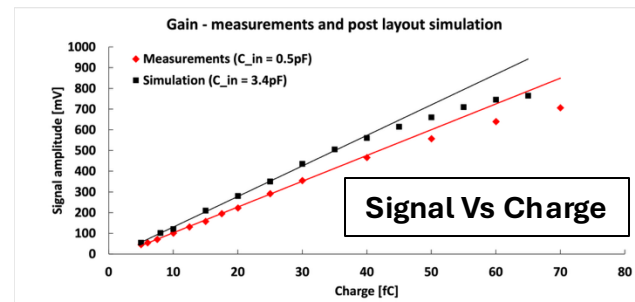
The main performance of the ASIC FAST3

All these results were obtained using a preliminary readout board adapted to FAST3 and with unpackaged ASICs.

Preliminary board developed for FAST2 and adapted to FAST3



Main results and performance obtained during the characterization of FAST3 in Laboratory and at Beam



References with scientific results:

- FAST3 ASIC: an analog front-end with 30 ps resolution, designed to readout thin Low Gain Avalanche Diodes, M. Ferrero *et al* 2025 *JINST* 20 C03007, 10.1088/1748-0221/20/03/C03007
- [M. Ferrero at TWEPP 2024](#)
- [M. Ferrero at TREDI 2024](#)
- FAST3: Front-End Electronics to Read Out Thin Ultra-Fast Silicon Detectors for ps Resolution, AM. Rojas, et al., J. 2022 IEEE Latin American Electron Devices Conference (LAEDC), 2022, 10.1109/LAEDC54796.2022.9908192

Project more in detail

❖ FAST3 ASIC

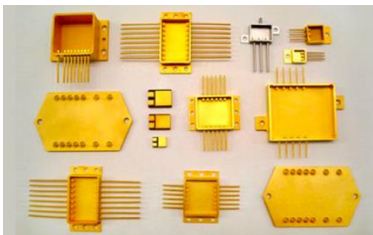
❖ FAST3 Packaging

❖ Readout board

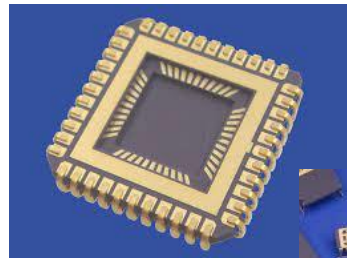
FAST3 Package - market survey and feasibility study

- The feasibility study of the package was conducted by [Electronica SRL](#) Company.
- Different commercial packaging options have been explored
 - Standard Metal, Ceramic and Plastic open cavity package (low compatibility with FAST3 Pinout and middle/large dimension)
 - Custom package (Very high cost)
 - MCM (Multi-Chip Module) package (low cost, full compatibility with ASIC pinout and small size)
- **Custom MCM has been chosen as packaging technology**
 - Connection technology with readout board: Ball Grid Array (BGA)
 - Easy mounting on readout board (**can be handled like an SMD component**)

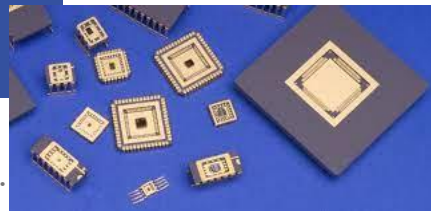
Metal package



13/11/2025

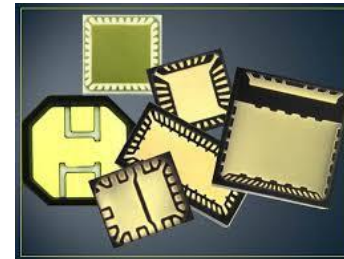


Ceramic package



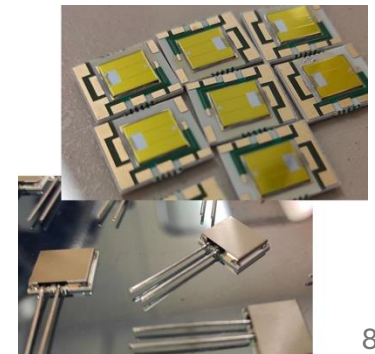
M.

Plastic open cavity



d State Detectors R&D

MCM

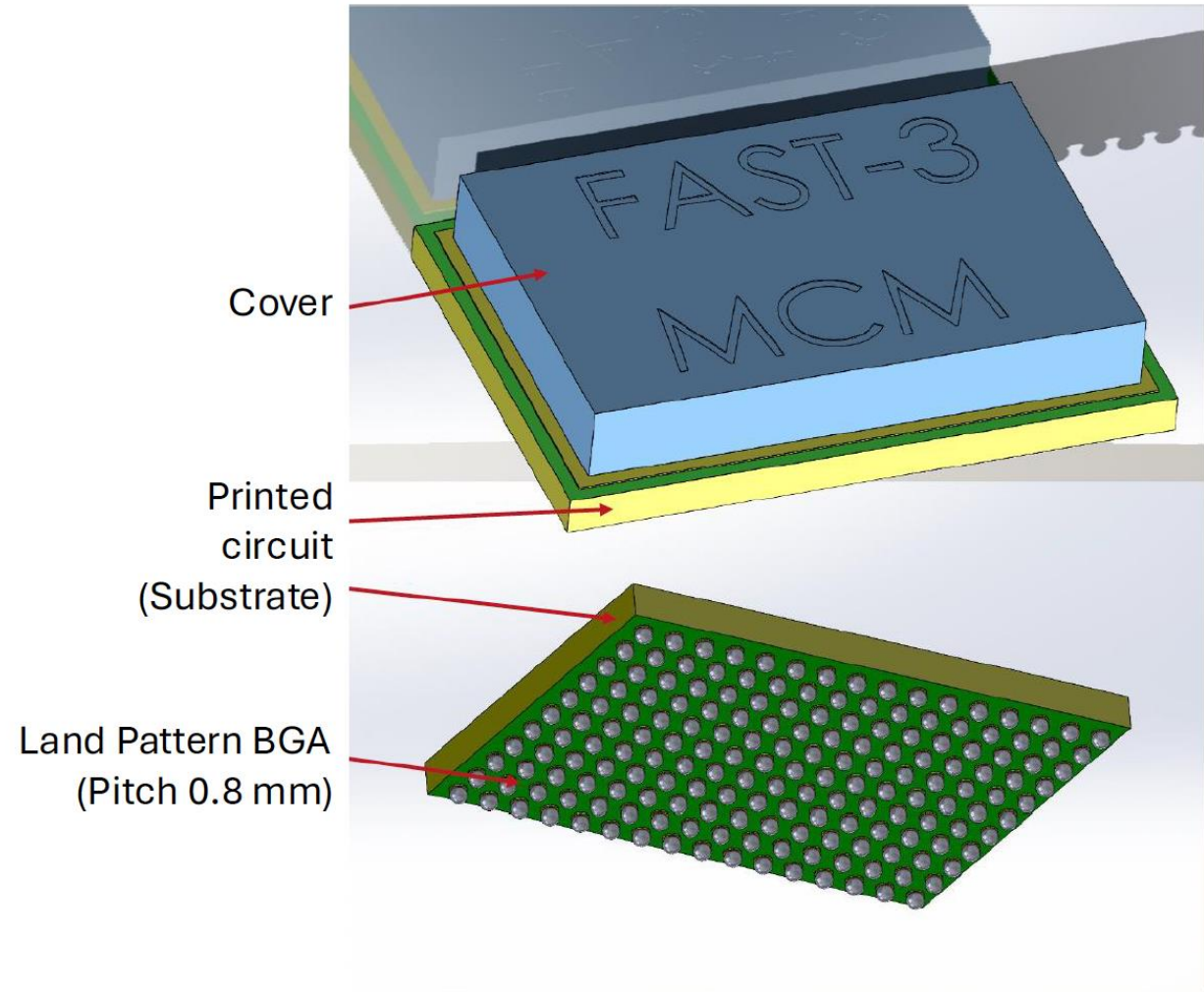
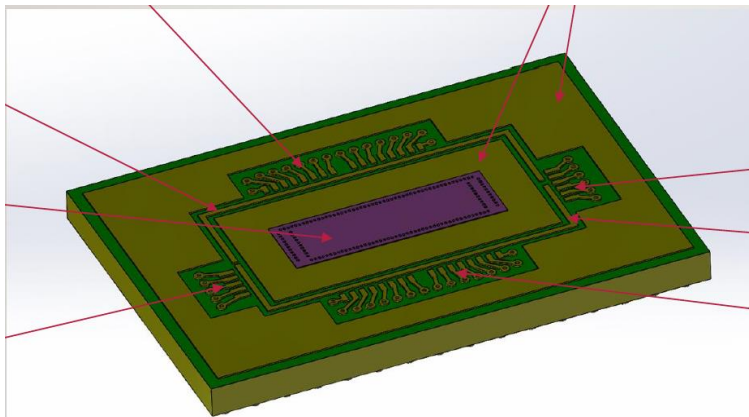


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FAST3 Package - MCM

Characteristics of the MCM package:

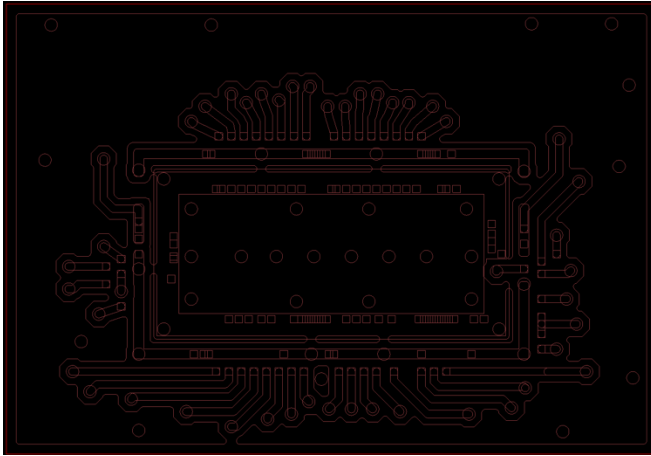
- FAST3 glued and wire-bonded on a printed circuit substrate of dimension $\sim 9 \times 13 \times 0.6$ mm
- Pinout technology: Ball Grid Array (BGA) pitch: 0.8 mm
- Metal cover for EM shielding



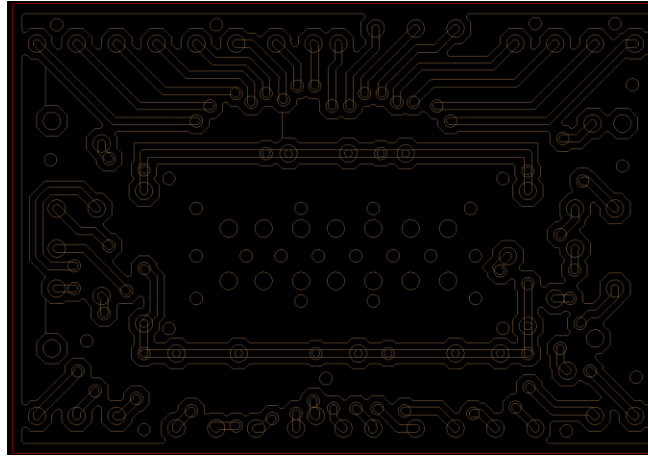
FAST3 Package – MCM Design

N. of layers of the MCM: 6

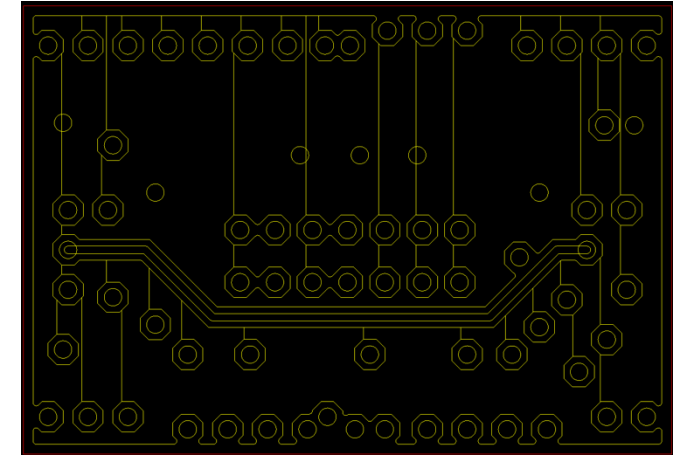
Top Layer: wire-bond layer



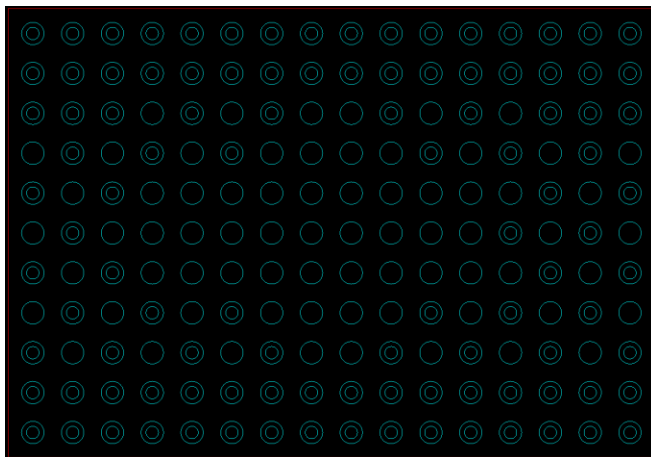
Inner 1: GND plane



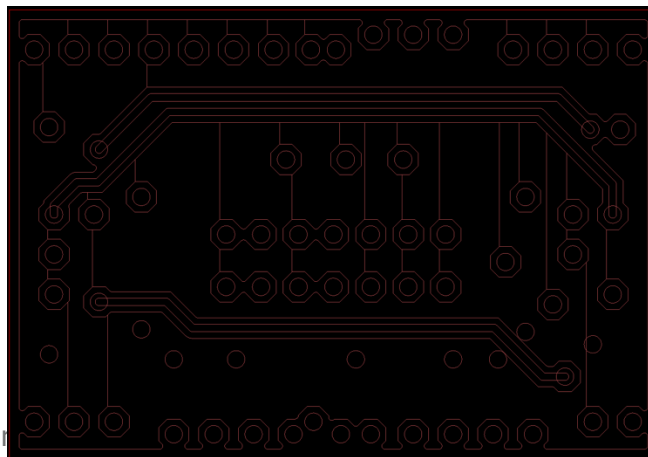
Inner 3: IOVDD plane



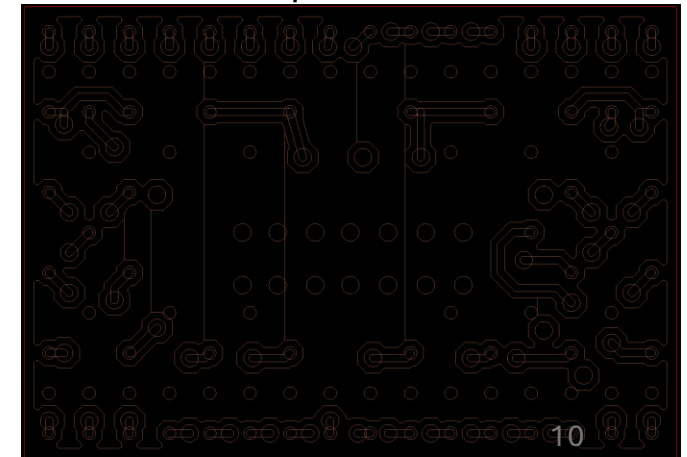
Bottom layer: BGA layer with 176
(105 used; 71 not used and grounded)



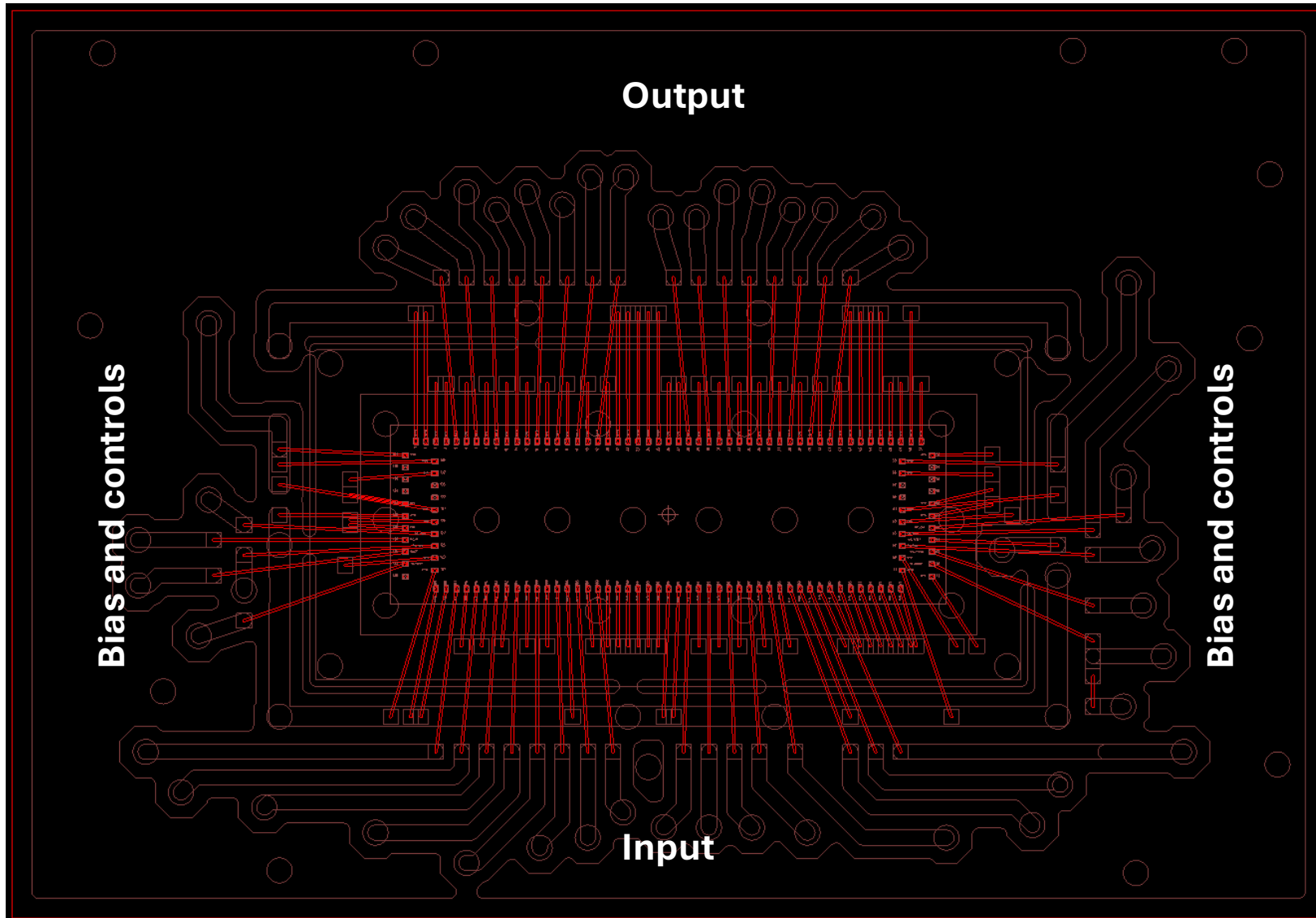
Inner 2: AVDD Plane



Inner 4: GND plane



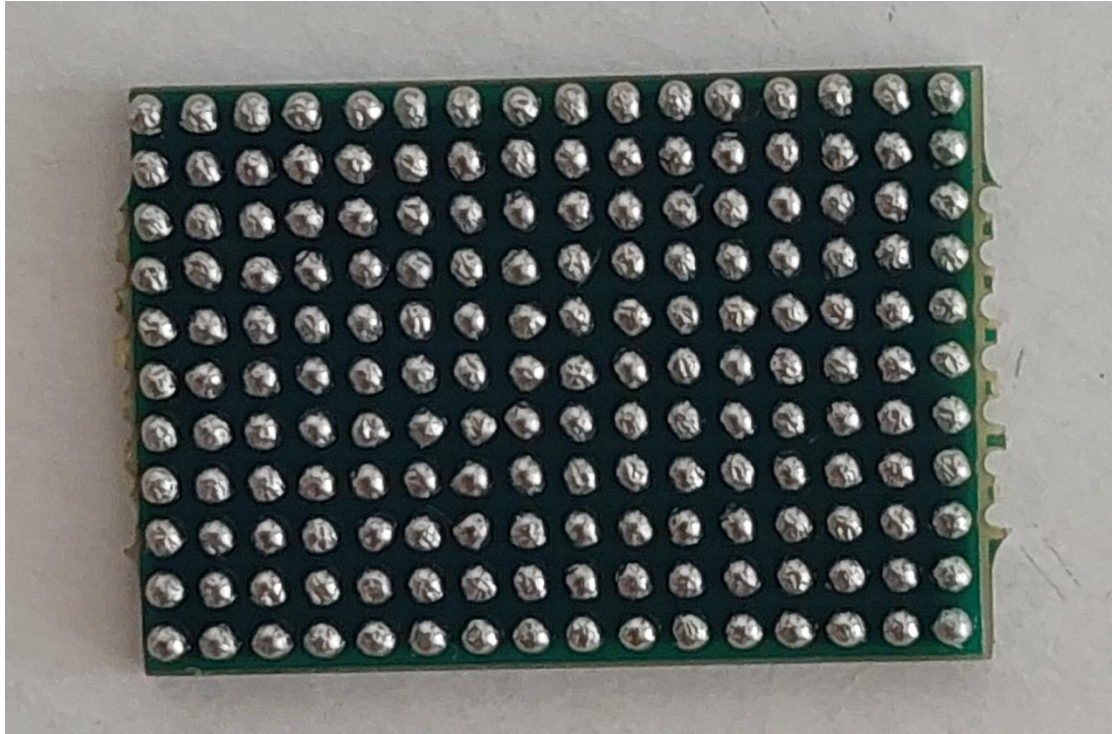
FAST3 Package – Bonding scheme



- 128 bonds
- Max bond length ~ 1.7 mm
- Two layer of bond on left and right side

FAST3 Package – BGA connection technology

Mechanical test of balls positioning on the back side of the MCM PCB



The balls have been positioned using a mask.

The company produced several masks to find the optimal one

Project more in detail

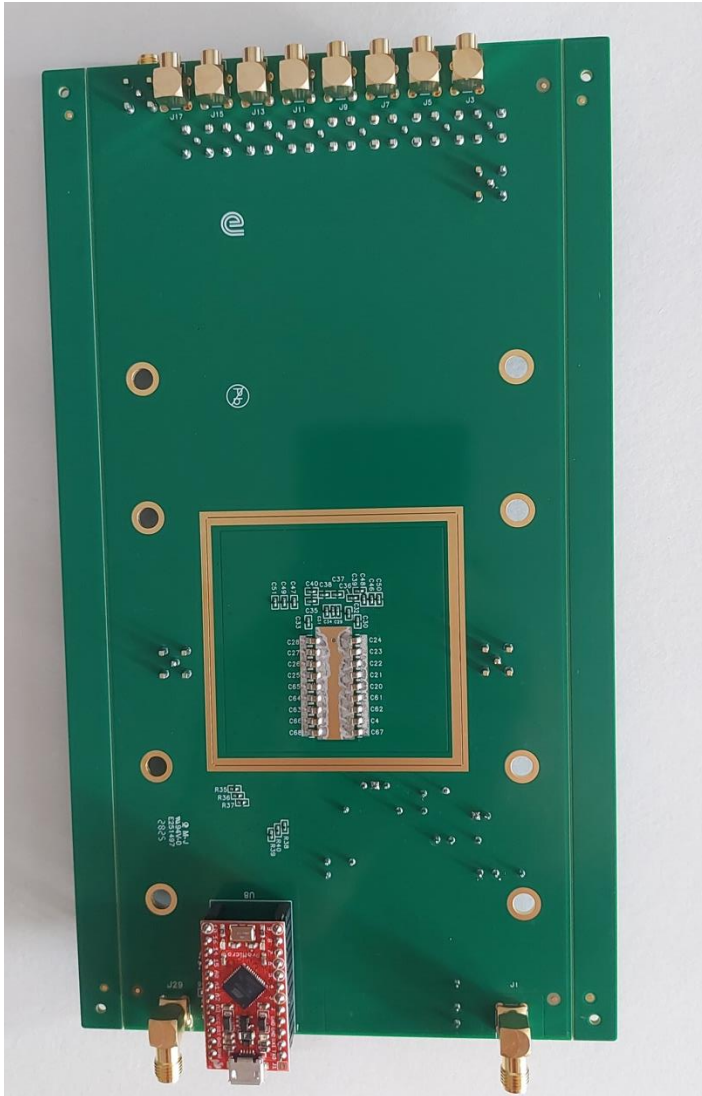
❖ FAST3 ASIC

❖ FAST3 Packaging

❖ Readout board

Readout board

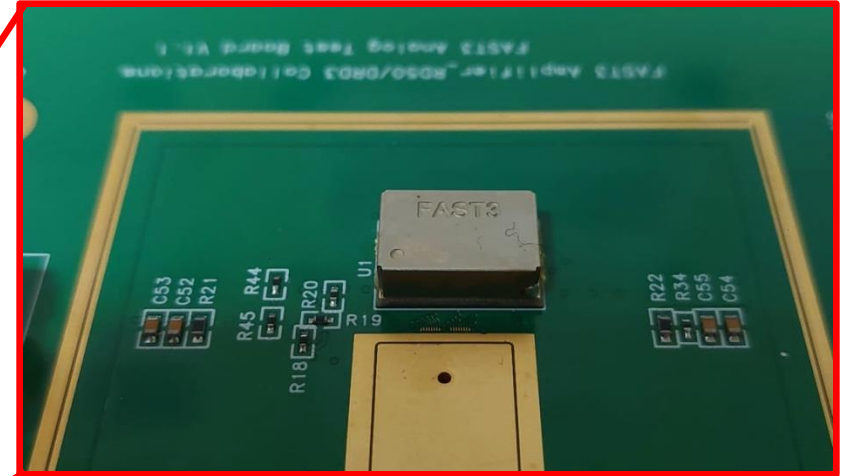
Bottom side



Top side

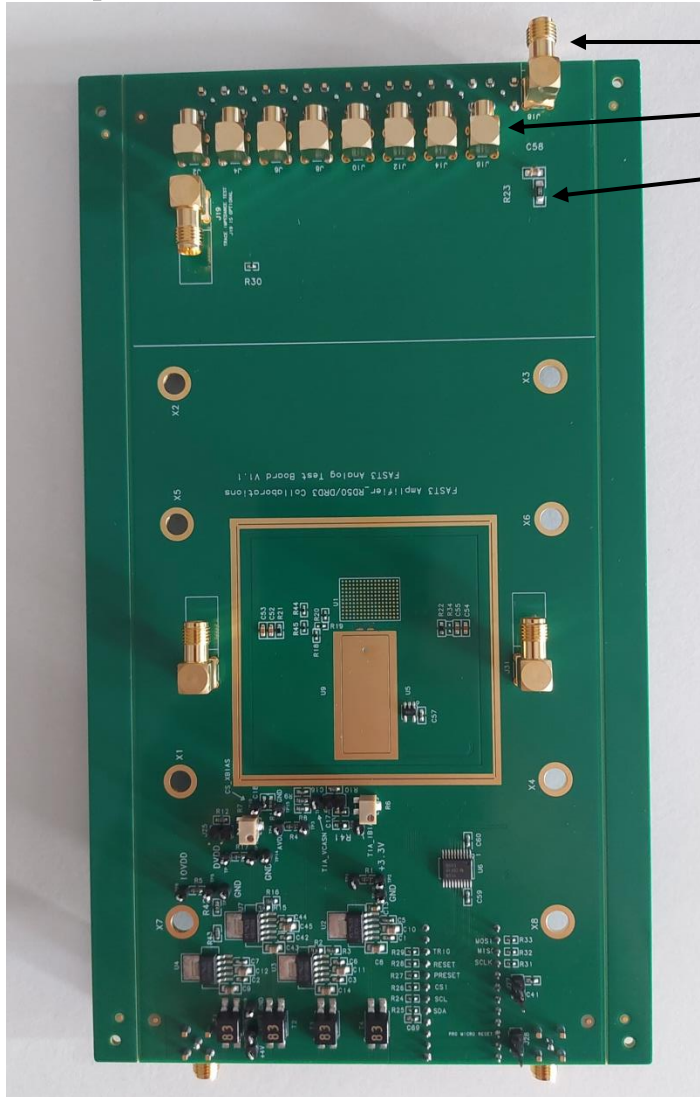


MCM welded on board



Readout board

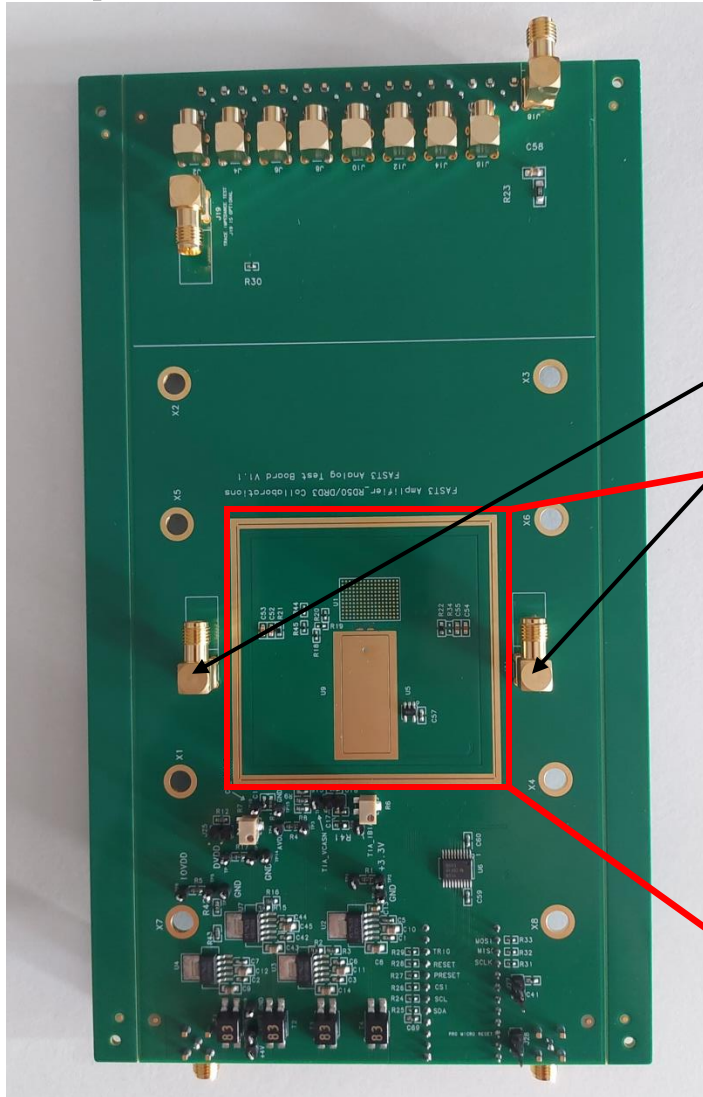
Top side



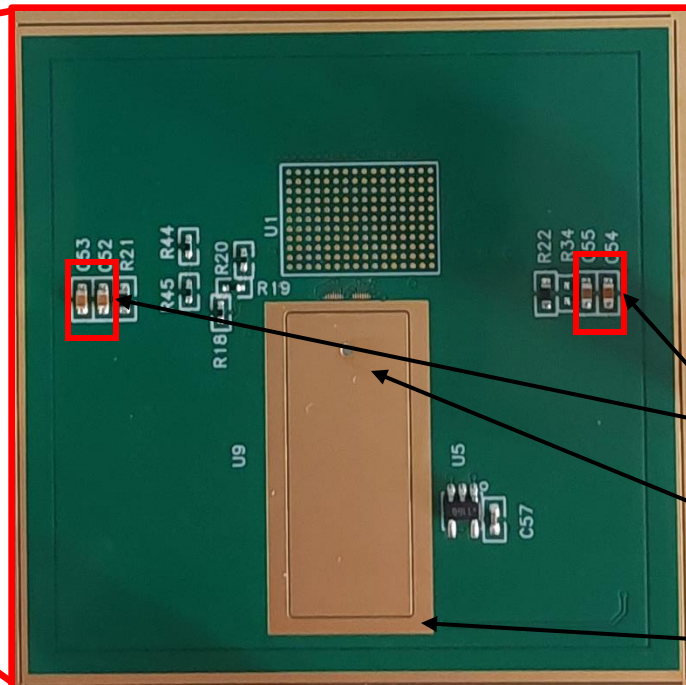
- SMA High Voltage connector
- MCX output connectors (8 for each side of the board)
- 10 kΩ resistor along the HV line

Readout board

Top side



- SMA High Voltage connector
- MCX output connectors (8 for each side of the board)
- 10 k Ω resistor along the HV line
- HV plate ~ 1 cm x 2.5 cm surrounded by GND ring
- **Calibration lines** (SMA connectors): it is possible to inject charge through 0.5 pF Capacitor in input to channels 1, 5, 12 and 16

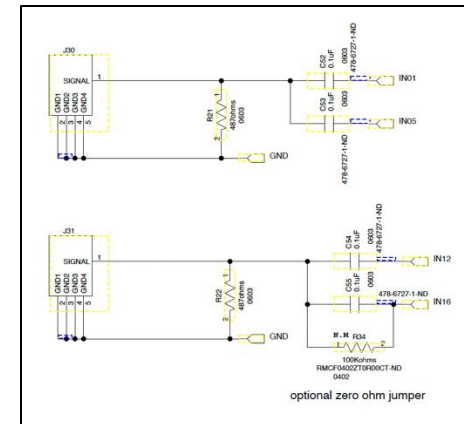


C = 0.5 pF

HV plate

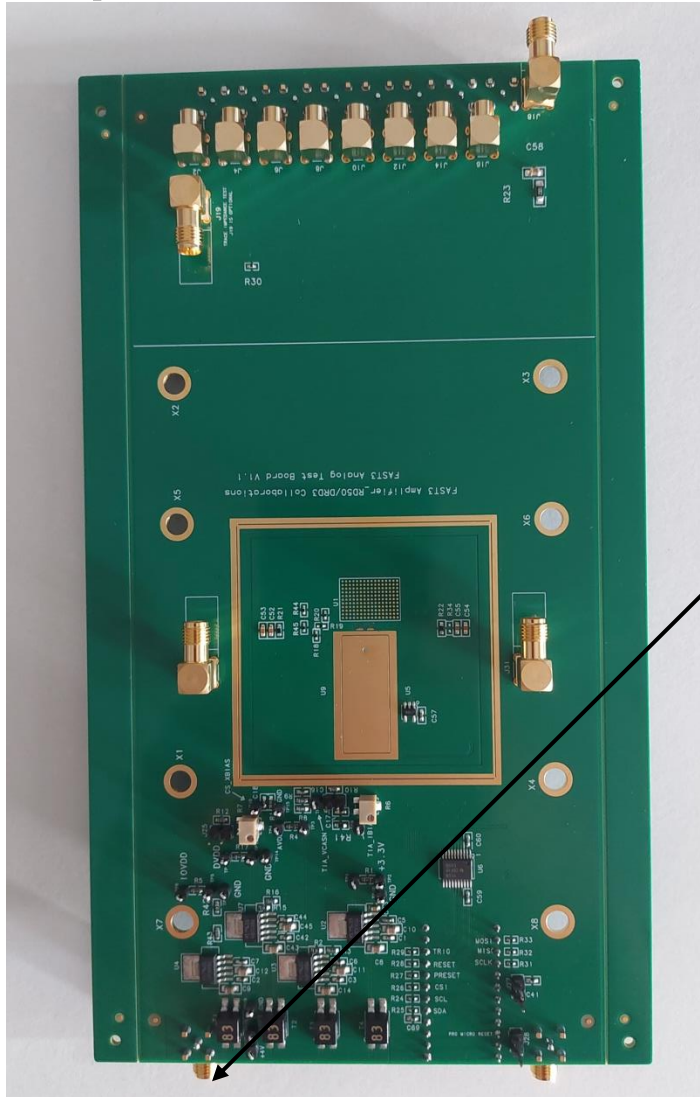
GND Ring

Electrical scheme of the calibration lines

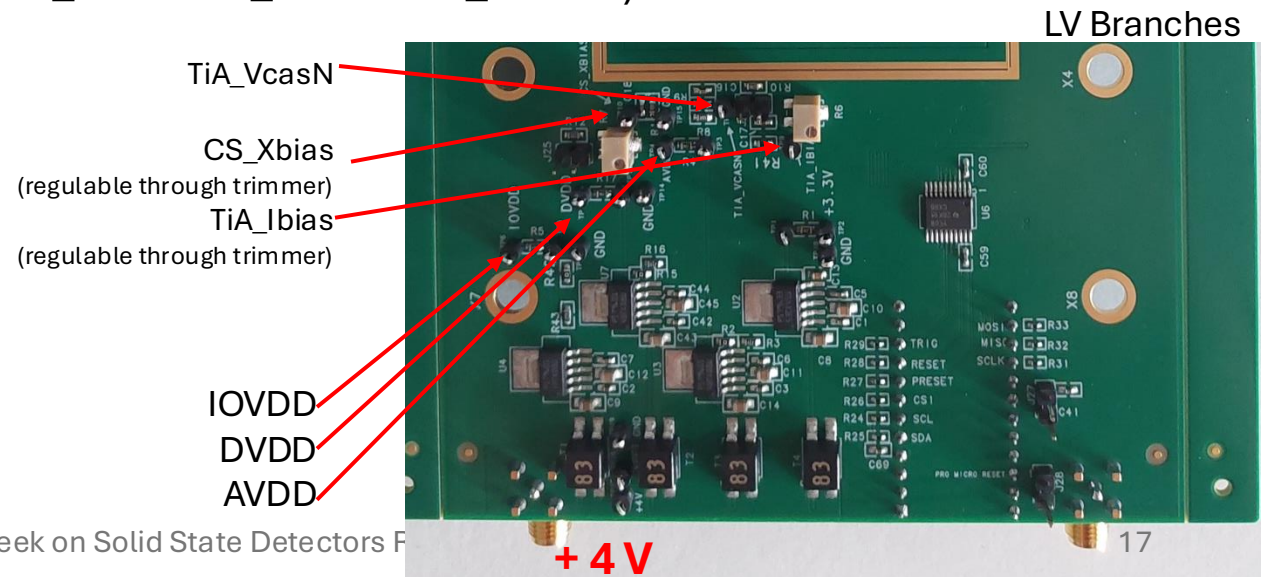


Readout board

Top side

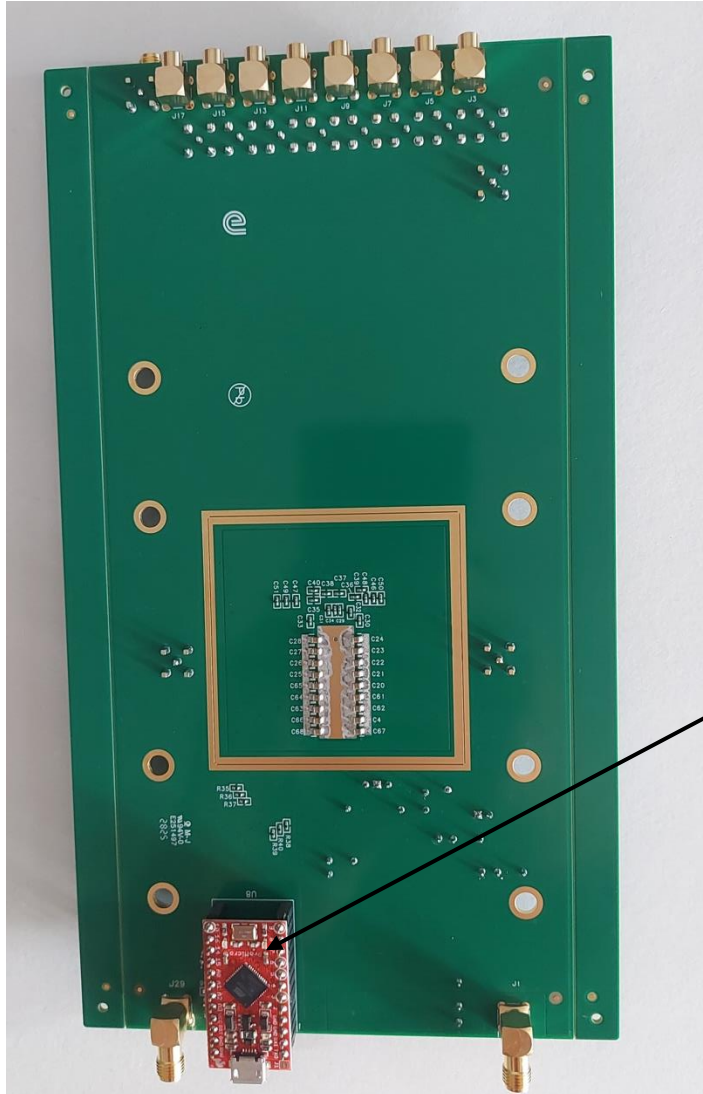


- SMA High Voltage connector
- MCX output connectors (8 for each side of the board)
- 10 k Ω resistor along the HV line
- HV plate \sim 1 cm x 2.5 cm surrounded by GND ring
- **Calibration lines** (SMA connectors): it is possible to inject charge through 0.5 pF Capacitor in input to channels 1, 5, 12 and 16
- Low Voltage SMA connector (Bias = + 4V)
- LV branches provides three different 1.2 V bias (AVDD/DVDD/IOVDD) and three other bias to set the working point of the amplification stages (TiA_Ibias/CS_Xbias/TiA_VcasN)



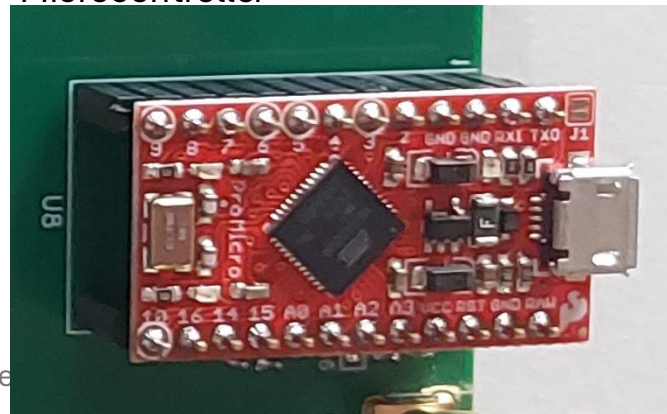
Readout board

Top side



- SMA High Voltage connector
- MCX output connectors (8 for each side of the board)
- 10 k Ω resistor along the HV line
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- LV branches provides three different 1.2 V bias (AVDD/DVDD/IOVDD) and three other bias to set the working point of the amplification stages (TiA_Ibias/CS_Xbias/TiA_VcasN)
- Compact Microcontroller compatible with Arduino language for gain programmable

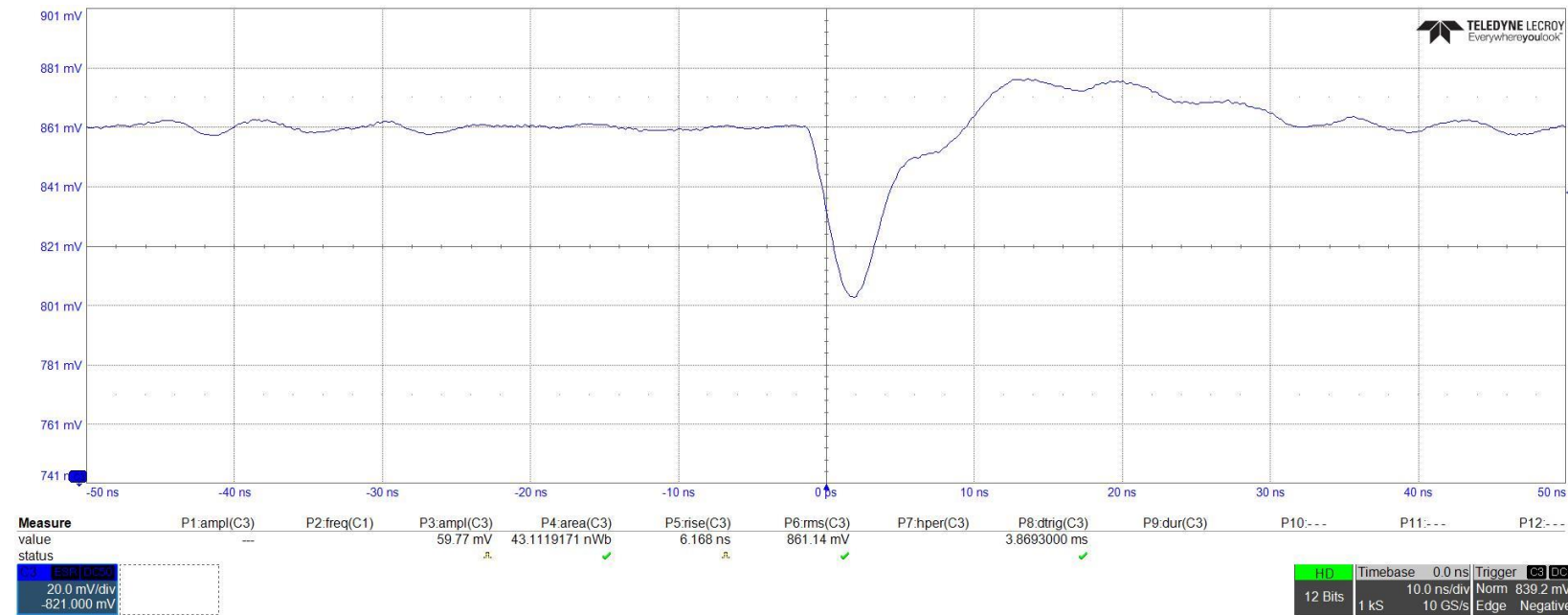
Microcontroller



The code for the programmable gain has yet to be develop

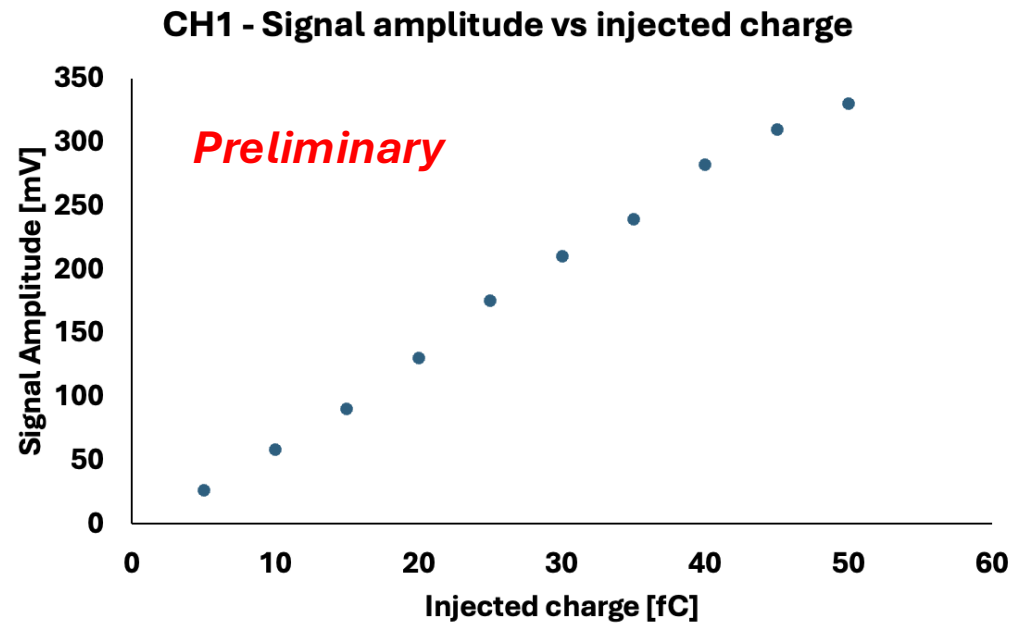
Power ON test

- FAST3-Amplifier switch ON
- A preliminary charge injection test showed that the FAST3-amplifier works



Power ON test

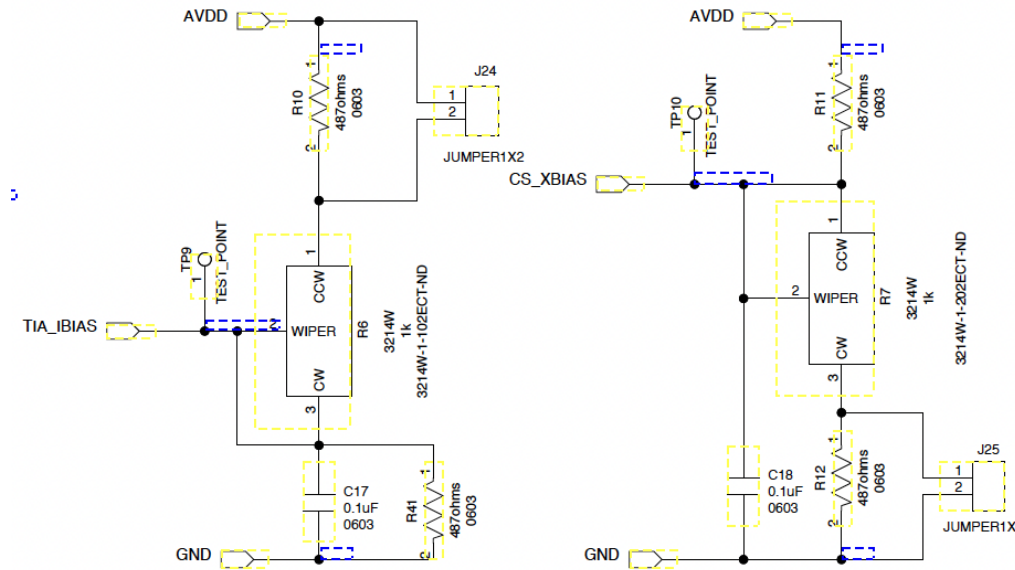
- FAST3-Amplifier switch ON
- A preliminary charge injection test showed that the FAST3-amplifier works



Power ON test

- FAST3-Amplifier switch ON
- A preliminary charge injection test showed that the FAST3-amplifier works
- The operation point of FAST3 is not the optimal one (The gain of FAST3 and S/N are 30%-40% lower than the expectation)

The operation point of the ASIC can be change at the board level, changing the resistors values of the bias branches TiA_Ibias and CS_Xbias



Summary

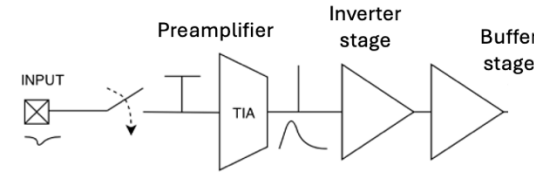
- Electronica released the batch of 10 amplifier at the end of October (2 amplifier on hold to wait the feedback from preliminary functionality tests)
- The power-on test show that the amplifier switch on correctly, but the ASIC working point is not the optimal one expected (too low gain)
- To set the properly operation point of the amplifier, the replacement of few resistor on the readout board is needed

One more week of work and we will have the first FAST3-Amplifier working properly and available to share with the institutes involved in the project.

Backup

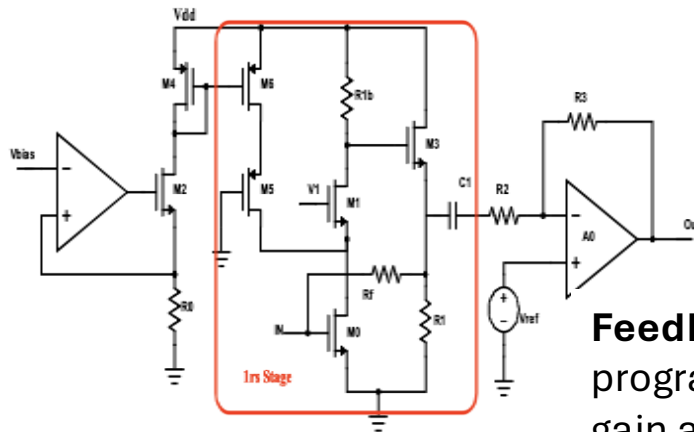
FAST3 prototype: Channel architecture

FAST3 Amplifier-only architecture (Analog version)



Pre-amplifier stage (2.3 mW/ch)

- Transimpedance Amplifier
- Common source topology implemented with RF input transistor
- 2 channel version:
 - Programmable DC gain: 3-bit adjustable gain
 - Fixed DC gain (not used for the RD50/DRD3 project)



Feedback resistor: in programmable version 8 different DC gain are obtained by combining three resistances: 5kΩ, 15kΩ and 30kΩ

Buffer stage (7.7 mW/ch)

- Operational amplifier (Class AB stage)
- DC gain = 6
- Guaranteed signal rise time of 1.5 ns
- Bandwidth = 1 GHz

