

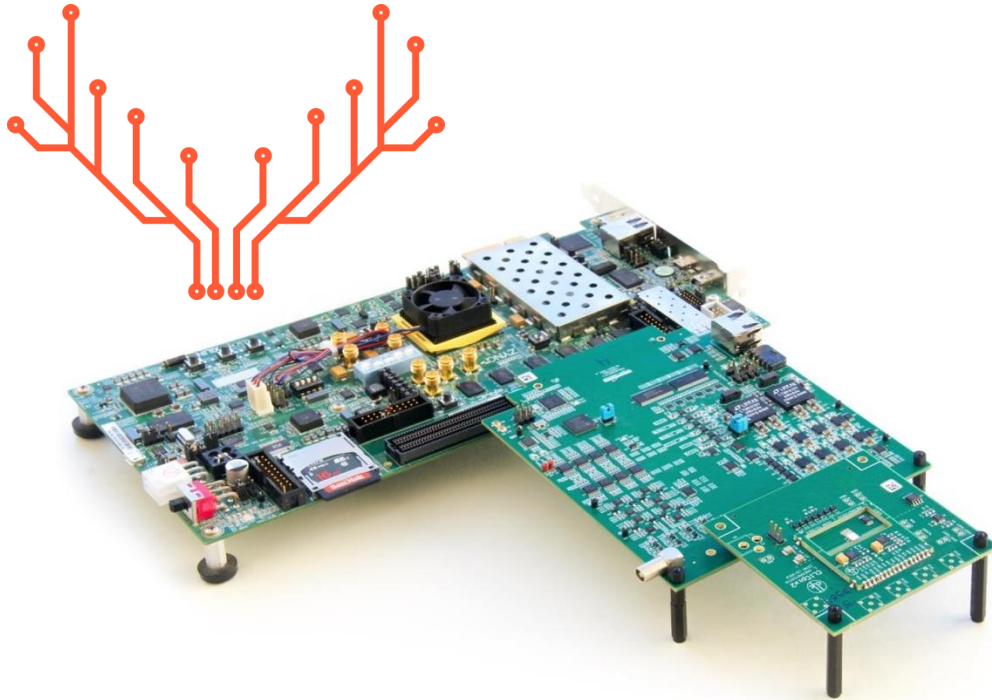
# Advancements and future expansions of the Caribou DAQ system

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4<sup>th</sup> DRD3 Week on Solid State Detectors – 13 November 2025

# An open source common platform

Open source hardware, firmware and software for laboratory and beam tests



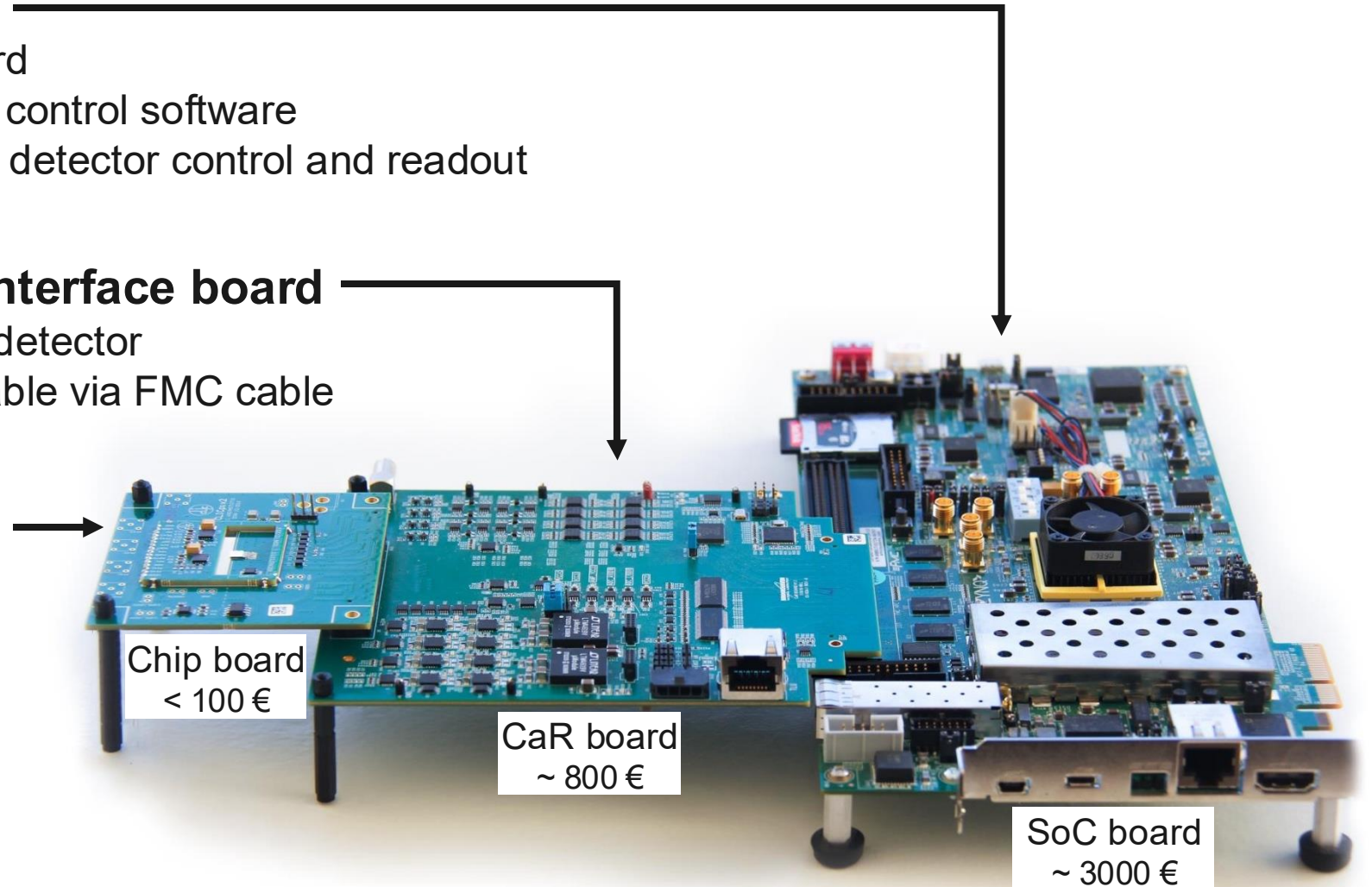
<https://caribou-project.docs.cern.ch>

Developed by a collective effort of hardware, firmware and software developers

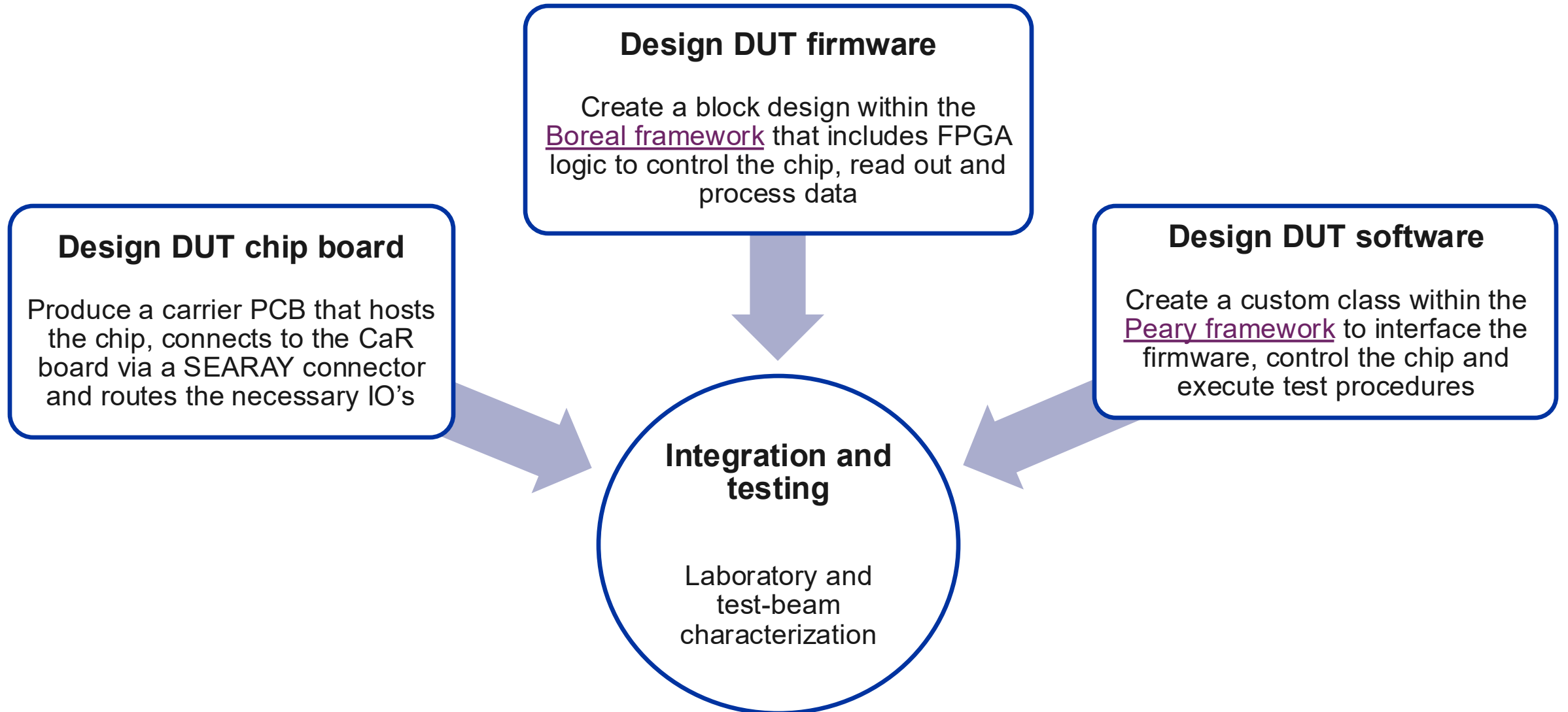


# A modular system architecture

- **System-on-Chip (SoC) board**
  - ie: Xilinx ZC706 evaluation board
  - Embedded CPU runs DAQ and control software
  - FPGA runs custom firmware for detector control and readout
- **Control and Readout (CaR) interface board**
  - Physical interface from SoC to detector
  - CaR – SoC connection extendable via FMC cable
- **Detector (chip) carrier board**
  - Custom low-cost PCB
  - Designed by users



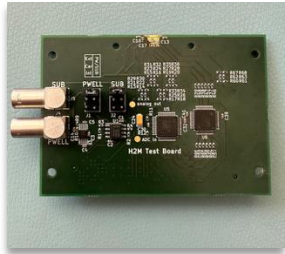
# A streamlined device integration workflow



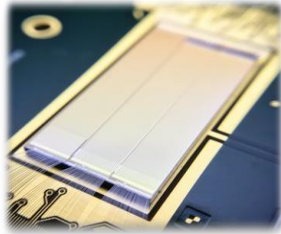
# A large variety of integrated detectors

- Multiple detectors already integrated and tested:

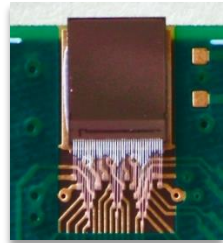
H2M



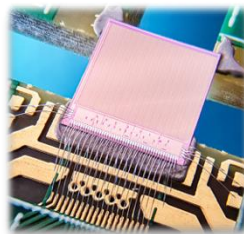
ATLASpix



CLICpix2



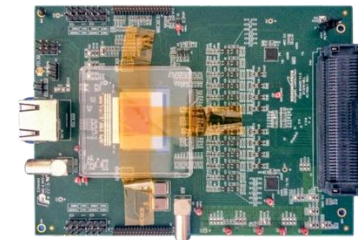
CLICTD



FASTPIX



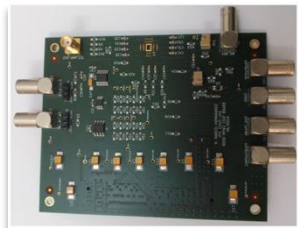
H35Demo/FEI4



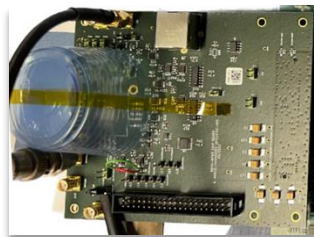
RD50-MPW1



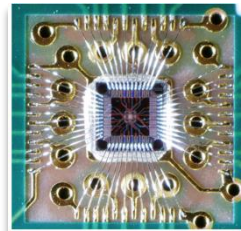
RD50-MPW2



RD50-MPW3



APTS



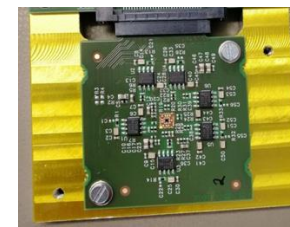
DPTS



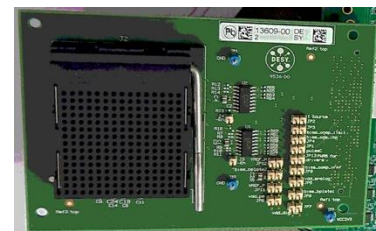
dSiPM



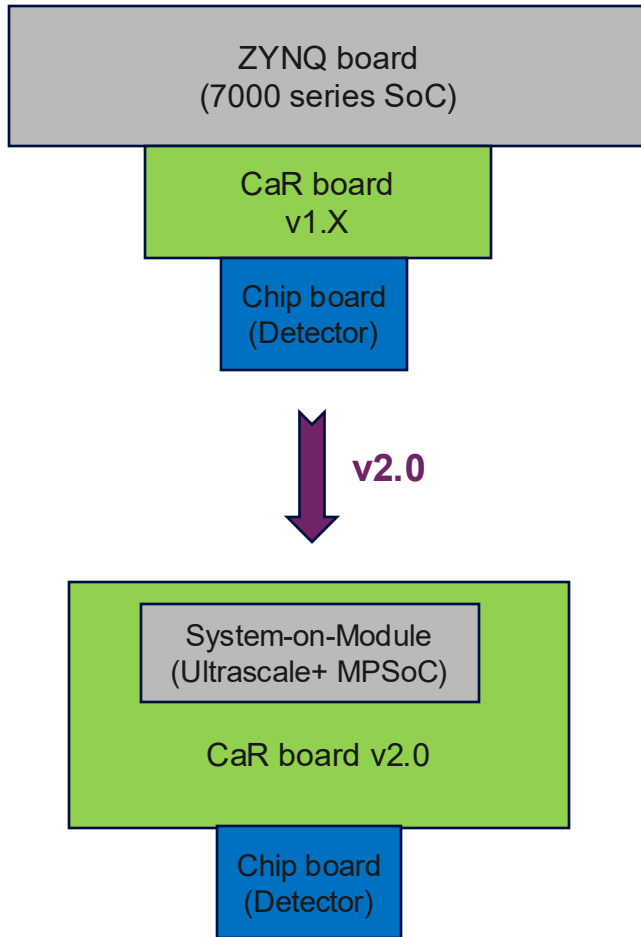
MLR1



CoRDIA



# An upcoming system upgrade - Caribou v2.0



- Based on commercial **System-on-Module (SoM)**
  - Integrated to the CaR board
  - Optimize system cost, increase flexibility and performance
- Targeting Mercury+ XU1 (UltraScale+) System-on-Module
- Test-board design finalized; Final board design progressing
- Expanding portfolio of supported boards

Xilinx ZC706  
evaluation board



**Supported**

**But discontinued for purchase**

Possible replacement: EVAL-TPG-ZYNQ3  
(not yet tested)

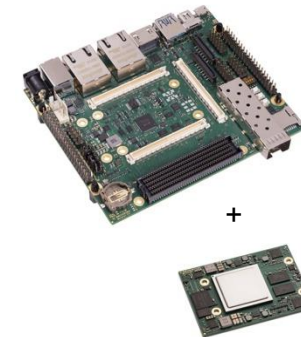
Xilinx ZCU102  
evaluation board



**Supported**

**Intermediate step towards Caribou v2.0**

Enclustra  
Mercury+ ST1



Enclustra  
Mercury+ XU1



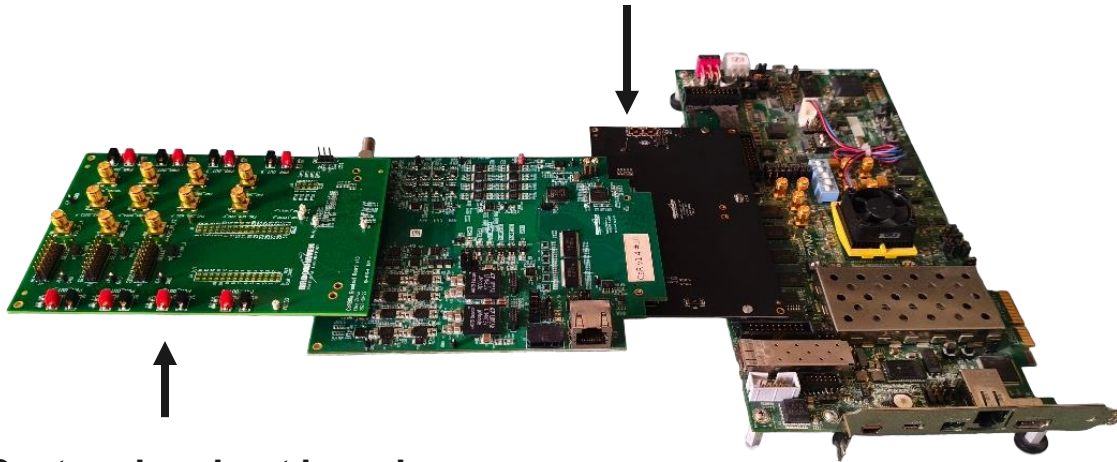
# A CaR board v1.5 validation setup

## Post-production quality control of CaR board

- Verification of all CaR board functionalities
  - LVDS, GT, power supplies, ADCs, ...
- Integrated with Boreal and Peary frameworks
- Validation performed prior to distribution of board

### Adapter board

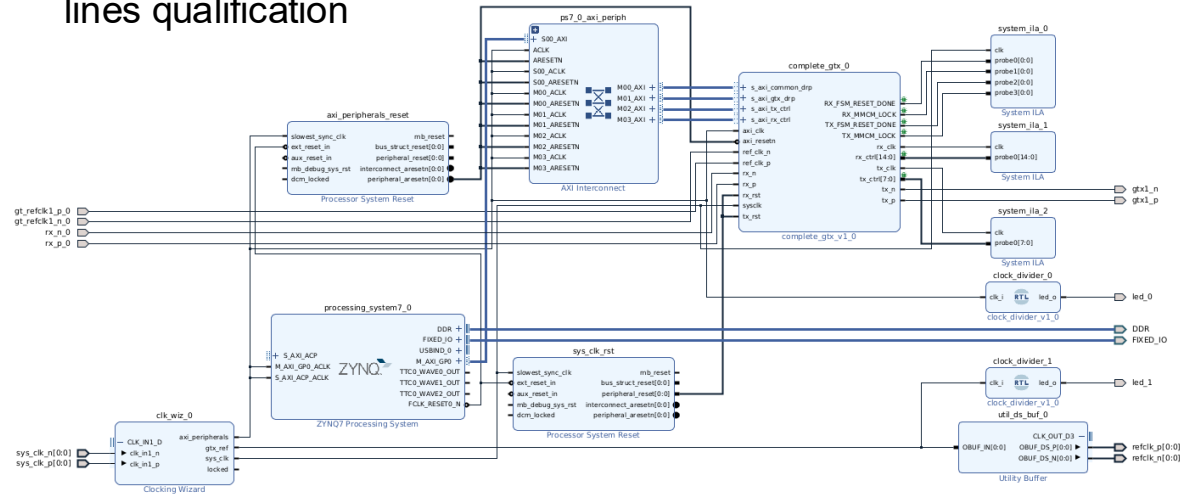
- Expands FMC IO's, giving access to all breakout board resources



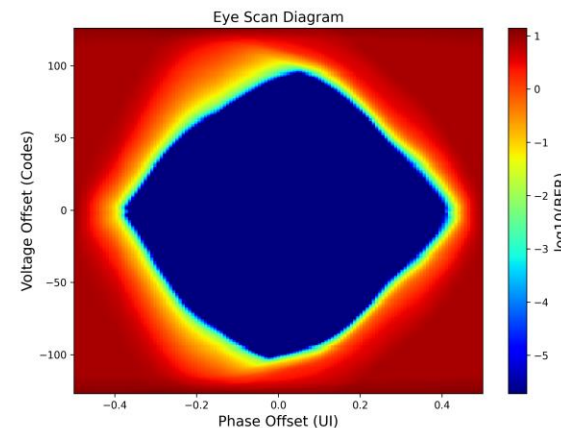
### Custom breakout board

- Looped LVDS signals
- SMA inputs to GTX lines
- Voltage and current outputs
- Inputs to slow and fast ADCs

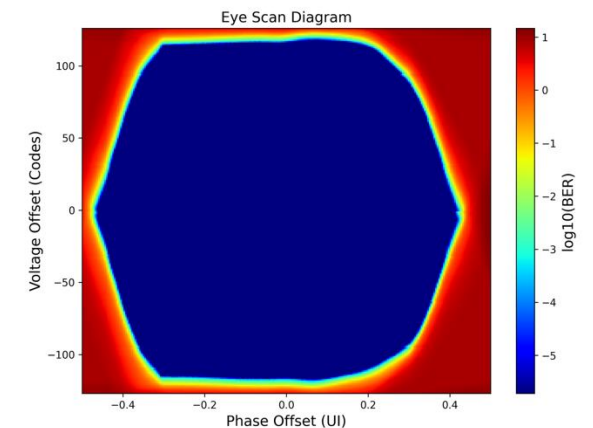
## Firmware block for GT lines qualification



Eye diagram @5.12 Gbps

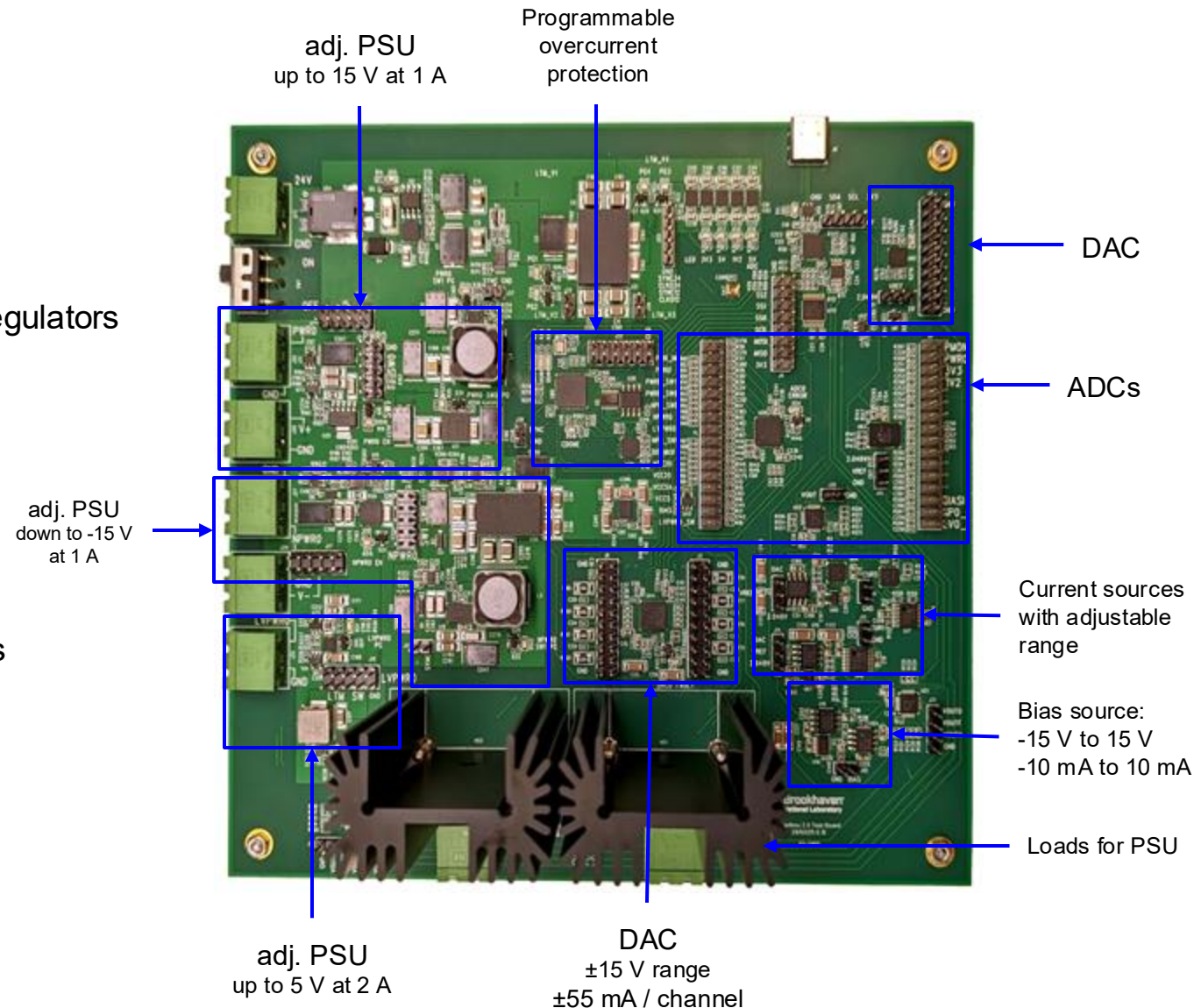


Eye diagram @2.56 Gbps



# A CaR board v2.0 test board

- Test board as an **intermediate step towards v2.0**
- **Goals:**
  - Verification of analog circuits and power supplies
  - Evaluation of different design options
    - Integrated DC-DC converter modules / discrete regulators
    - High / low current sources
- **Simplified compared to full-scale v2.0**
  - No SoM, controlled via USB
  - Fewer resource channels
- **Improvements with respect to v1.5:**
  - Increased range for power supplies and current sources
  - Negative supply voltages
  - Improved overcurrent protection
  - Better ADCs and DACs
- Scale up to v2.0 after all circuits are validated
- Boards arrived and are currently being tested



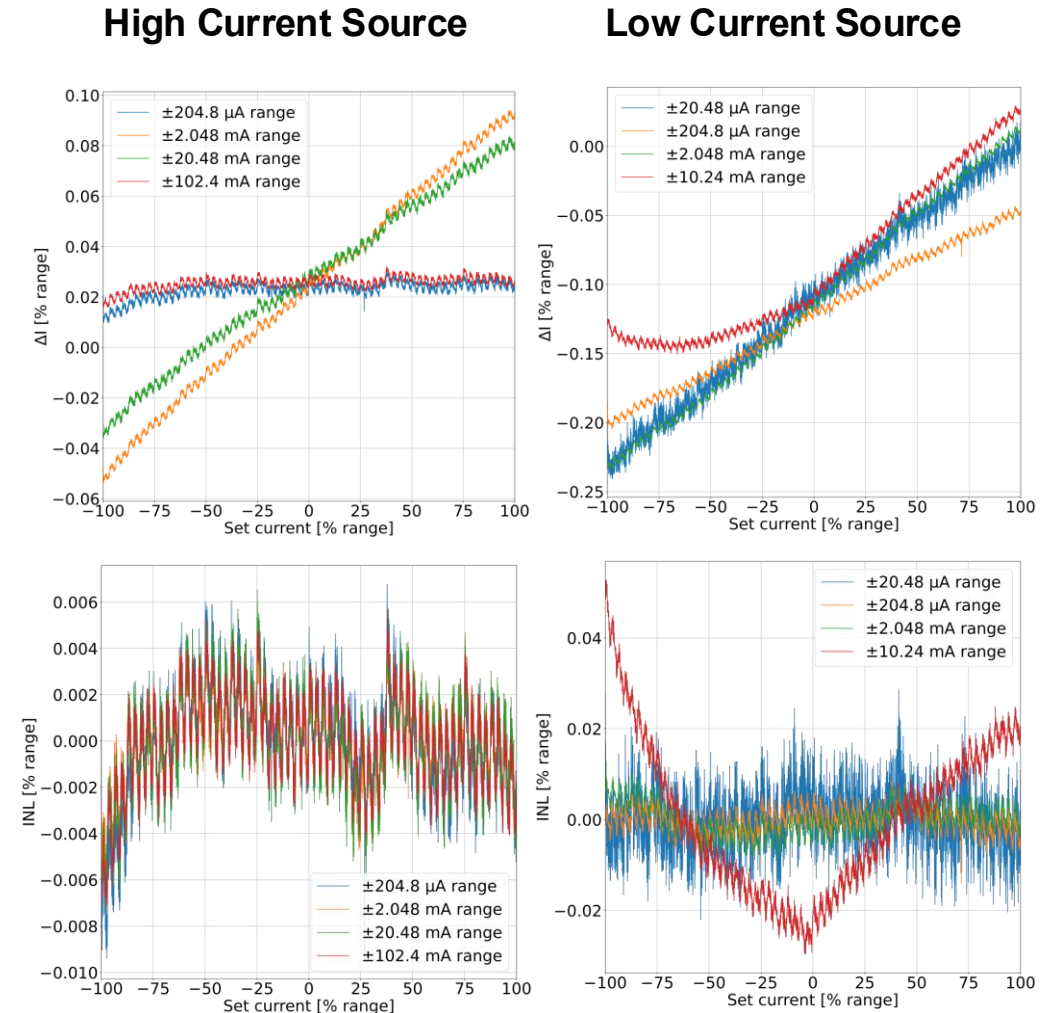
# A CaR board v2.0 test board – Example result

## Current sources

- **Two variants:**
  - High current source: up to 102.4 mA
  - Low current source: up to 10.24 mA
- The INL is almost identical across all ranges and agrees well with INL of the DAC
- Maximum INL is  $\pm 1$  LSB and  $\Delta I$  yields a  $\pm 0.1$ – $0.25\%$  deviation
- High current source performs significantly better than the lower current source

## Other components

Tests of the other components ongoing (power supplies, ADCs, DACs, Over-Current-Protection logic design, ...)



# A set of new FPGA common modules

## Expanding portofolio FPGA modules

- Signal and bus synchronizers
- RTL-based clock gating
- Configurable counter
- Pulse edge detection logic
- Pulsing and shutter control
- AXI4Lite register map
- AXI-Stream (de)serializer
- Trigger Logic Unit (TLU) interface
- AD9249 high-speed ADC interface
- Time-to-Digital Converter (TDC)

All integrated with functional verification into the [Boreal-Modules](#) library shipped with our [Boreal](#) FPGA framework

Focus on porting some of the modules to the UltraScale+ platform in preparation for Caribou v2

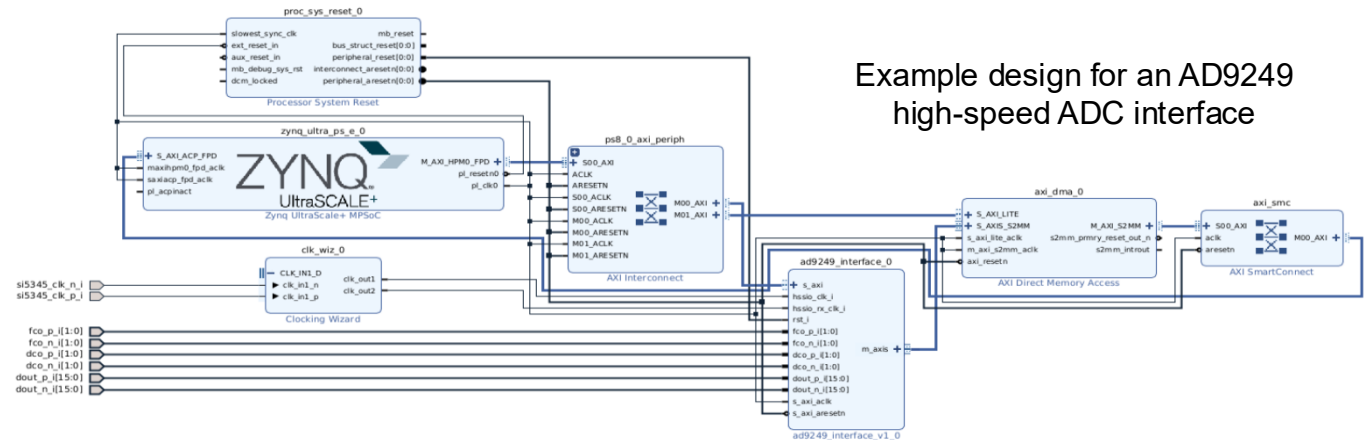
Xilinx [ZCU102](#) evaluation board



Enclustra [Mercury+ ST1](#)



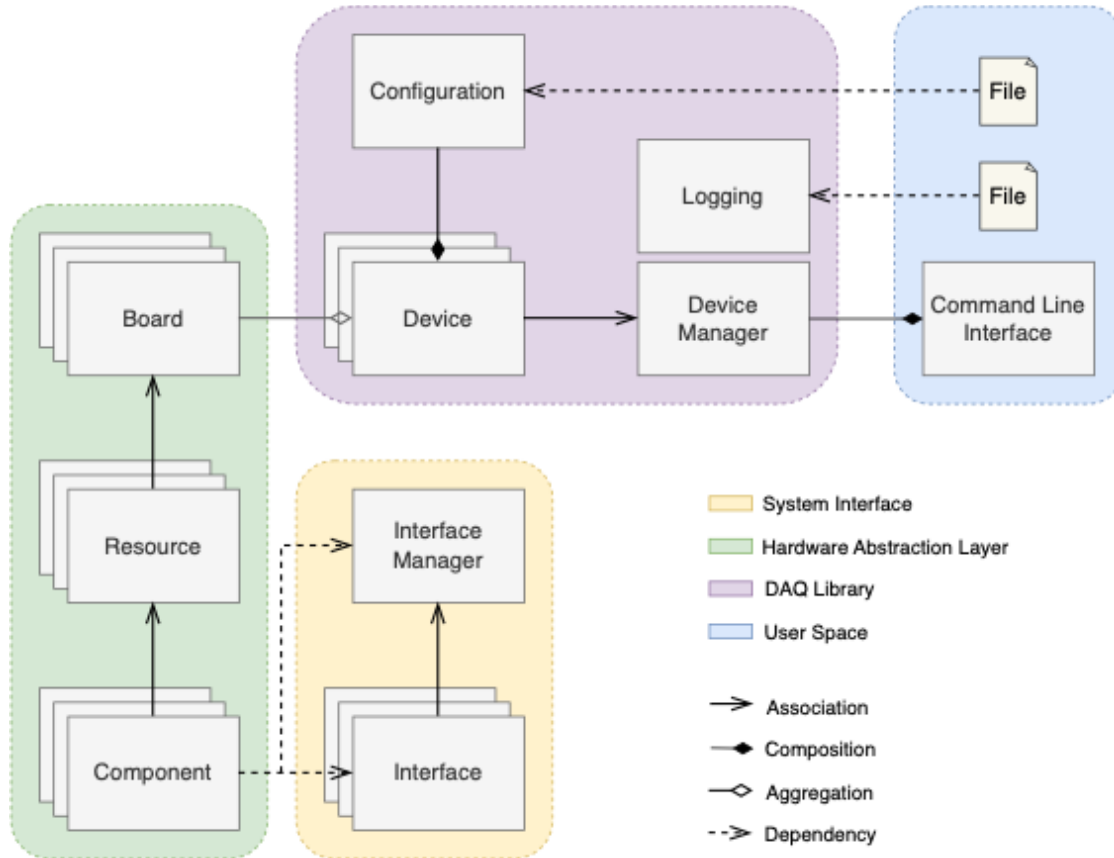
Enclustra [Mercury+ XU1](#)



Example design for an AD9249 high-speed ADC interface

# A new embedded software architecture

A major release is on its way with a new architecture and Hardware Abstraction Layer structure

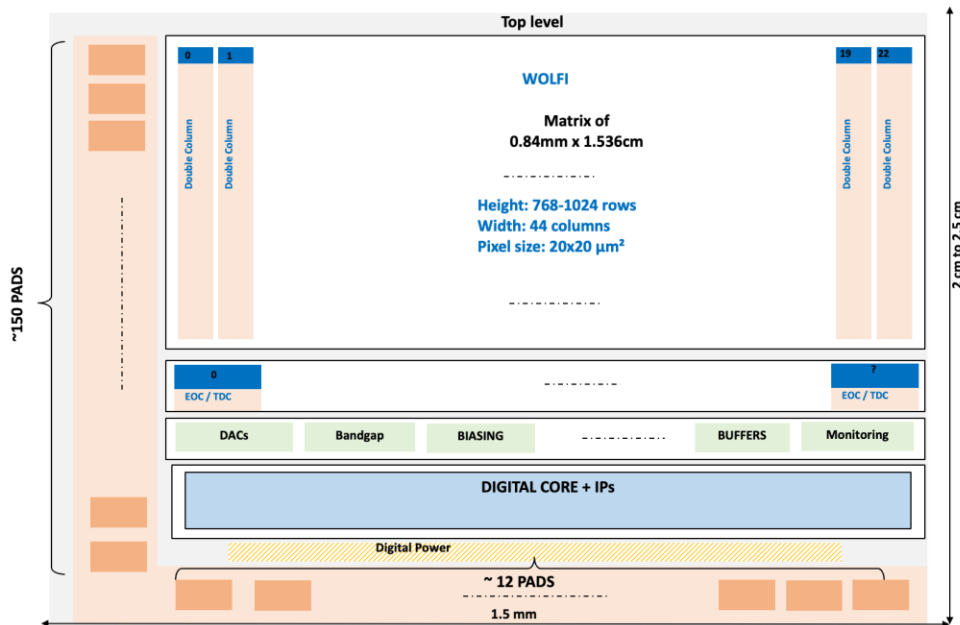


- New concept of *Resources*
  - *Logical board functionalities that may be implemented using one or more hardware components to achieve a specific purpose*
- Individual *Component* classes
  - Independent support for each IC (power supply, ADCs, DACs, clock synthesizer, ...)
- Improved modularity for an easier integration and multi-board/platform support
  - Any new *Component* or *Resource* can be easily added to the hierarchy
  - Any new *Board* can be constructed using available *Components* and *Resources*
- Streamlined CI/CD with cross-platform compilation for an inclusive development workflow

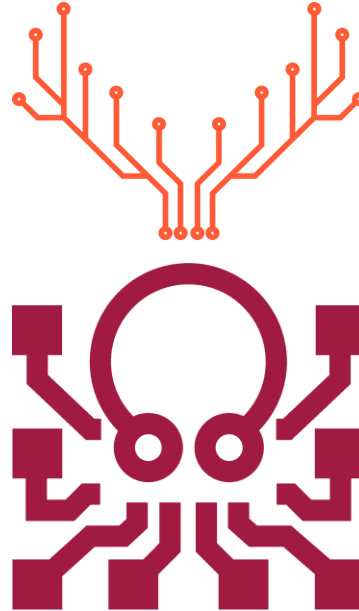
# A test system for the OCTOPUS project

## Target prototype: WOLFI

- MAPS vertex sensor demonstrator for future lepton colliders
- Based on APA readout architecture
- On-chip IpGBT Encoder and 6 TX @10G24
- Full Caribou integration in the plan



WOLFI Layout



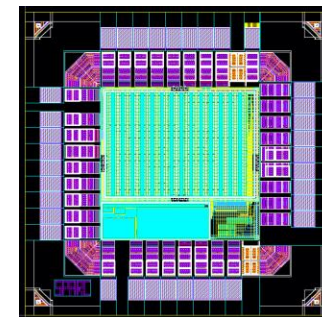
[Link to DRD3 talk by Roberto Russo](#)

## OCTOPUS WP3: Data Acquisition

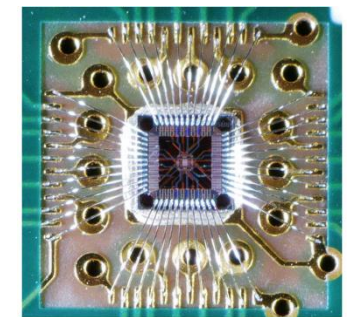
- Chip board design for prototypes
- Integration of prototypes (software, firmware)
- Chip board assembly, bonding and logistics

## Pilot prototypes:

- SPARC (ER2)
  - Testing Asynchronous Priority Arbitrer (APA) readout architecture
- APTS w/ N-Cross (ER2 respin, ER3)
  - Testing layouts from OCTOPUS simulation
- OCTOPUS chiplets (ER3)
  - Different blocks for large-area chip



SPARC



APTS

# A CaR board v1.5 combined purchase order



## Expanding our User Community



- **>60 CaR boards** produced
- Distributed to **>20 institutes**
- Supported as RD50 and DRD3 *Common Funds* project

[CaR Board v1.5 schematics](#)

2024-2025 purchase order summary

Batch	Delivery	Boards	Institutes	Status
MAY2024	July 2024	31	9	Complete
JAN2025	March 2025	12	7	Complete
NOV2025	~ March 2026	9	5	Ongoing

[CaR board Common-Func Project Description](#)

## Call for new purchase order

Currently collecting requests for another CaR board v1.5 combined purchase order

**Unit price: 800-1000€**

Would you like to acquire one or more board ?

**! Contact us !**

**at**

[caribou-developers@cern.ch](mailto:caribou-developers@cern.ch)

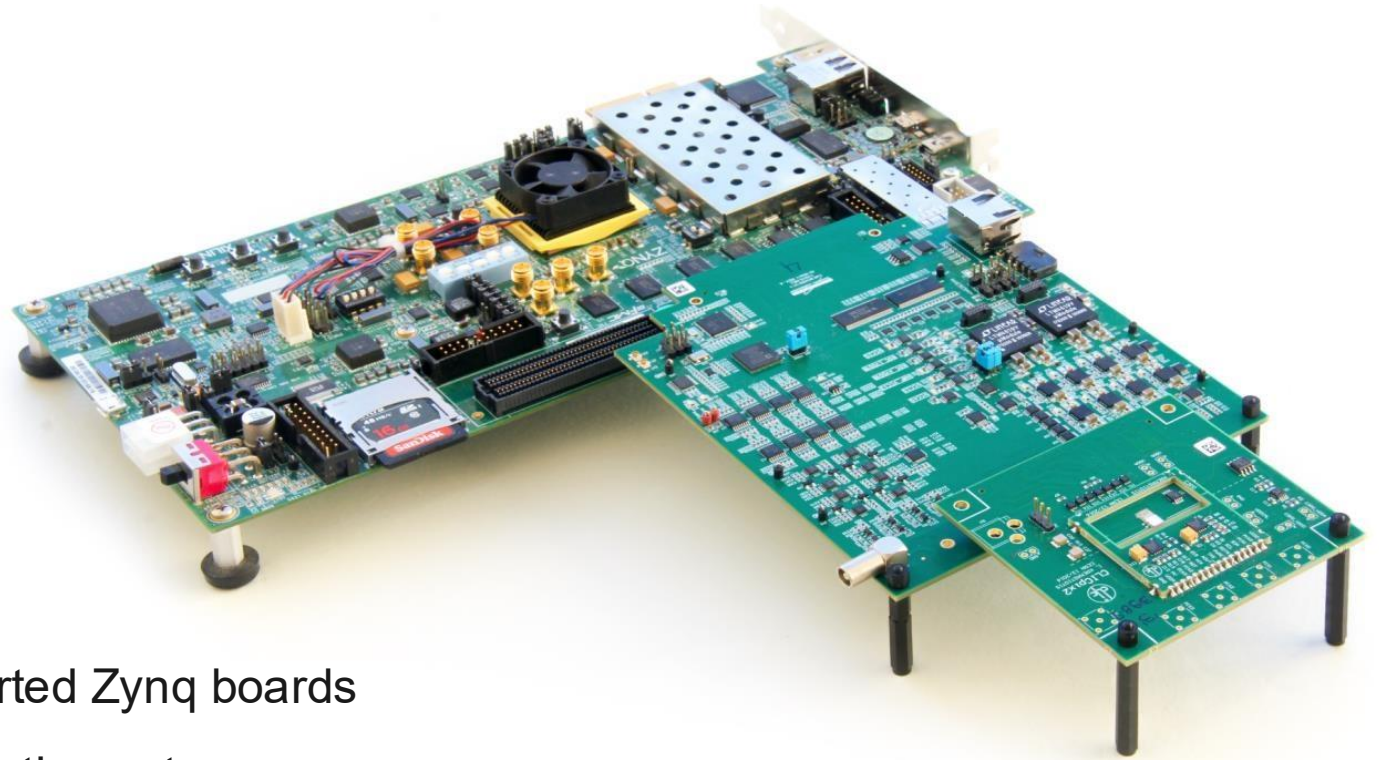
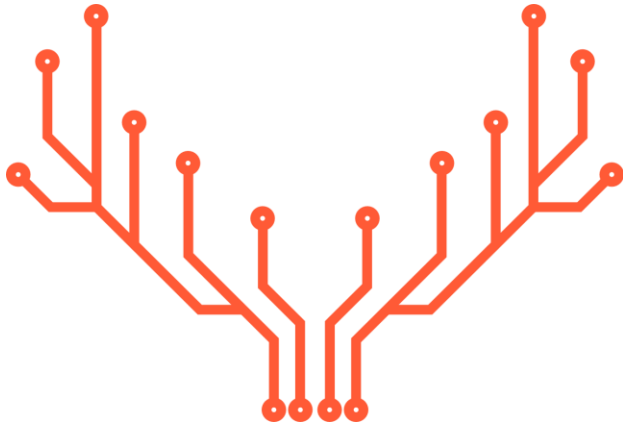
**or**

[dominik.dannheim@cern.ch](mailto:dominik.dannheim@cern.ch)

[younes.otarid@cern.ch](mailto:younes.otarid@cern.ch)

We plan to amend the existing common-funds project for CaR boards v1.5, once we have the final list of institutes and number of boards

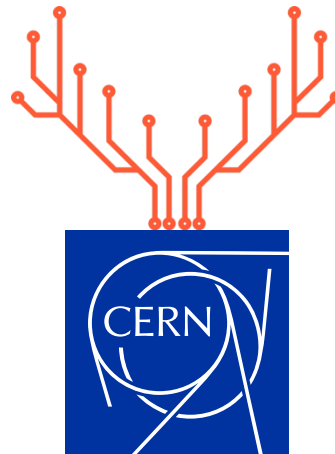
# Summary



- Expanding of the portfolio of supported Zynq boards
- Developing a CaR board v1.5 validation setup
- Producing and testing of CaR board v2.0 test board
- Expanding the FPGA design workflow and pool of common modules
- Improving the embedded DAQ application architecture and design
- Calling for a new CaR board v1.5 common purchase order



# Thank you



## Contact

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[home.cern](http://home.cern)

# A modular system architecture

