

# Status on access and submission in TPSCo 65nm ISC

*November 10<sup>th</sup> 2025*

## TPSCo 65 nm ISC status

- Process with modifications qualified for HEP, made available to the community. Further optimizations in ER2.
- Foundry has been very flexible in making process modifications in a collaborative effort.
- Synergy between EP R&D WP1.2 and ALICE with significant effort for the ALICE ITS3 upgrade
- No MPWs, only engineering runs
  
- Submissions so far used to define a custom design flow and support for common run, see Pedro Leitao's presentation <https://indico.cern.ch/event/1553023/>
  
- ER2 was submitted with the MOSAIX for the ALICE ITS3 upgrade and 36 chiplets (see next page), wafers in the line, but no precise delivery date yet.
  
- ER3 is to be submitted next year with final MOSAIX, where ALICE intends to also use chiplet positions to prepare for ALICE3.

**DRD3 Questions:**

- **Can you provide the timeline that will be honoured? How much does that plan depend on the fraction of the money provided by the DRD3 groups for the MLR runs.**
- **Does the initial pledge that CERN financial contribution to the MLR runs is around 50% and that 50% should be collected by the participating projects still hold?**
- **What is the size of chiplets that would be available in the coming ER for ITS3 and what would be the cost for those that would like to participate in it. When do you need the feedback?**
- **DRD7.6a project proposal contains the sharing of existing or future IP blocks of various types to the community. We understood that includes DRD3 groups (with proper NDA signed), is that correct? If yes, can we define the protocol of how to transfer that to DRD3 designs.**

**MPR runs:**

- CERN can organize MPR runs upon request from the community, provided participants can generate the required funding. Participants are then fully in control of the schedule and can decide on the submission date at their convenience.
- CERN will participate with a financial contribution of about 50% to runs where it includes a significant number of test designs, and hence a significant fraction of the area.
- Today, due to the delays with the ER2 submission and the commitments with ALICE ITS3 (ER3), CERN does not see a large contribution possible before the first half of 2027. Should there be an MPR run before that, CERN would participate bearing a cost proportional to the area usage, as any other user of the run (assuming CERN would have a small structure to drop in).
- If users are ready for a substantial MPR run at the end of 2026, they should set the timeline and CERN will assist with the submission, as announced previously. CERN will however only contribute pro-rata area usage if it has structures to drop in.
- Note: dedicated runs using existing mask sets to study the sensor where only the layout of the sensor implants are modified and chiplets are made available with the new sensor layout can be envisaged.

## Chiplets in ER3:

### Projects interested:

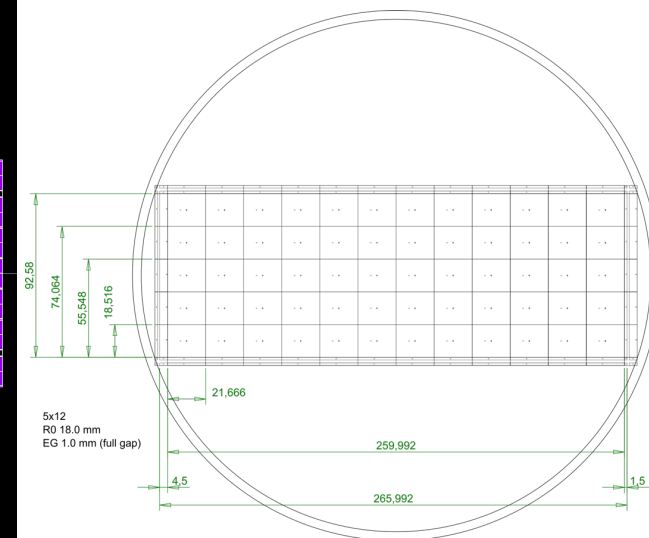
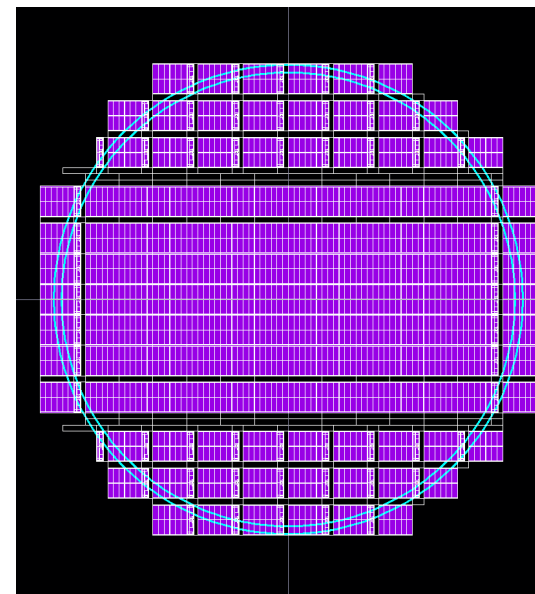
- Octopus, Manta, Architectures for Timing, Malta
- TDC (SLAC), Plasma diagnostic sensor, Particam

### ER3: identical floorplan apart from chiplets: in total 36 positions

- 2 x 14 chiplet positions in the stitched regions
- 2 x 3 in the left end cap, 2 x 1 in the right end cap

### ALICE:

- ER3 will be owned and managed by ALICE. In principle ALICE is willing to accommodate a few chiplets on ER3, but discussions on sharing the run and its timeline will be difficult before the MOSAIX silicon (ER2) is in hands. There is thus significant uncertainty in any plan based on piggy-backing on ER3. Based on previous experience, one can envisage ~20 % or 6-7 chiplet positions of 1.5 mm x 1.5 mm are made available, combined or not into larger chips (always 1.5 mm wide, probably up to a maximum of 3 x 1.5 mm, tbc). Feedback on whether combined chiplets are desired should come by early next year.



**IP sharing: (see also P. Leitao's presentation on support) <https://indico.cern.ch/event/1553023/>**

- TPSCo offers mixed-signal design kit: PDK (analog), DDK (digital), IP blocks: std. cells, I/O pads, SRAM/ROM compiler, eFuses
- CERN has created a number of technical add-ons to the design kit: modified pads and pad ring for chiplets, sensor layout, isolation structures, SLVS pads, custom DRC rules and a design flow:
  - RTL2GDS workflow (digital-on-top methodology)
  - IR drop and electromigration analysis support
  - SEE design and verification support
- CERN makes available pad ring, sensor layout, isolation structures, custom DRC rules, and design flow, to all users having signed nda and compliance letters, including those from DRD3.
- For IP blocks, as is always done in other technologies supported by the CERN Foundry Service, the group(s) having designed the block remain its owners. Any use of the block must thus be negotiated on a case-by-case basis with the owner(s). IP blocks should have been tested on silicon.
- CERN will facilitate the process by providing template agreement documents in line with the conditions applicable in other technologies, and compliant with the Europractice and Cadence agreements in place. For frequently used IP blocks, one could envisage negotiating access conditions once and centrally with the owner(s), and setting up template agreement documents which would then be used upon request on a case-by-case basis.

**Summary:**

- CERN can organize and support separate runs to avoid issues with synchronization with ALICE.
- CERN makes available pad ring, sensor layout, isolation structures, custom DRC rules, and design flow, to all users having signed nda and compliance letters
- Concerning the IP, the institutes that designed it, remain its owner. Once a block is tested, its sharing can be negotiated on a case-by-case basis, where CERN can help with the paperwork. It was agreed we would start with few blocks, based on a grouped request by DRD3.
- Access: Most groups that requested access should now have access. We are now grouping the new demands to avoid sending requests one by one.