

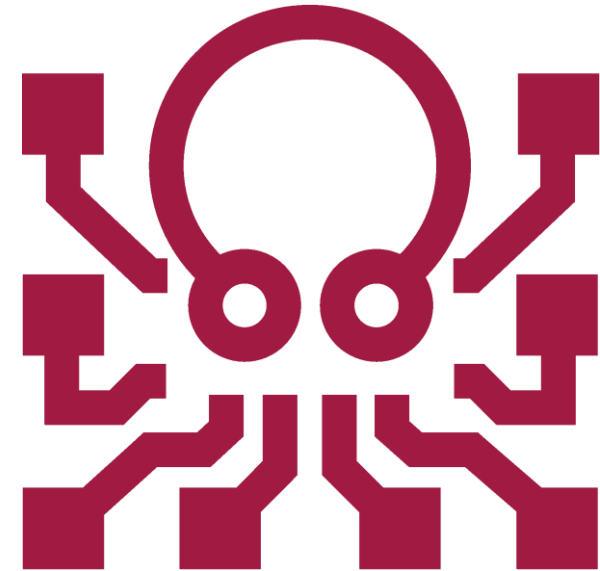
The OCTOPUS project

Optimizing monolithic active pixel sensors for the next generation of lepton collider experiments

Roberto Russo

on behalf of the OCTOPUS project

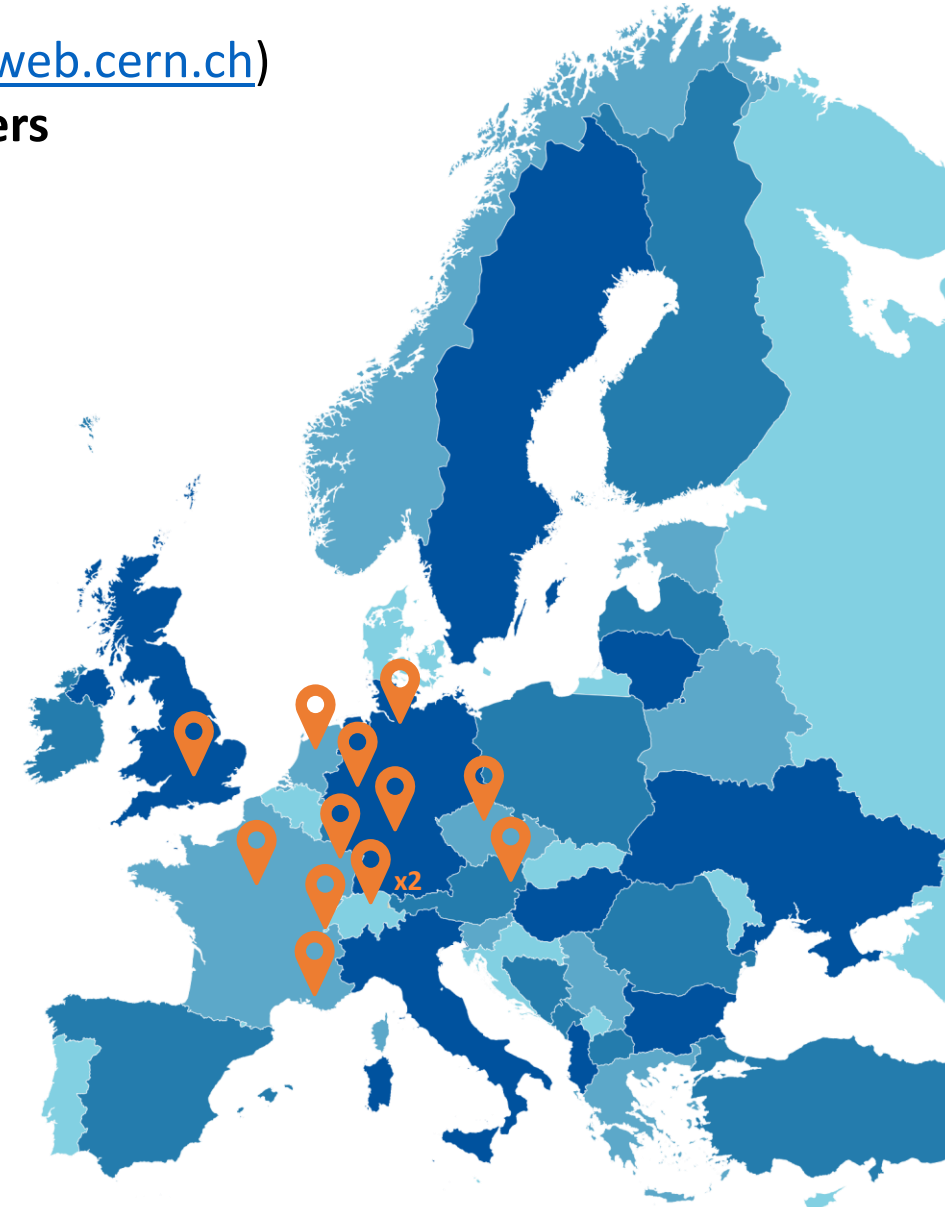
4th DRD3 week on Solid State Detectors R&D
CERN, 10 November 2025



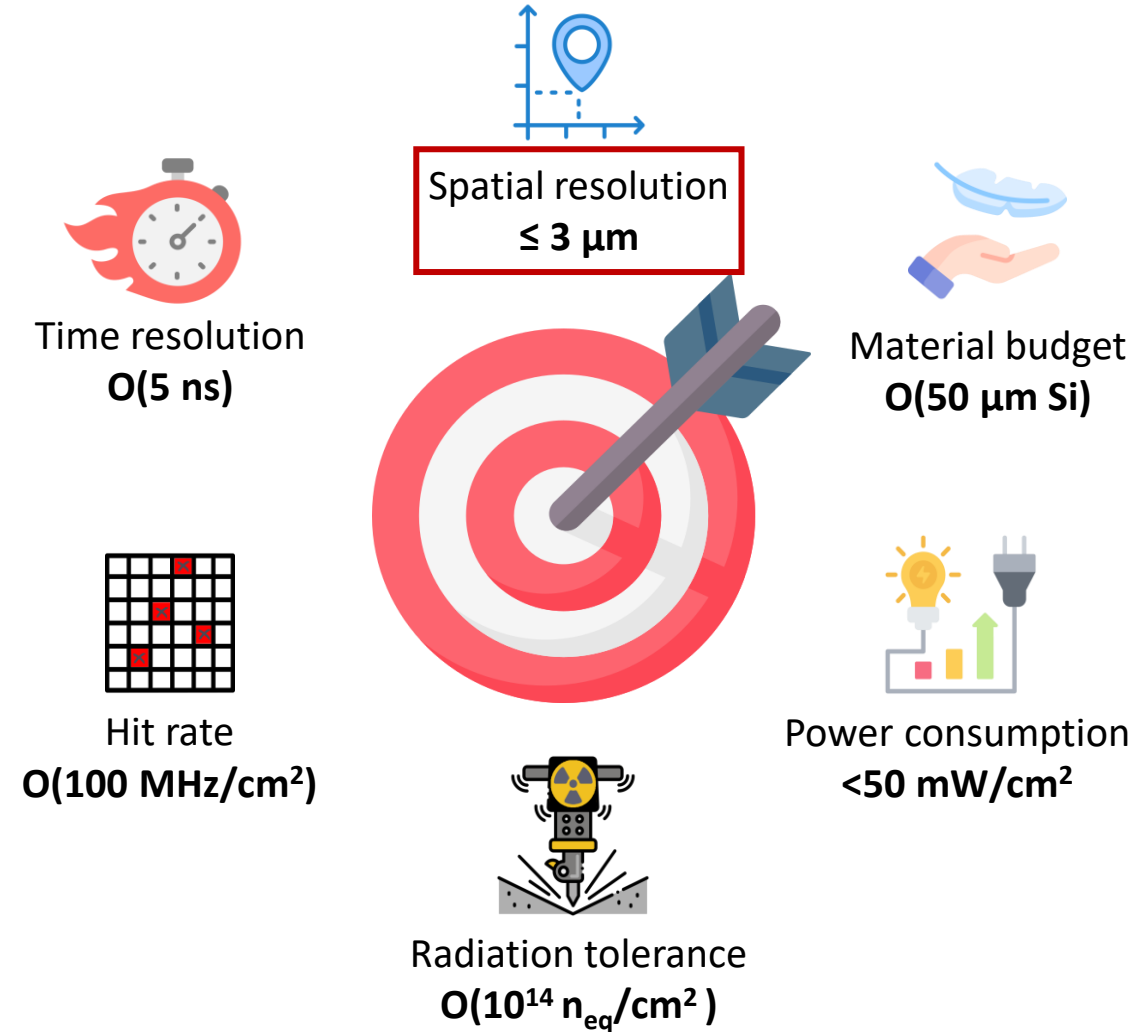
Optimized **C**MOS **T**echnology **F**or **P**recision in **U**ltra-thin **S**ilicon (octopus.web.cern.ch)

- R&D program towards a **vertex detectors** for the **future lepton colliders**
- **Reticle-size CMOS sensor** in **TPSCo 65 nm** process
- Full R&D chain performed by 13 institutes across Europe

Member institutes	
APC Paris	GSI Darmstadt
Universität Bonn	IPHC Strasbourg
CPPM Marseille	MBI Vienna
CERN Geneva	NIKHEF Amsterdam
DESY Hamburg	University of Oxford
ETH Zürich	Universität Zürich
FNSPE CTU Prague	

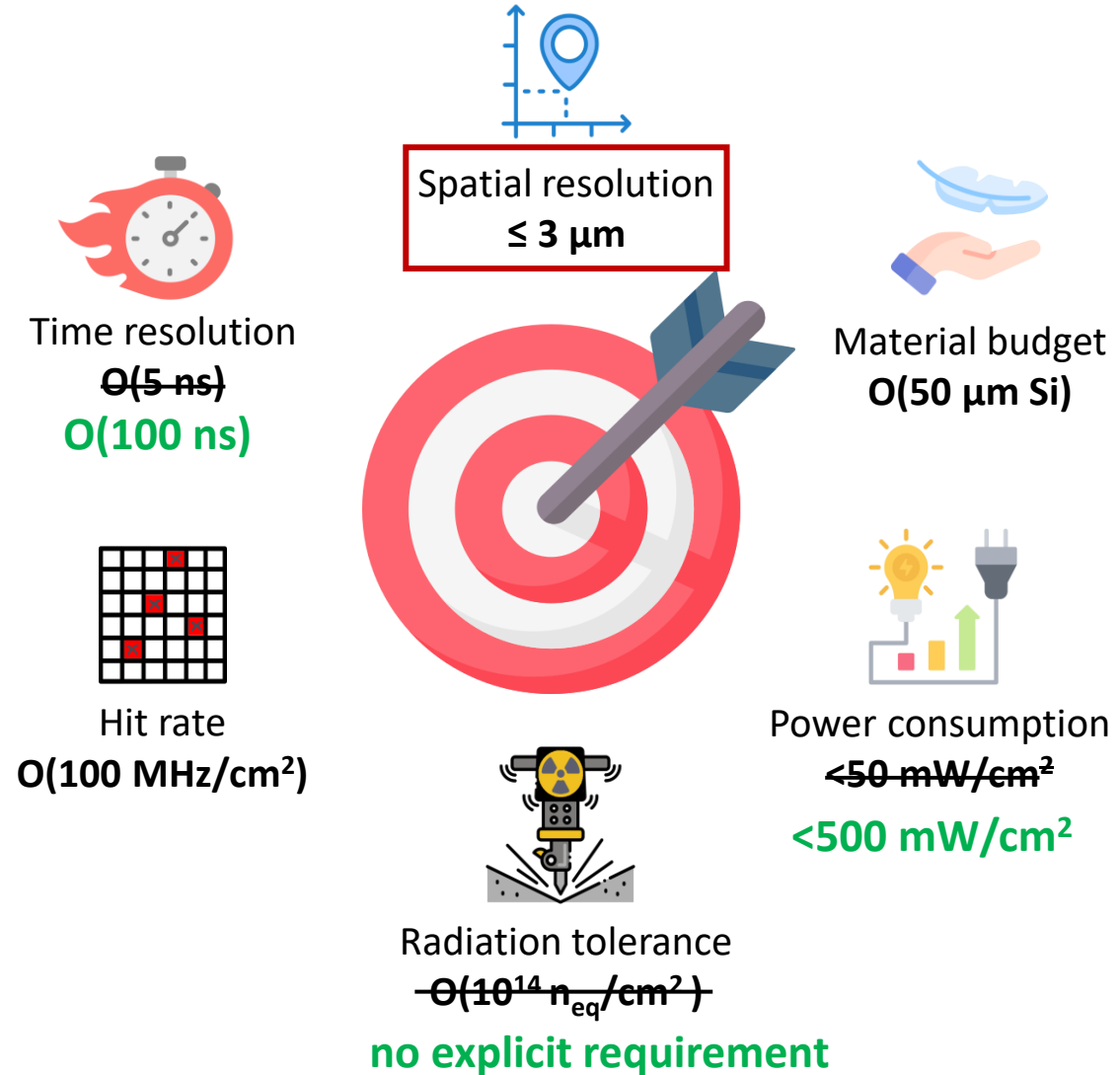


- **Reticle-size, fine-pitched** monolithic active pixel sensor (**MAPS**) demonstrator for vertex detectors operating in future $e^+ e^-$ colliders
- **TPSCo 65 nm CMOS process** available thanks to liason with DRD7
- Sensor requirements aligned with the 2021 ECFA detector [roadmap](#)
 - Final requirements will be updated after approval of a future collider project
- Particularly “**aggressive**” **spatial resolution** goal
 - Severe limitation to pixel pitch

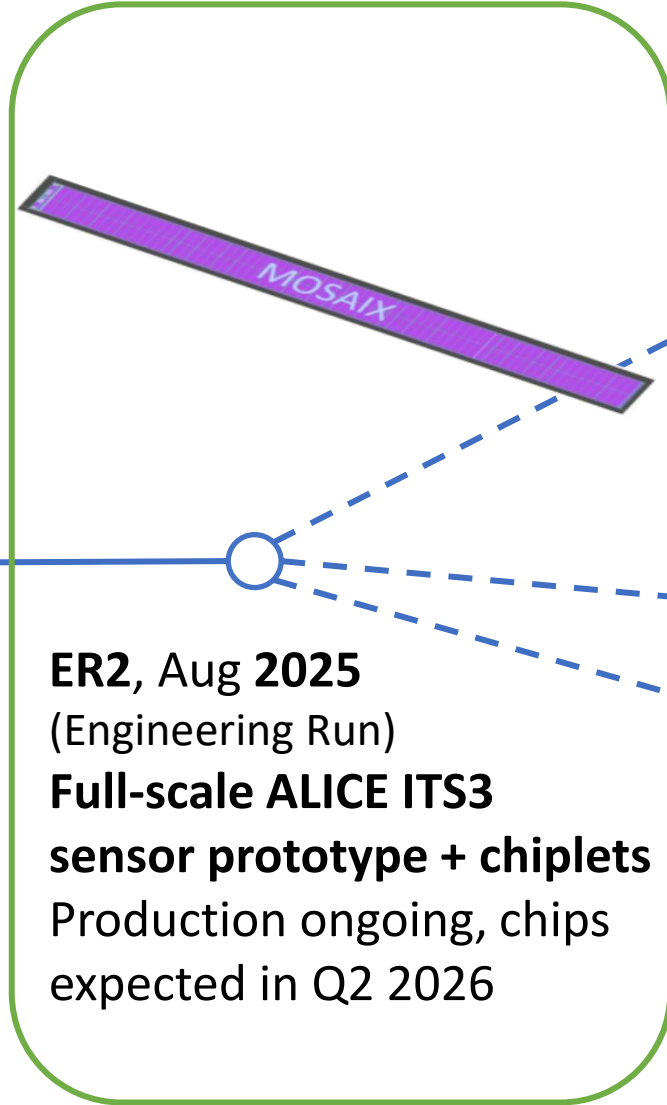
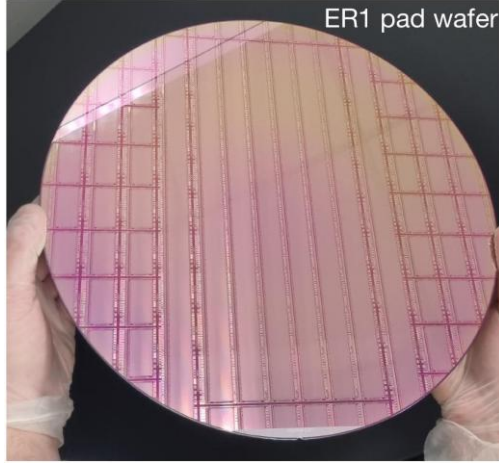
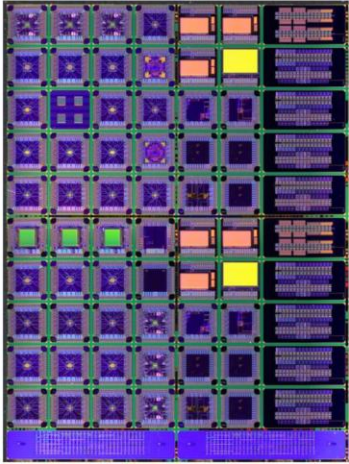


Intermediate goal: beam telescope upgrade

- Sensor R&D adopting a multi-staged approach
- Intermediate sensor fulfilling only a **subset of final demonstrator's specs**
 - **Relaxed** requirements on **time resolution**, **radiation tolerance**, and **power consumption**
- Target application: **reference detectors for beam test measurements**



OCTOPUS different options



ER2 respin, Q1(?) 2026
Replacement of ER2 mask set
 Possibility to implement
 new sensor layouts

ER3, Q3(?) 2026
Sensor production for ITS3
 ALICE-specific submission,
 possible room for chiplets

MPR2, Q3(?) 2027
 (Multi-Project Run)
Shared engineering run
 Full reticle-size in principle
 available

MLR1, Dec 2020
 (Multi-Layer Reticle)
1.5 × 1.5 mm² chiplets
 First submission in
 TPSCo 65 nm CMOS
 technology

ER1, Dec 2022
 (Engineering Run)
**Wafer-scale sensors +
 chiplets**
 First submission including
 stitched sensors

ER2, Aug 2025
 (Engineering Run)
**Full-scale ALICE ITS3
 sensor prototype + chiplets**
 Production ongoing, chips
 expected in Q2 2026

A simulation flow to accelerate the design

SYNOPSYS®

+



+

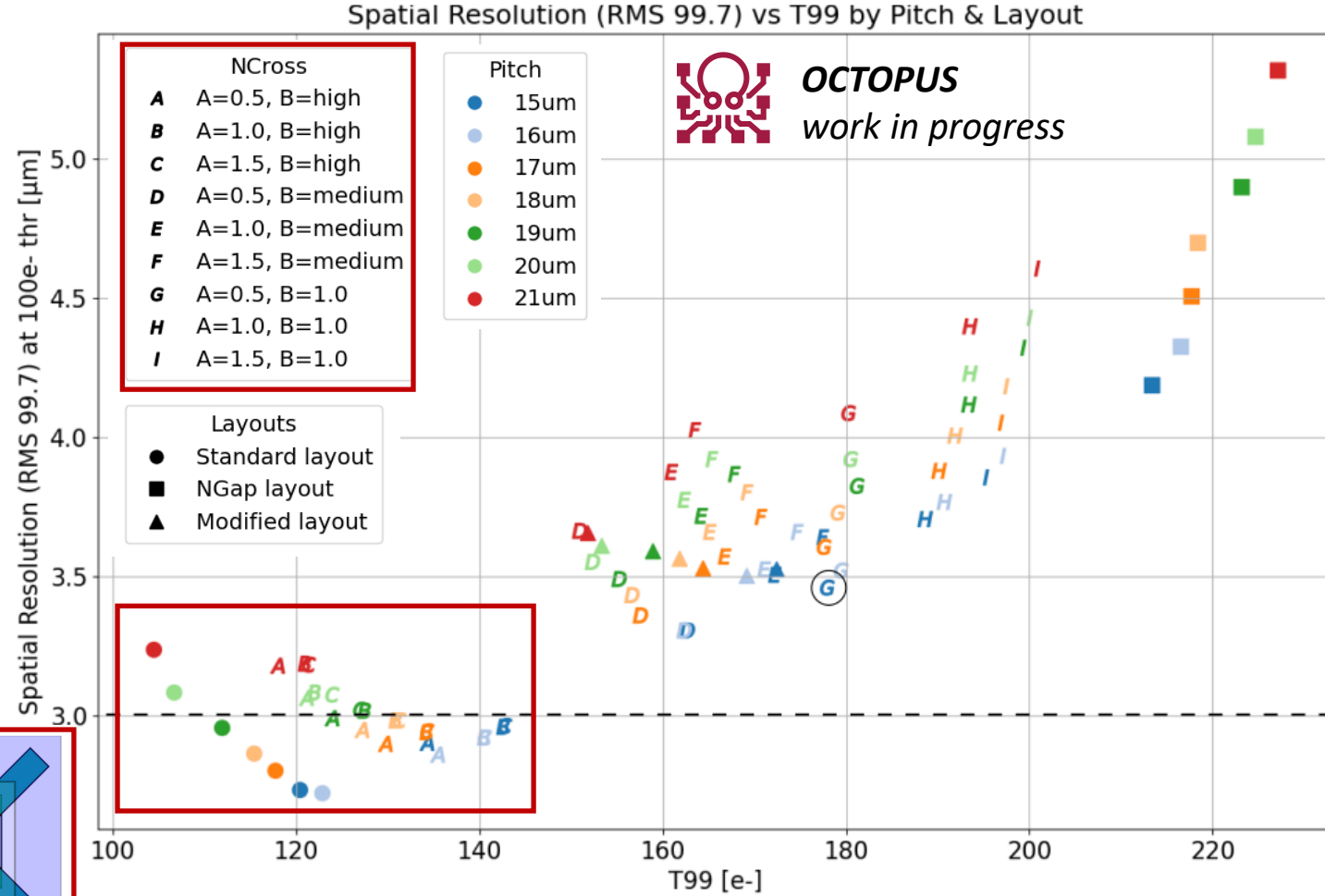
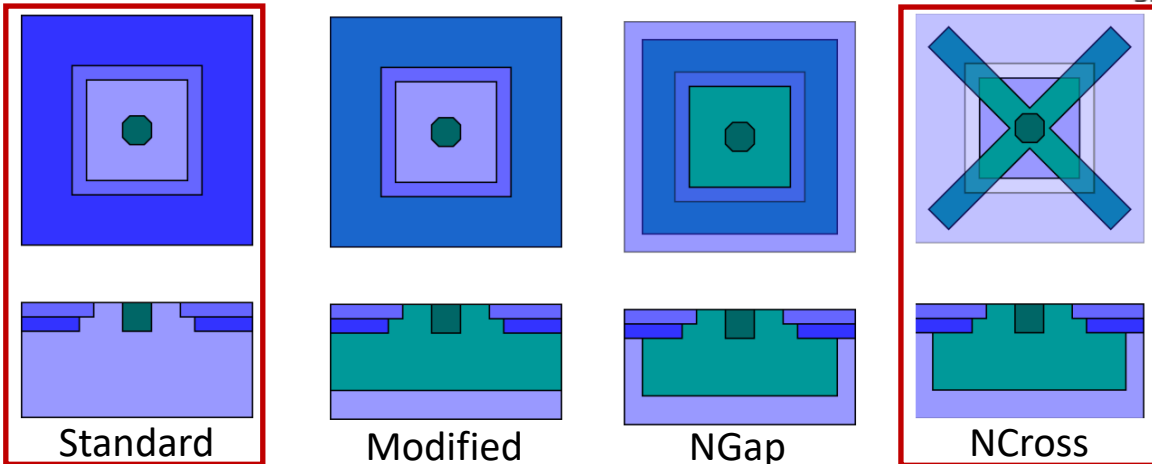


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Key4hep

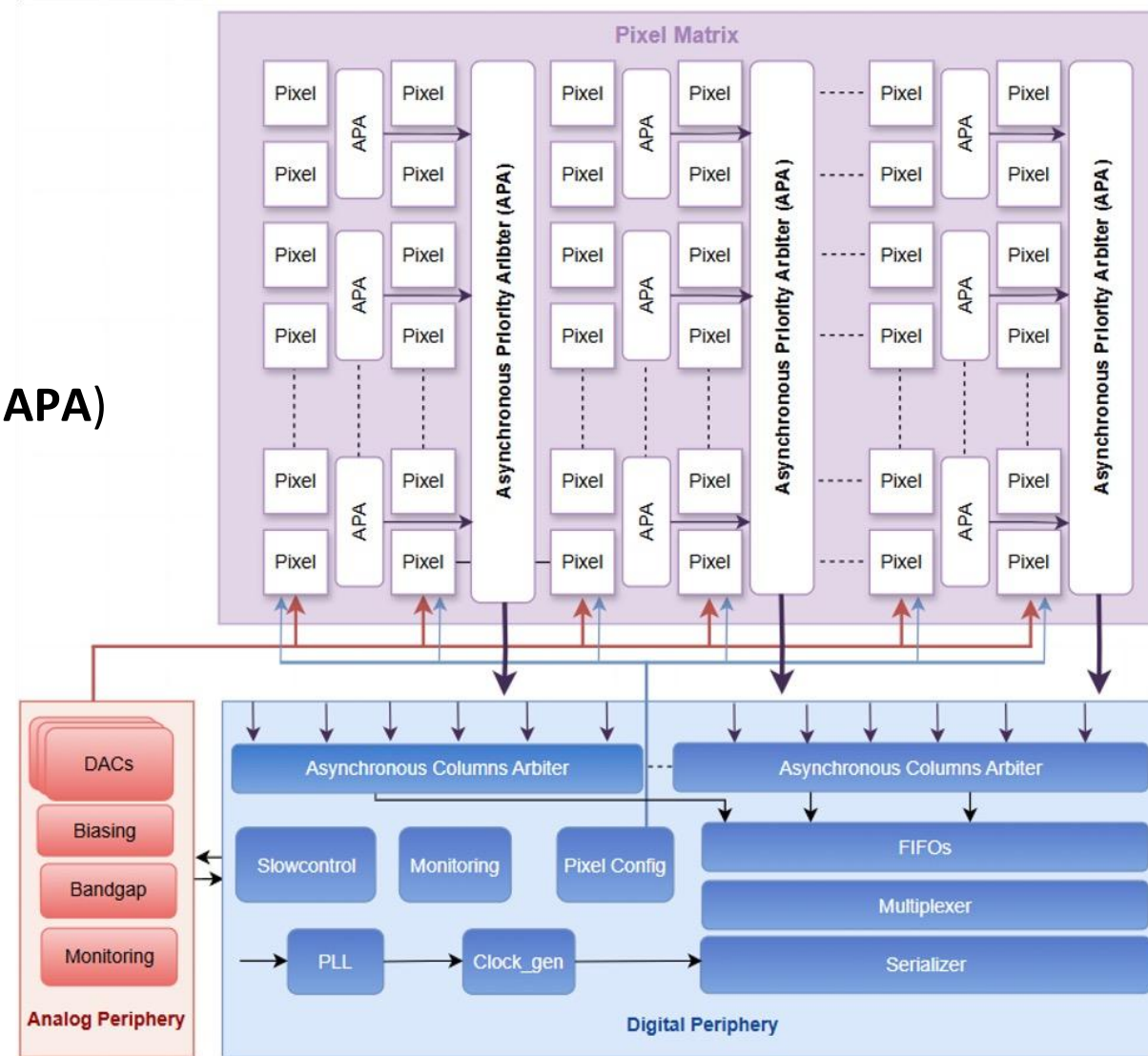
- **Full-stack simulation pipeline** from the particle interaction with the sensor to the chip digital output, and from the single chip to the entire detector
 - Optimization of sensor layout design for MAPS in 65 nm CMOS technology
 - **Synopsys Sentaurus TCAD**: sensor layout and electrical properties
 - **Allpix²**: radiation-matter interaction, charge transport, signal induction, integration with SPICE simulators to include analog front-end
 - Modelling of circuit-level readout behaviour
 - **PixESL**: Very Front-End (VFE), periphery, data aggregation
 - Connection to performance of future vertex detectors
 - **Key4hep** : full detector simulation from event generation to analysis

- **Two layout options to reach 3 μm resolution target at pixel pitch $\leq 20 \mu\text{m}$**
 - Standard
 - **NCross**: novel layout with cross-shaped low dose n-type implant
- Include **analog test chiplets** implementing **NCross layout in next TPSCo 65 nm submission** (ER2 respin/ER3)



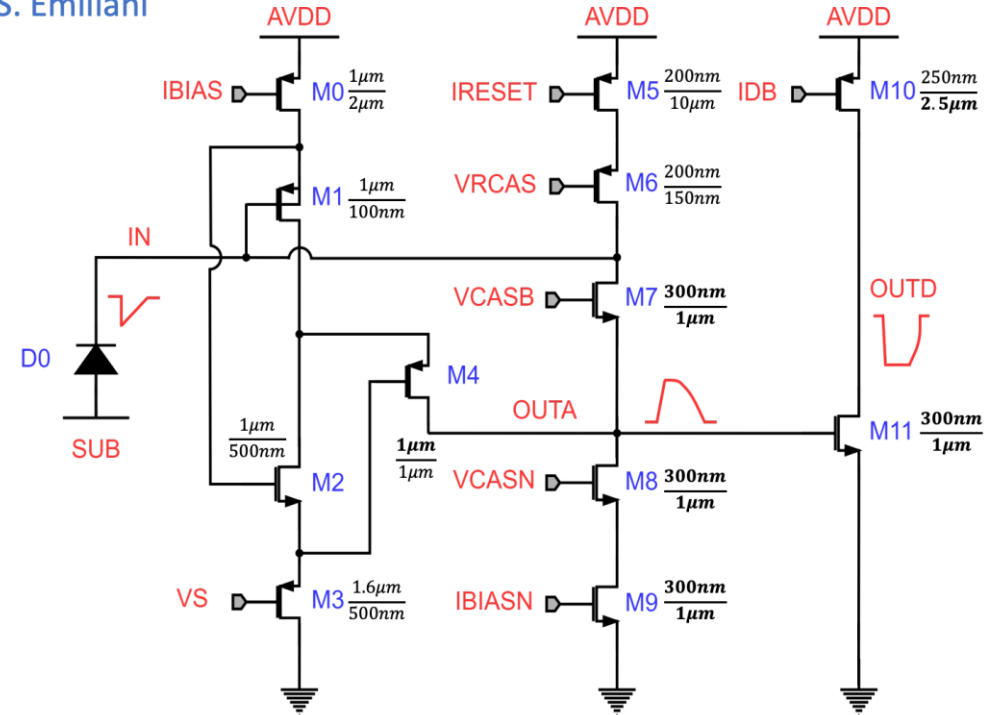
More details in Anastasiia Velyka's [talk](#) (WG4)

- Matrix of **1024 rows × O(1400) columns**
 - Pixel pitch $\leq 20 \mu\text{m}$
 - Matrix of $2.05 \text{ cm} \times \sim 2.8 \text{ cm}$
 - Plus chip periphery
- Active matrix with minimal intelligence
 - Compact in-pixel analog front-end
- Matrix readout based on **Asynchronous Priority Arbiter (APA)** with pixel grouping
 - **Asynchronous readout:** no clock in matrix
 - Compact scheme to fit in $\leq 20 \mu\text{m}$ pitch
- Column merging and time stamping with TDC at the end of column (EOC)
- All biasing from the bottom of the chip



- Requirements:
 - Spatial resolution: compact footprint
 - Temporal resolution: peaking time < 100 ns
 - Total power consumption: 50 mW/cm² → ~ 0.2 μW/pixel
- Sample signal rising and falling edge to retrieve **ToT information**
 - Charge weighting** in cluster reconstruction for spatial resolution
 - Time walk correction**
- Front-end architectures under consideration:
 - DPTS-like
 - MOSAIX-like
 - Alternative front-end proposal

S. Emiliani

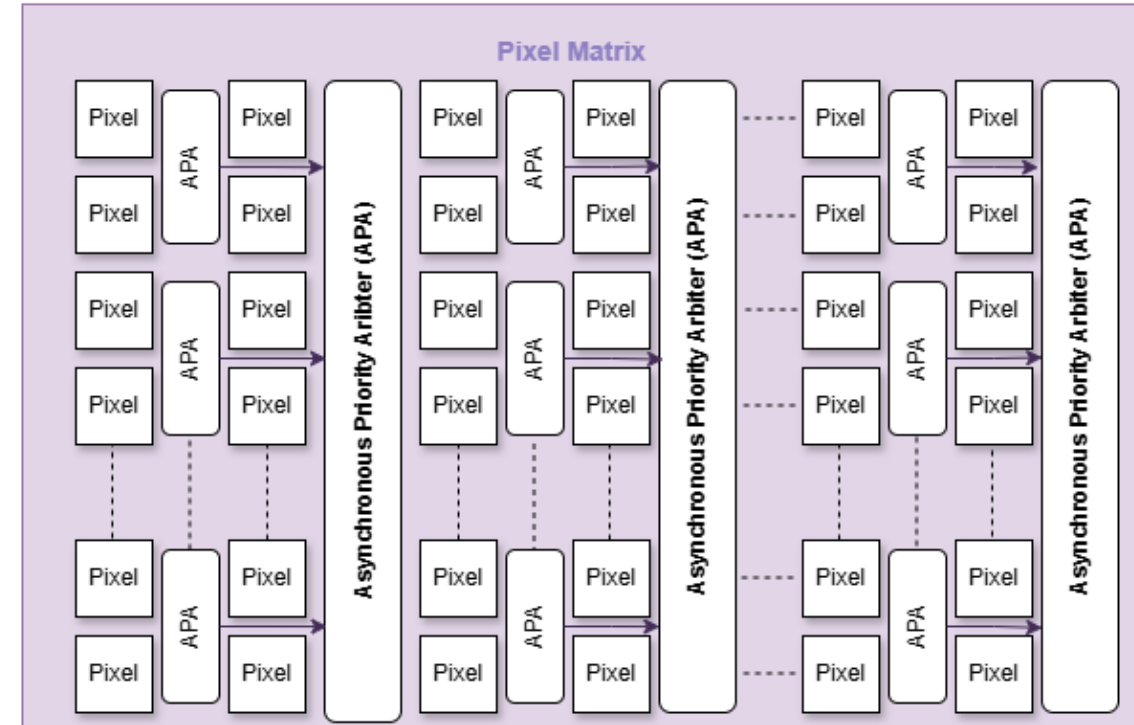


MOSAIX front-end

(<https://indico.cern.ch/event/1461789/>)

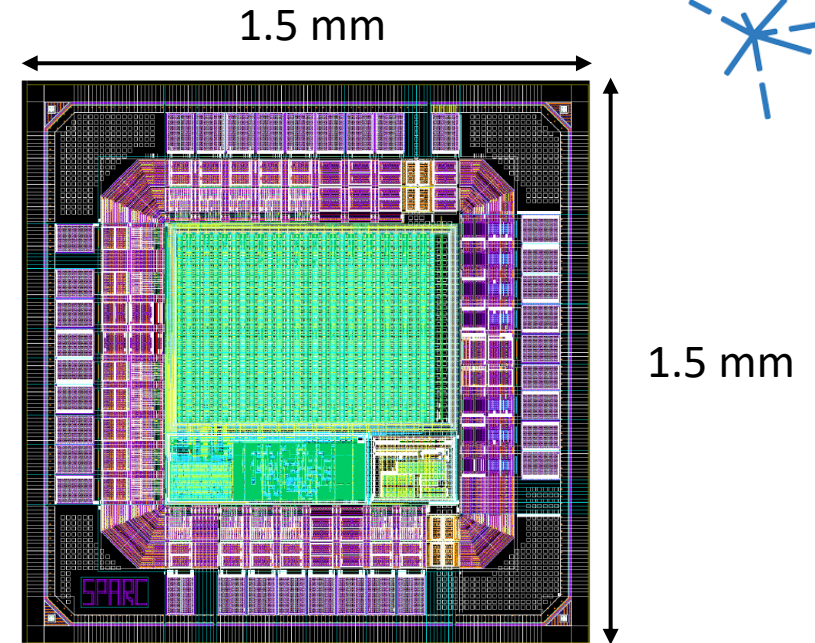
DPTS characterization: [doi:10.1016/j.nima.2023.168589](https://doi.org/10.1016/j.nima.2023.168589)
 DPTS front-end: [doi:10.1109/TNS.2023.3299333](https://doi.org/10.1109/TNS.2023.3299333)

- Pixels grouped in double columns
- **Hits** are **propagated** via **APA** tree to the periphery - receiver unit - **asynchronously** (no time stamping clock)
- **SPARC** chip (TPSCo 65 nm ER2 submission, August 2025) is **proof of concept** of MAPS matrix based on such **asynchronous readout architecture**

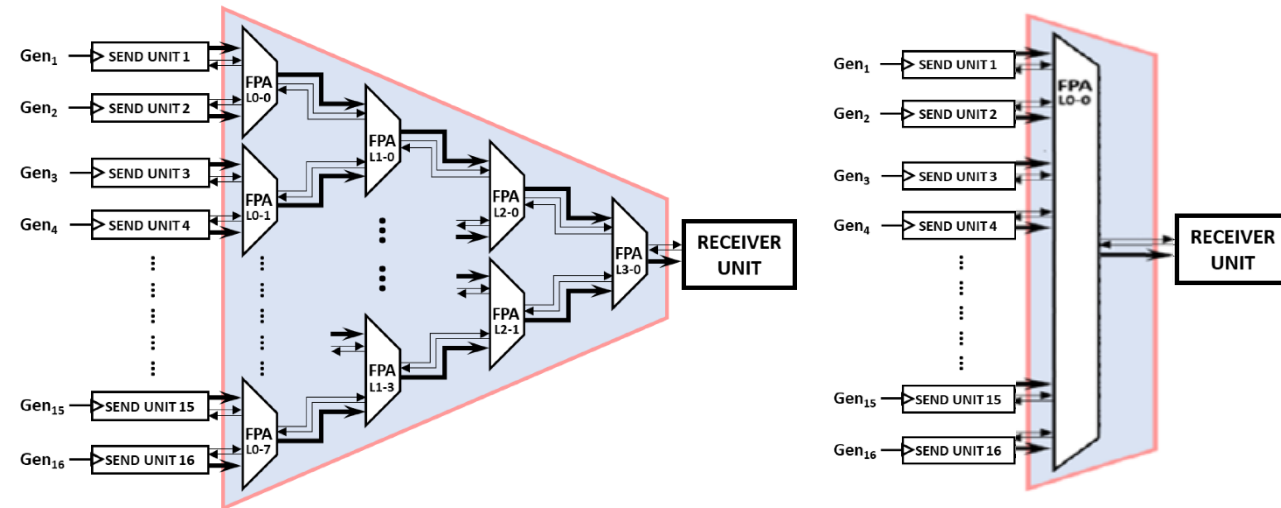


Asynchronous matrix read-out architecture concept:
[doi:10.1016/j.nima.2024.169663](https://doi.org/10.1016/j.nima.2024.169663)

Interlude: the SPARC chip



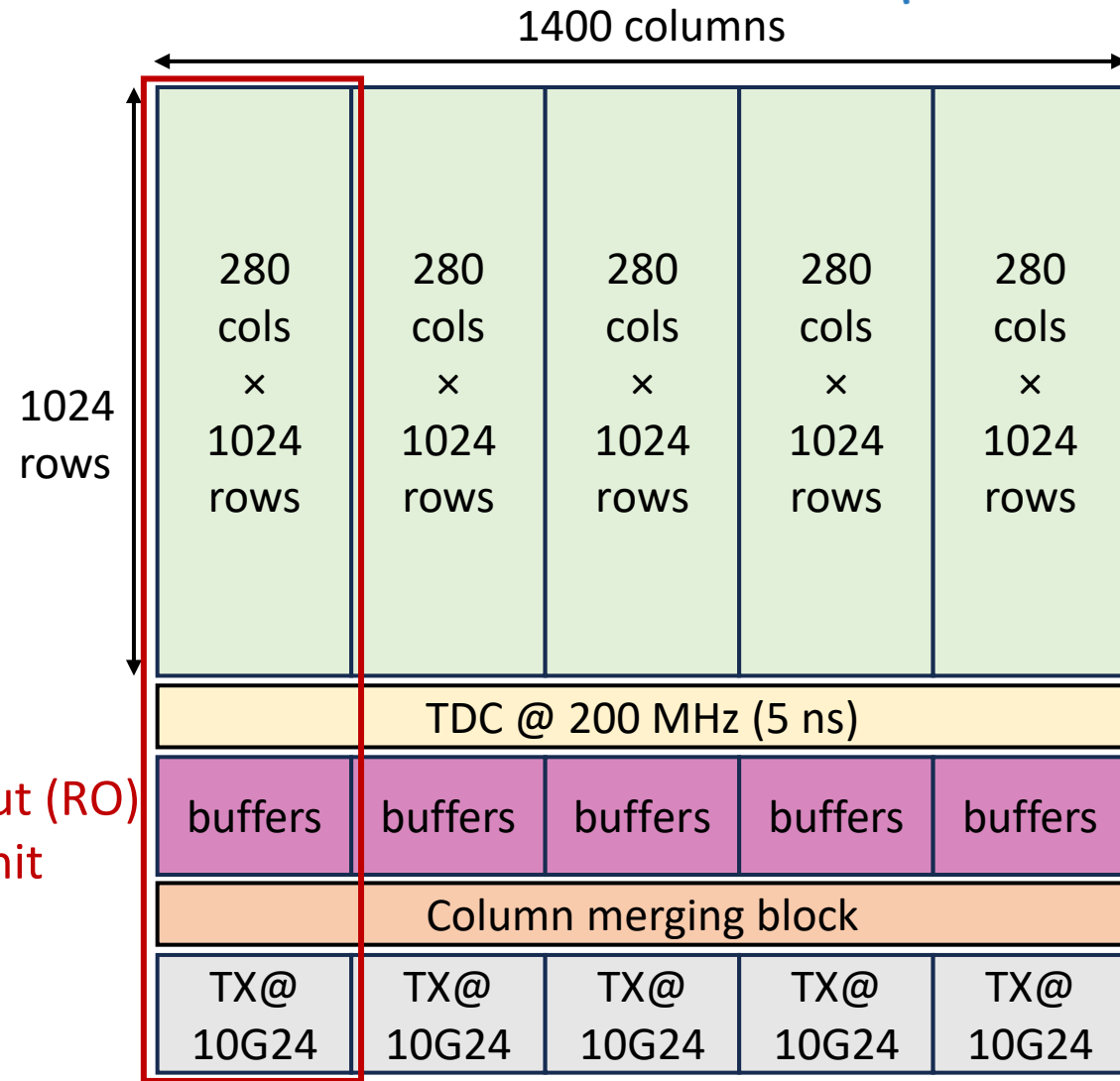
SPARC chip layout



Functional structures of 2:1 and N:1 APA tree types

- **S**ensor **P**ixel **A**synchronous **R**eadout **C**MOS
- Test the feasibility of asynchronous matrix readout in MAPS
 - Pixel matrix: 32×28
 - Pixel pitch: $24 \mu\text{m} \times 16 \mu\text{m}$
 - Pixel front-end: DPTS-like (CERN)
 - APA tree types: 2:1, 4:1, 16:1, 64:1
 - Designed by: IPHC, IRFU
 - Submission: ER2 (summer 2025)
- Simulations show **few ns** of **reading speed** and less than **10 mW/cm²** of **power density**
- Extensive characterization campaign starting in 2026
 - Evaluate the better tree topology
 - Test timing performance
 - Test hit rate capability

- **End of column (EOC) structure:**
 - **5 ns TDC** precision for time stamping (TS)
 - **Buffering** of hits
 - Buffer depth crucial design parameter
 - **Column merging logic**
 - **Time stamp (TS) and hit address** encoding in **hit word**
 - **High speed link**
 - **10.24 Gbps IpGBT-like transceivers (TX)** are the preferred option
 - ❖ Desire to reuse MOSAIX on-chip IpGBT coder and TX@10G24
 - **Data frame sent out at 40 MHz (25 ns)**
- Set of columns grouped and read out by a TX defines a **readout (RO) unit**
- Focus of RO unit design on **data transfer efficiency**



Possible proposal of OCTOPUS chip

- Three column merging concepts being investigated:

1. APA

- RO unit divided in subunits **read out by Async Priority Arbiters (APA)**
- Requires 6-bit column address in hit data word
- Each RO unit always sends an hit, even if idle

2. ROW

- RO unit **read out sequentially (by row)**
- No column address in hit data word
- For each readout cycle, a TX frame is filled with a certain number of buffer words, even if idle

3. ROWZeroSuppr

- RO unit **read out sequentially (by row) with zero suppression**
- Reading only active columns without column address:
 - Words with occupancy (Full/Empty column) information sent out first
 - Then only words of hit data from full columns

lpGBT-like TX data frame

H	Data 192b								FEC 12	LM	
6b	W	W	W	W	W	W	W	W	spare bits	48b	10b

Col Addr	Row Addr	Time Stamp	R/F
6b	10b	10b	1b

APA hit data word

Row Addr	Time Stamp	R/F
10b	10/11b	1b

ROW hit data word

H	Left/Right	Column occupancy
1b	1b	20/21b

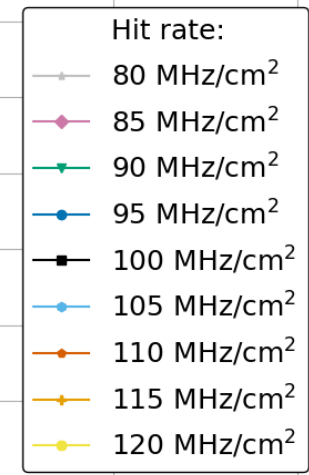
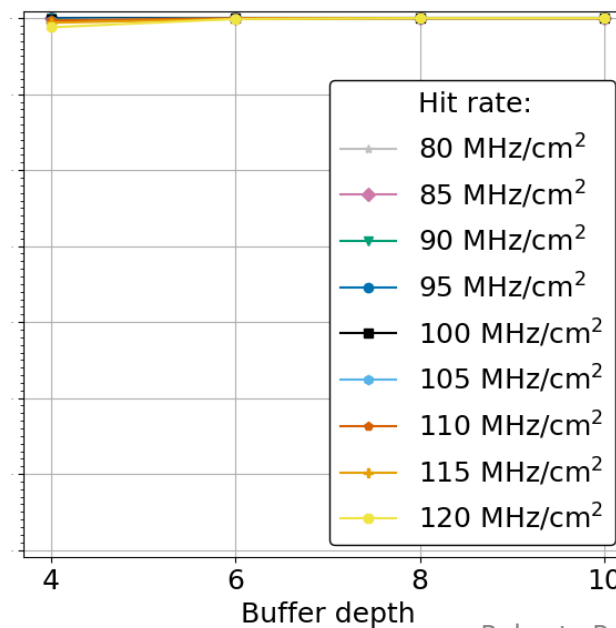
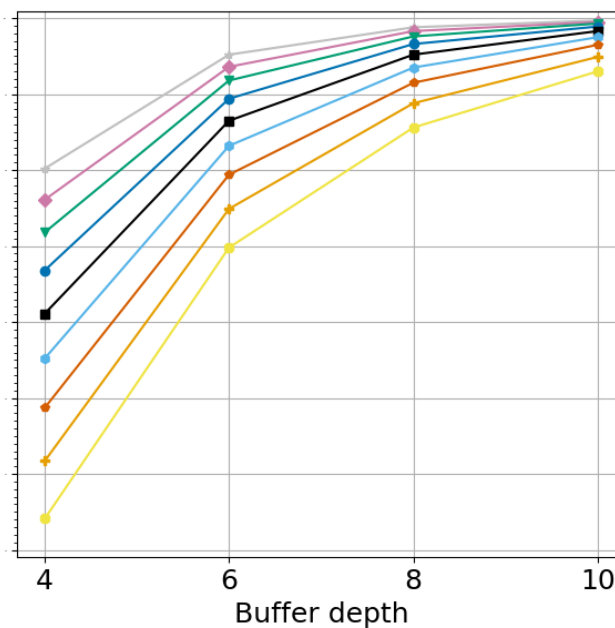
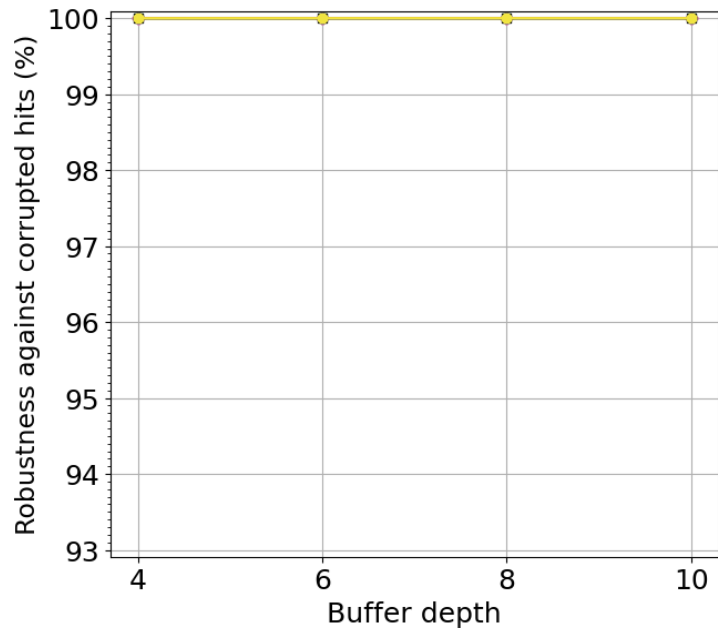
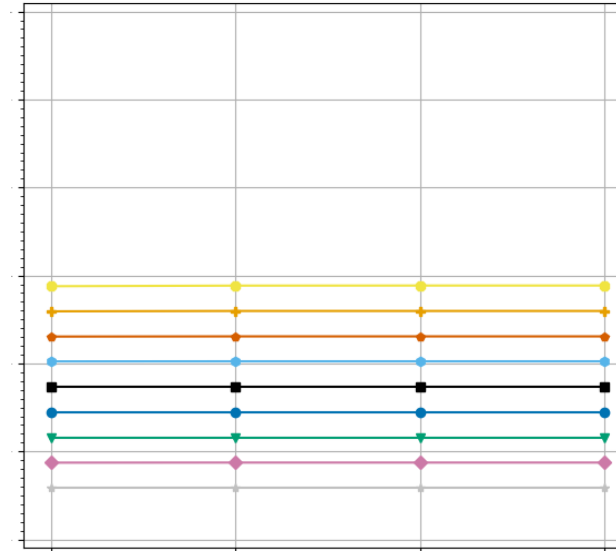
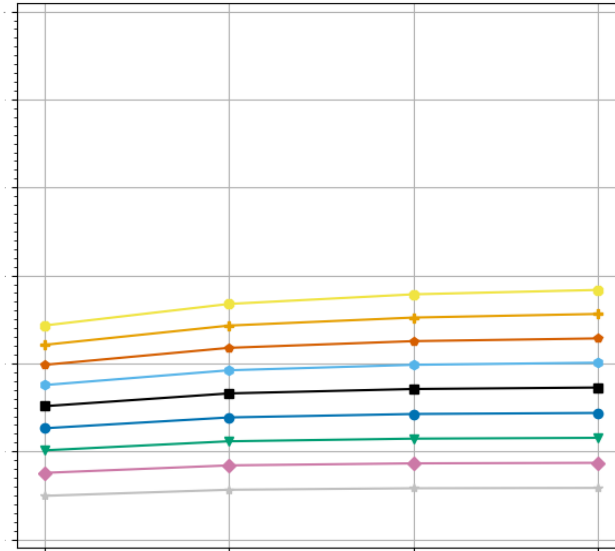
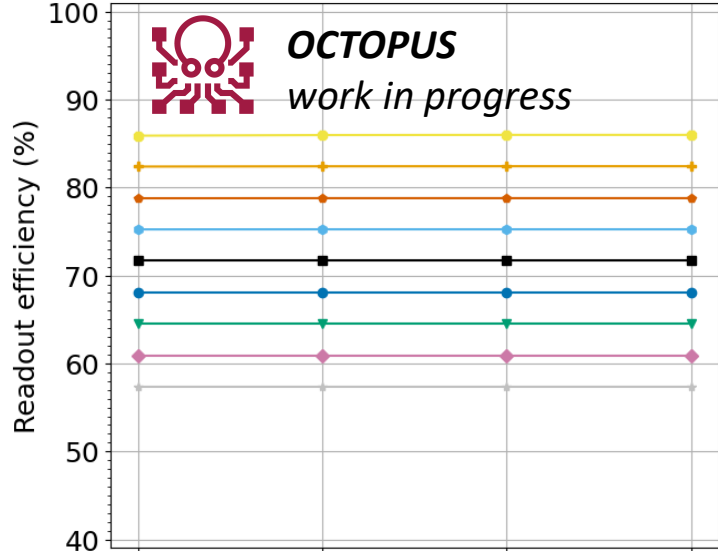
H	Row Addr	Time Stamp	R/F
1b	10b	10/11b	1b

ROWZeroSuppr column occupancy and hit data words

APA

ROW

ROWZeroSuppr



- The **OCTOPUS** project aims to develop **fine-pitched MAPS** based on **65 nm CMOS** technology
- R&D driven by key requirements of vertex detectors operating in the **next generation of lepton colliders**
- Design strategy for the first OCTOPUS chip:
 - **Compact analog in-pixel front-end**
 - Matrix readout implementing **Asynchronous Priority Arbiter (APA)** architecture
 - End of column (**EOC**) time stamping via **TDC** with **column merging logic**
- Common design approach and **synergy with MANTA project** (see Michael Deveaux's [talk](#), WG1)
- Ongoing activities & next steps:
 - Finalization of EOC high-level modelling and kick-starting RTL design
 - Summary report on characterization of results of prototypes in TPSCo 65 nm CMOS process being finalized
 - Contribution to SPARC testing
- ❖ Plans for the next submissions in TPSCo 65 nm CMOS process:
 - ER2 respin/ER3 (2026): analog test structures with NCross layout, optimized analog front-end, EOC architecture
 - MPR2 (2027?): full readout unit

And an announcement...

7th Allpix² User Workshop

28 - 30 April 2026

MBI-ÖAW, Vienna, Austria

Abstract Deadline: 23 March 2026

Registration Deadline: 15 April 2026



Organisers

Brigitte De Monte

Håkan Wennlöf

Paul Schütze

Sebastian Onder

Simon Spannagel

Thomas Bergauer

allpix-quared-workshop@cern.ch



<https://indico.cern.ch/e/apsqws7>



Additional slides

OCTOPUS project
D. Dannheim, S. Spannagel

WP1: Simulations
A. Ilg, A. Velyka

WP2: ASIC design
F. Guezzi, L. Huth,
S. Senyukov

WP3: Data Acquisition
Y. Otariid

WP4: Testing and characterization
F. King, M. Franks

System Demonstrator (DRD8)

Task 1:
Sensor optimization/
TCAD

Task 1:
Sensor and
pixel front-end design

Activity 1:
Caribou 2.0 development

Task 1: Summary of
current 65 nm CMOS
demonstrator results

Activity 1:
Concept, design of
mechanics & cooling

Activity 1:
Allpix² development

Task 2:
Matrix architecture and
readout design

Task 1:
Chipboard design for
prototypes

Task 2:
Lab characterization, FE
optimization, calibration

Activity 2:
Design & construction of
beam telescope

Task 2:
Detector performance/
Allpix²

Task 3:
Periphery, DACs and
slow control

Task 2:
FW & SW integration
of prototypes

Task 3: Beam test
characterization,
simulation comparison

Activity 3:
Prototype construction

Activity 2:
Physics performance/
Geometry optimization

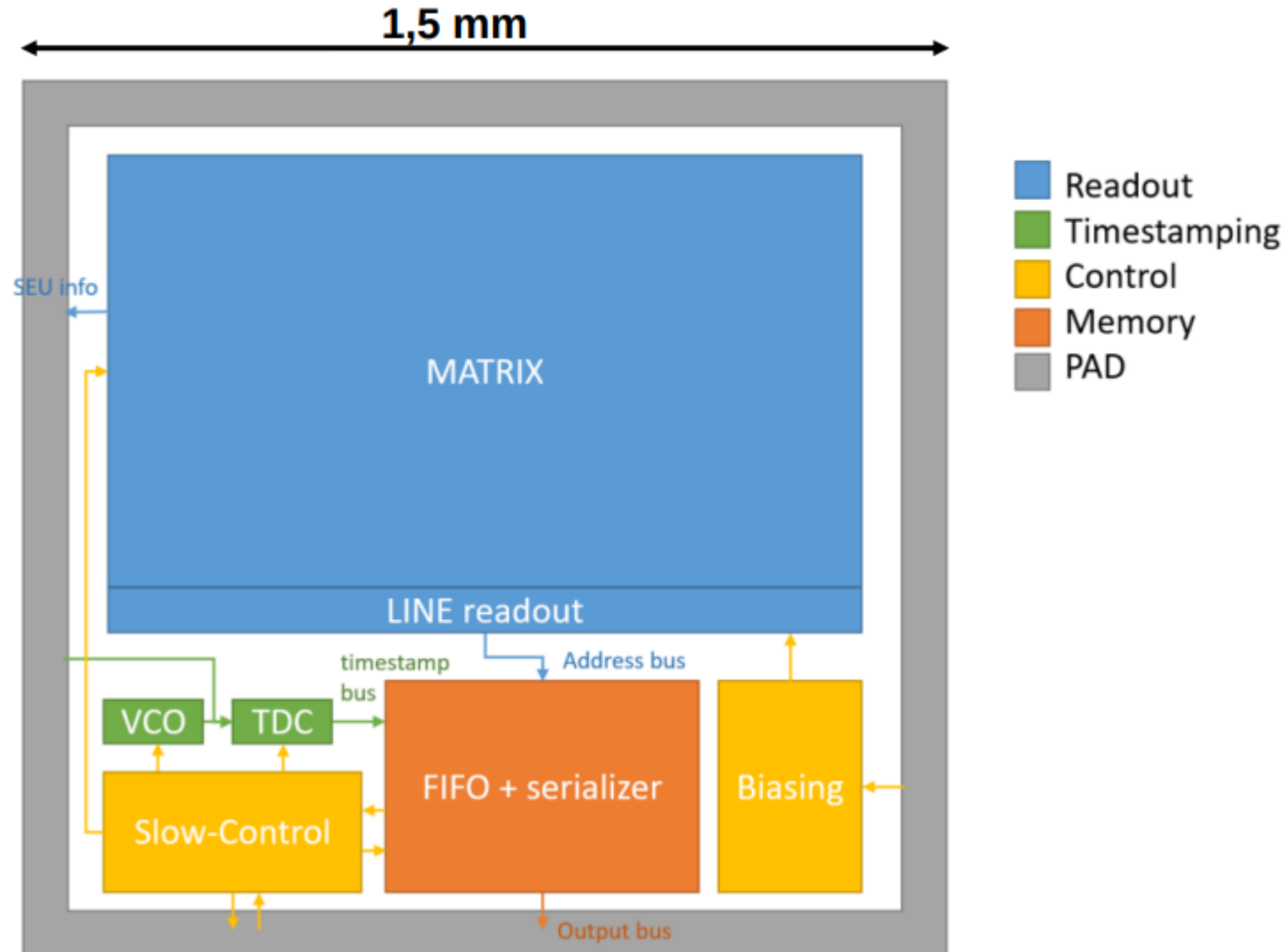
Task 4:
Transceivers and
readout design

Task 3:
Chip/board assembly,
bonding & logistics

Activity 1:
Sensor irradiation &
testing

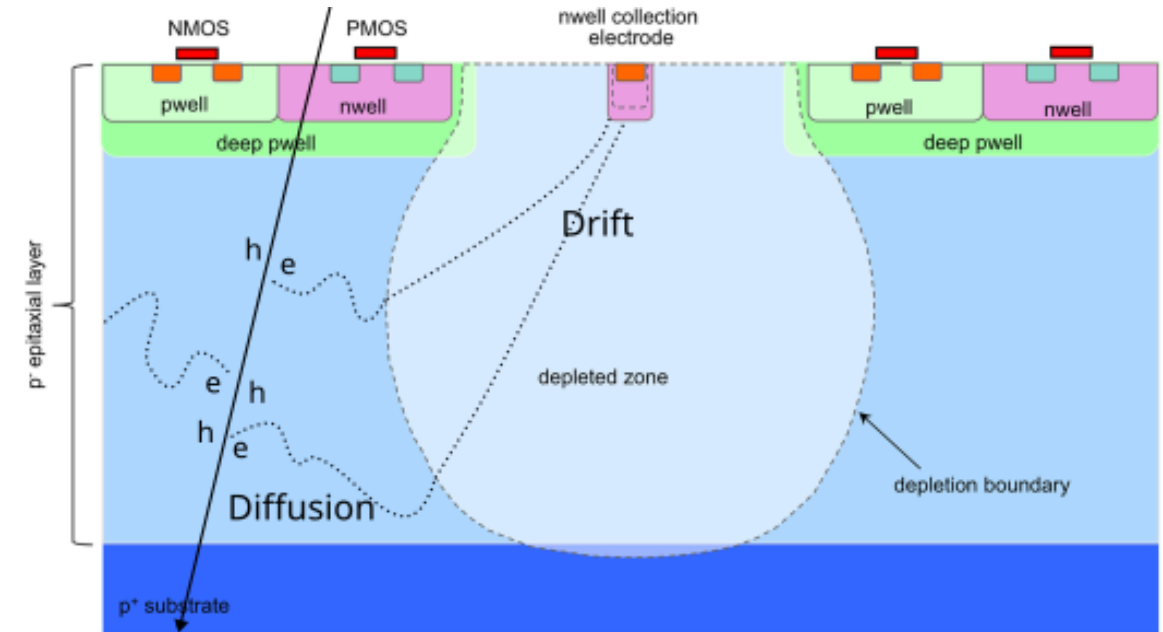
Activity 1:
Submission coordination
and DRD7 liaison

- Matrix
 - 32 rows × 28 columns
 - End-of-Column (EoC) readout with Asynchronous Priority Arbiter (APA)
- Timestamping
 - VCO (~2 ns) and grey code TDC
- FIFO and serializer
 - Double port FIFO
 - Input Asynchronous
 - Output Synchronous
- Slow control
 - Serial Peripheral Interface (SPI)
 - 16 registers of 8 bits (2 hard coded)
- Biasing
 - Provide pixel biasing from pads



- **Standard process**

- Small n-well collection electrode on high-resistivity p-type epitaxial layer
- Reverse substrate bias applied to increase depleted zone
- Sensitive epitaxial layer partially depleted
- Part of signal charge collected from the non-depleted layer via diffusion
- Operational up to 5 kGy TID and $1.7 \times 10^{13} \text{ 1 MeV n}_{\text{eq}} \text{ cm}^{-2}$ NIEL fluence

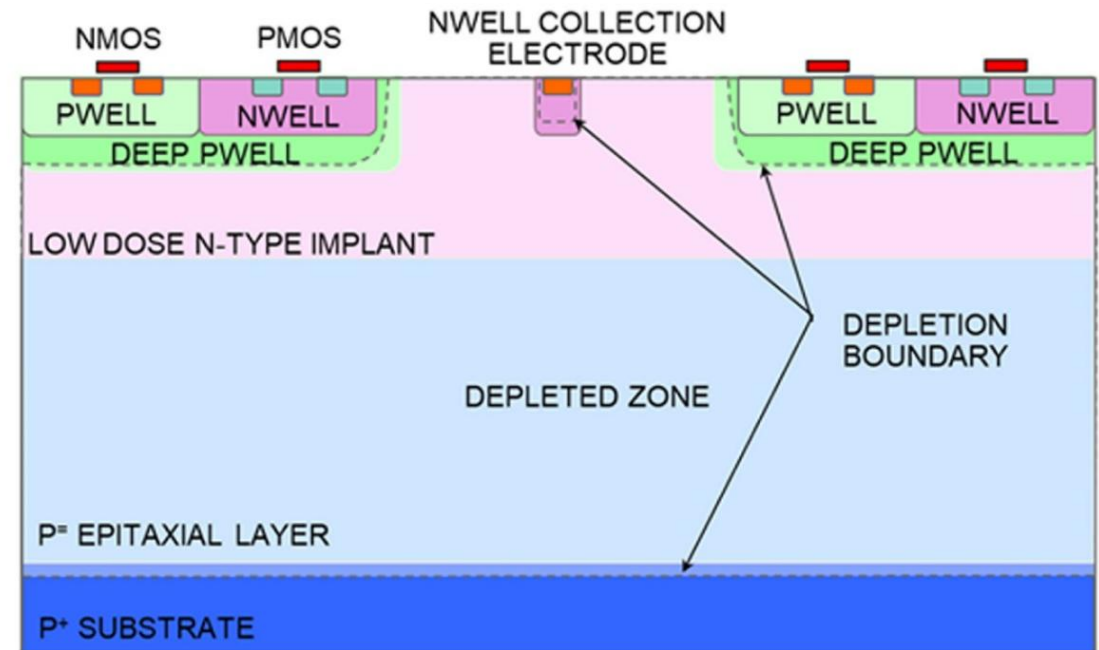


Optimization of 65 nm CMOS process:

[doi:10.22323/1.420.0083](https://doi.org/10.22323/1.420.0083)

- **Modified process**

- Addition of a low-dose n-implant below the electrode
- Extends the junction to fully deplete the epitaxial layer
- Weak lateral electric field at pixel edges and corners
- MALTA collaboration observed loss of detection efficiency at pixel corners for 180 nm CMOS sensors irradiated with $1 \times 10^{15} \text{ 1 MeV } n_{eq} \text{ cm}^{-2}$ NIEL ([doi:10.1016/j.nima.2019.162404](https://doi.org/10.1016/j.nima.2019.162404))



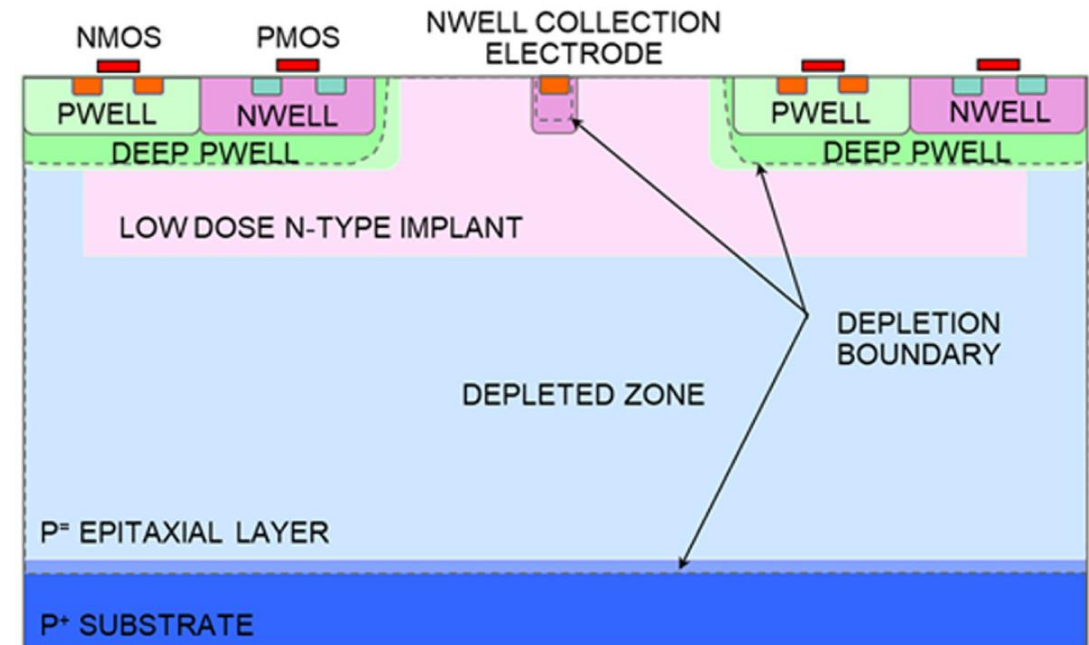
More details in [doi:10.1016/j.nima.2017.07.046](https://doi.org/10.1016/j.nima.2017.07.046)

Optimization of 65 nm CMOS process:

[doi:10.22323/1.420.0083](https://doi.org/10.22323/1.420.0083)

- **Modified with gap process**

- Gap in the n-implant at the pixel borders
- Improves lateral field near the pixel boundary
- Accelerates the charge collection to the electrode and improves the radiation hardness



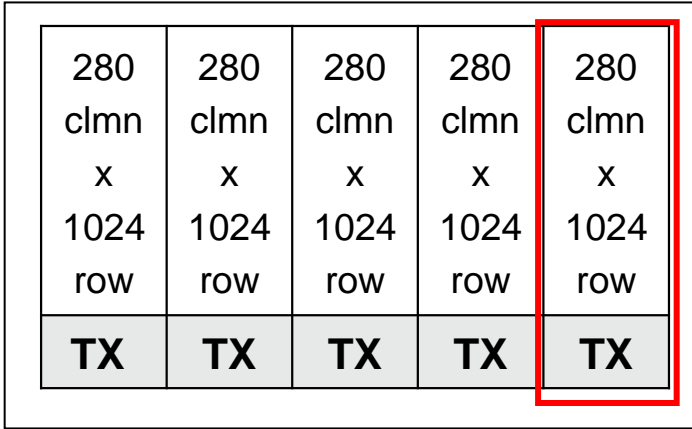
More details in [doi:10.1088/1748-0221/14/05/C05013](https://doi.org/10.1088/1748-0221/14/05/C05013)

Optimization of 65 nm CMOS process:

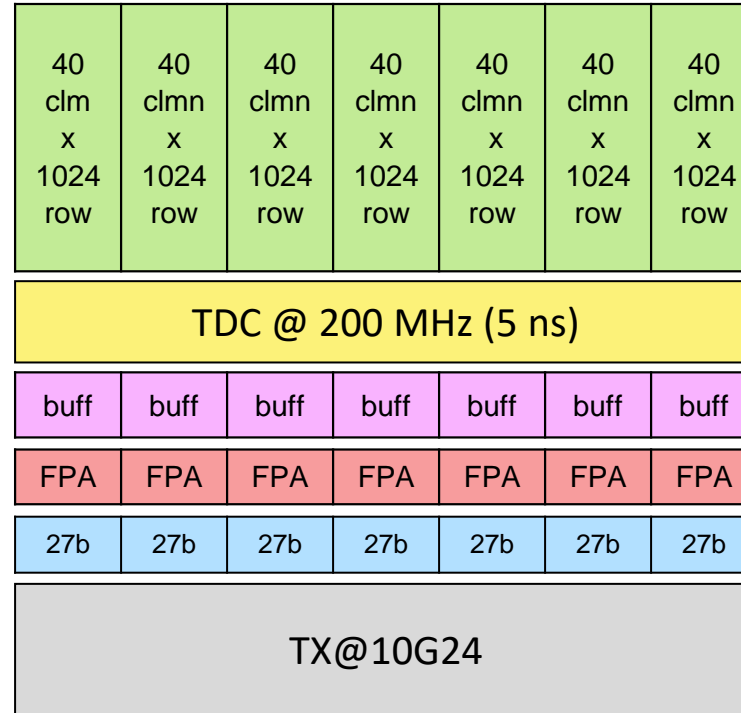
[doi:10.22323/1.420.0083](https://doi.org/10.22323/1.420.0083)

APA readout concept

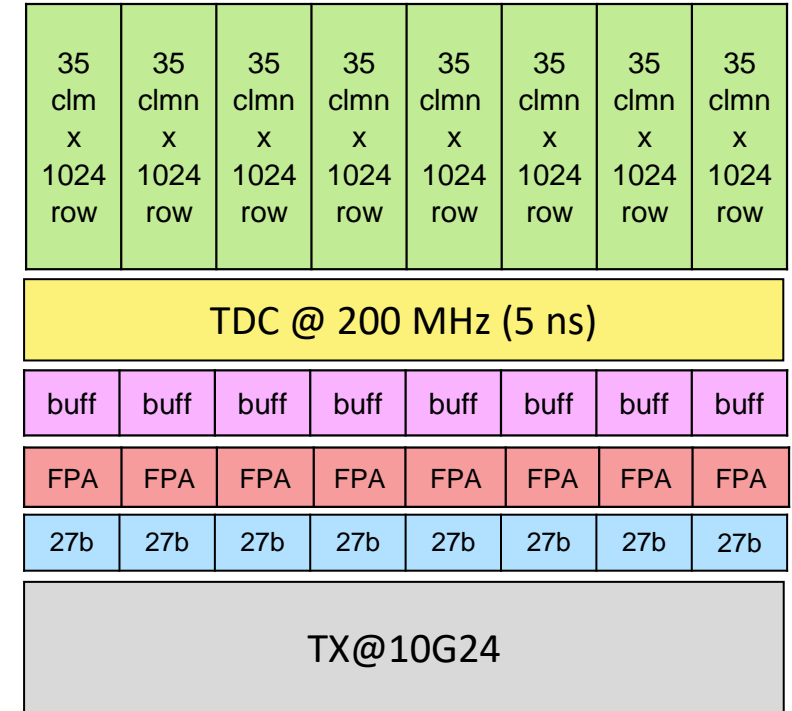
OCTOPUS



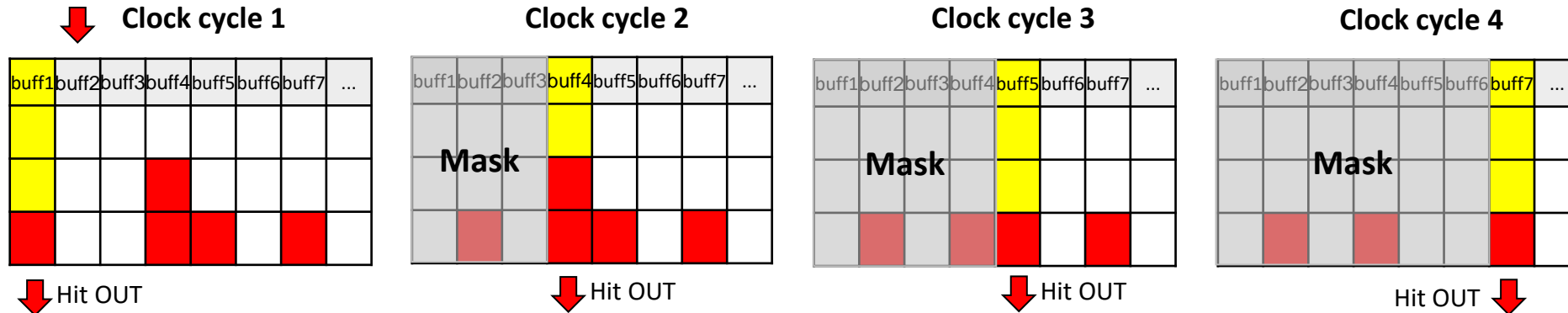
FEC12 (192b)



FEC5 (224b)



- Matrix of 1024 × 1400 pixels
- 5 × readout (RO) unit
- 10G24, FEC12 & FEC5
- FPA with mask
- Hit data word size **h** =
 - $h = 10b$ (row address) + $6b$ (clm address) + $10b$ (timestamp) + $1b$ (R/F flag)



ROWZeroSuppr readout concept

- What's in a subframe?
- Row Zero Suppression block generates 2 occupancy words for the LEFT and RIGHT half of the subunit, respectively
 - Occupancy = word size – 2b -> 2×occupancy= Maximum number of column to be grouped into subunit
 - If less columns, use filler bits in the occupancy word
- Then it sends out full columns word only

H	Data 192b								FEC 12	LM	
6b	W	W	W	W	W	W	W	W	spare bits	48b	10b

H	Left/Right	Column occupancy
1b	1b	20b

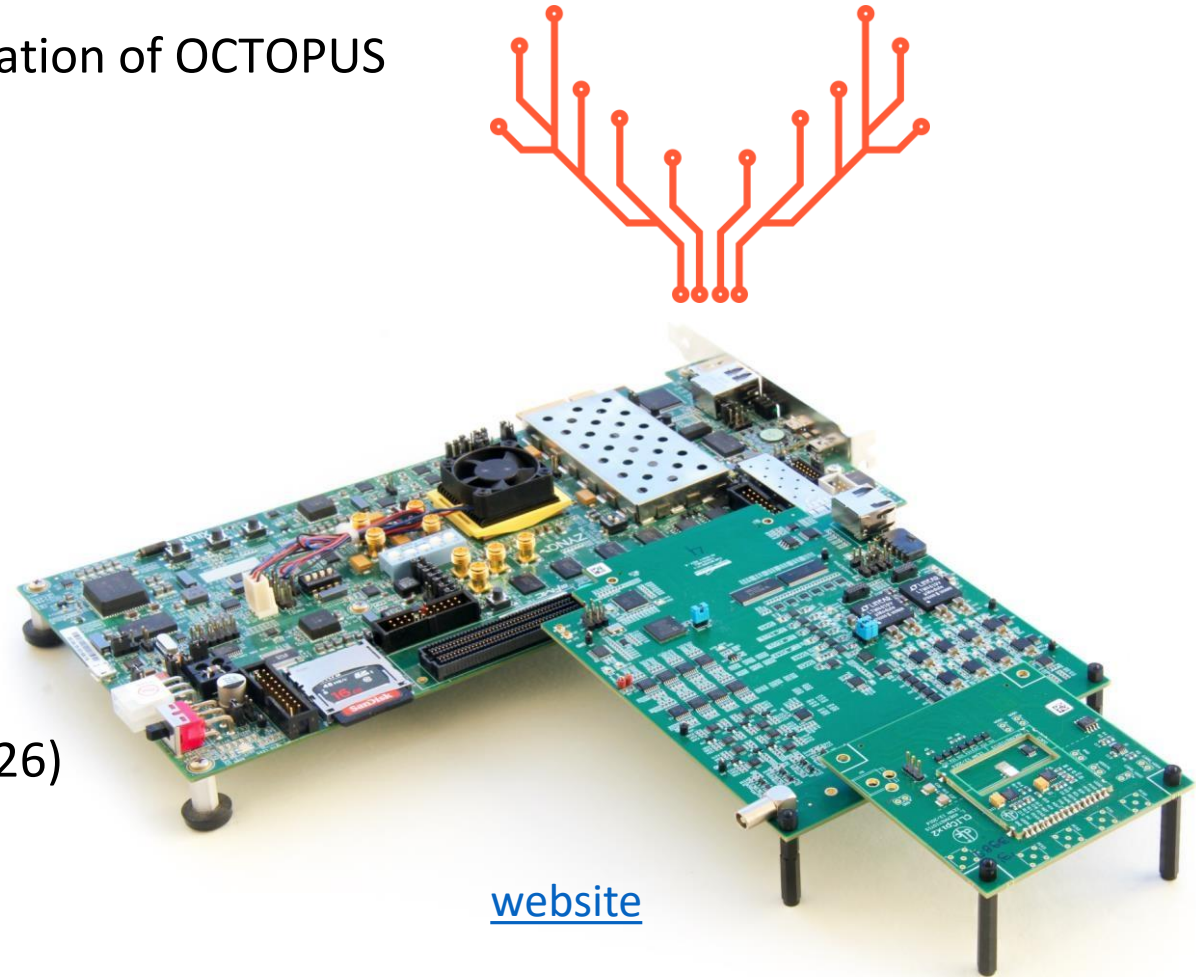
H	Row Addr	Time Stamp	R/F
1b	10b	10b	1b

```

--- Sub-Unit 0 (Columns 0-35) Simulation Log ---
Time(ns)  State      Data
---
15591525  LEFT       000000100110110000
15591550  RIGHT      000110011101000100
15591575  SEND       col=6 (depth=1)
15591600  SEND       col=9 (depth=1)
15591625  SEND       col=10 (depth=1)
15591650  SEND       col=12 (depth=1)
15591675  SEND       col=13 (depth=2)
15591700  SEND       col=21 (depth=2)
15591725  SEND       col=22 (depth=1)
15591750  SEND       col=25 (depth=2)
15591775  SEND       col=26 (depth=1)
15591800  SEND       col=27 (depth=1)
15591825  SEND       col=29 (depth=3)
15591850  SEND       col=33 (depth=1)
15591875  LEFT       000100010001110000
15591900  RIGHT      000101110001000001
15591925  SEND       col=3 (depth=1)
15591950  SEND       col=7 (depth=2)
15591975  SEND       col=11 (depth=1)
---
    
```

- Simulation assumptions:
 - Simulating only one RO-unit
 - 5 million hits per RO-unit simulated at different hit rates ($\pm 20\%$ target hit rate)
- Two metrics used to evaluate readout concepts
 - **Readout efficiency (RE)** = # hit words sent out / (# hit words sent out + # idle words sent out)
 - **Robustness against corrupted hits (RCH)** = $1 - (\text{total lost hits} / \text{total input hits})$
- In the computation of RCH, R and F hits belonging to the same event are considered as independent, i.e. if one of the two is lost the other is not counted as lost

- **Caribou** chosen as DAQ system for the testing and operation of OCTOPUS prototypes and final demonstrator
 - Open source hardware, firmware, and software
 - Already used for lab and beam test operations of other pixel sensor prototypes
 - APTS, DPTS, H2M, etc
- Hardware components:
 - **SoC board**: embedded CPU running DAQ system
 - **CaR board**: power supply, data and control links
 - **Chip board**
- OCTOPUS community will use **Caribou DAQ** already for the **testing** of the **SPARC chip** (starting in 2026)



[website](#)

More details in Younes Otarid's [talk](#) (WG5)