

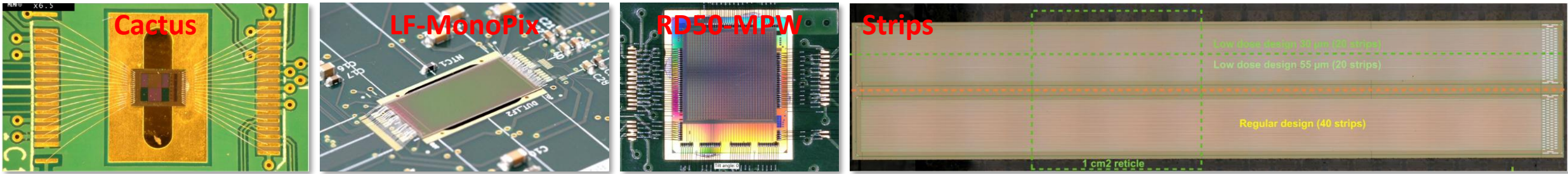
DRD3 Community Shared Submission in LF15A Technology

Eva Vilella, University of Liverpool

- This presentation provides a snapshot of the status of our discussions with LFoundry and the chips interested in joining the submission – Several aspects are not final yet.
- This presentation is scheduled to finish at 14:55 h, and I start teaching at 15:00 h.

Motivation

- 150 nm HV-CMOS from LFoundry is a well-known process in the detector R&D community



Apologies if I have forgotten your favourite 150 nm LFoundry chip

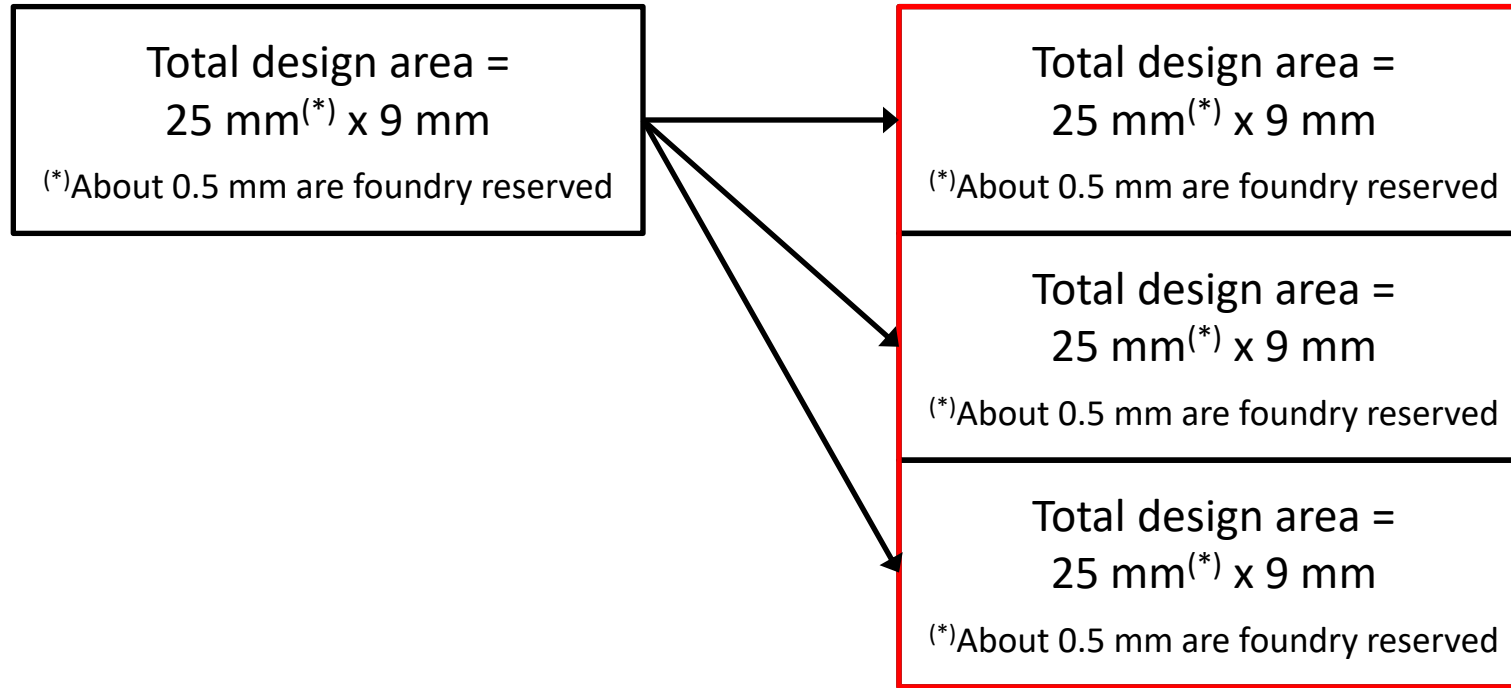
- Challenges**

- Generally, we do small prototypes through Multi-Project Wafer (MPW) submissions, sharing the wafer with chips from other customers within or beyond the community.
- Our designs often come with special requests: post-processing (done at wafer level), special passivation layers, custom-layers, etc.
- It is challenging for the foundry to provide dedicated, one-to-one support for our projects.

LFoundry suggested (in 2023!!) that the detector R&D community collaborate on a joint Multi-Layer Mask (MLM) submission so that they can better support these needs.

Shared submission – 1x3 Multi-Layer Mask (MLM)

▪ What is a 1x3 MLM?



Advantages

- Wafer ownership (easier post-processing)
- Large number of fabricated wafers
- Cost-effective route for sensor prototyping

New challenges

- Submission specifications must be compatible (*e.g.* substrate resistivity, passivation layer, final thickness...)
- Submission date must be acceptable by all chips
- Composition of final design area + DRC errors feedback
- Payment through one-single customer (no invoice split)

New challenges

Submission specifications

- We have done a thorough check, and there is compatibility

Submission date

- We have proposed March 2026 to LFoundry, although the date has not been confirmed for now
- In principle, the date is acceptable by all interested chips (however, see following slides)

Final design area + DRC errors feedback

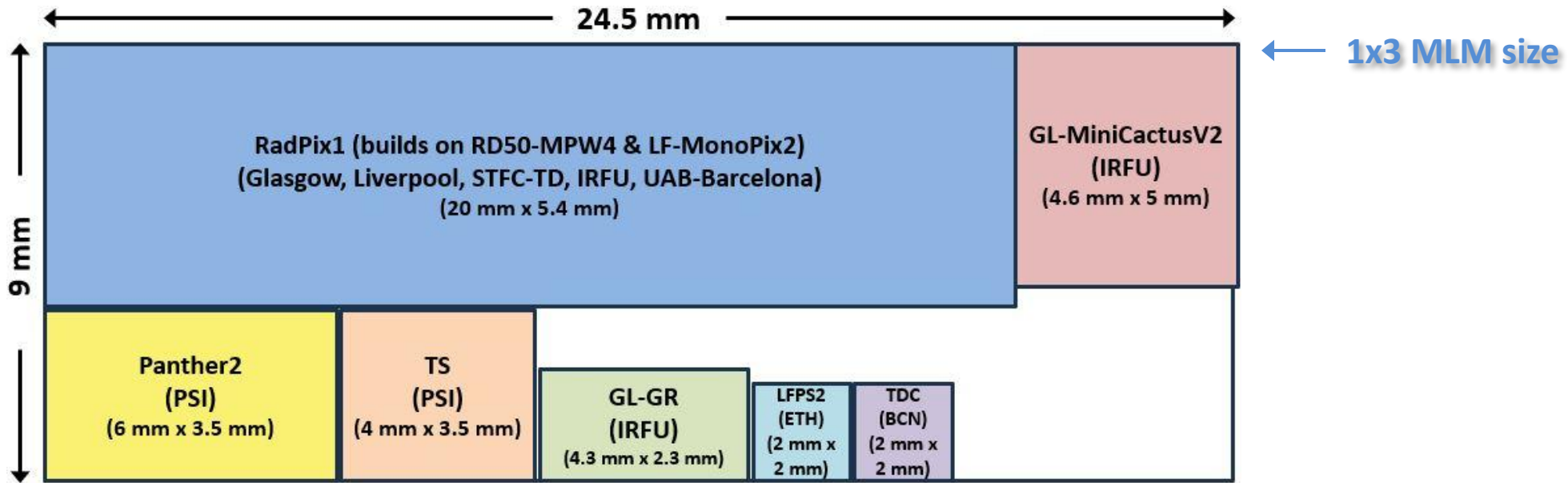
- Teams designing the proposed chips are small; they do not have the resources to do this
- We have proposed to LFoundry that they take care of composing the final design area and providing the DRC errors feedback to the teams (currently expecting an answer)

Payment through one-single customer

- We have spoken with CERN Procurement and they are supportive of this

Interested chips (I)

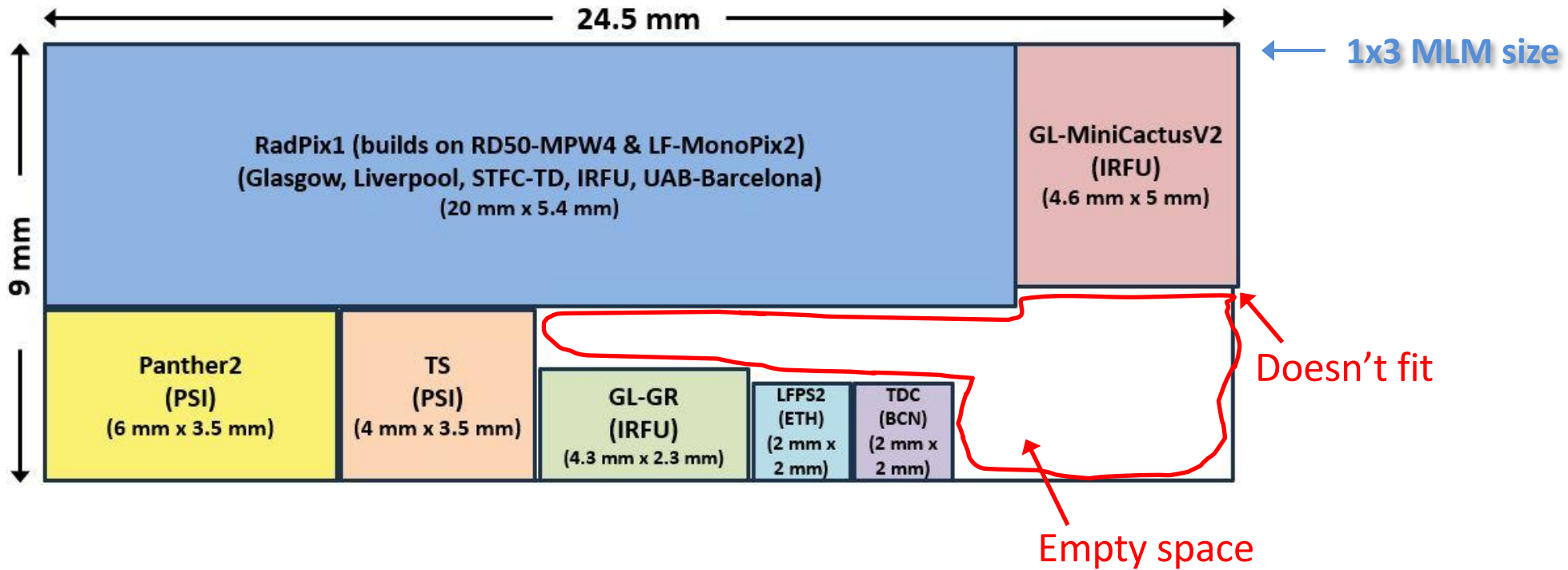
Preliminary



Chip name
(chip design effort)
(X mm x Y mm) = (Horizontal mm x Vertical mm)

Interested chips (I)

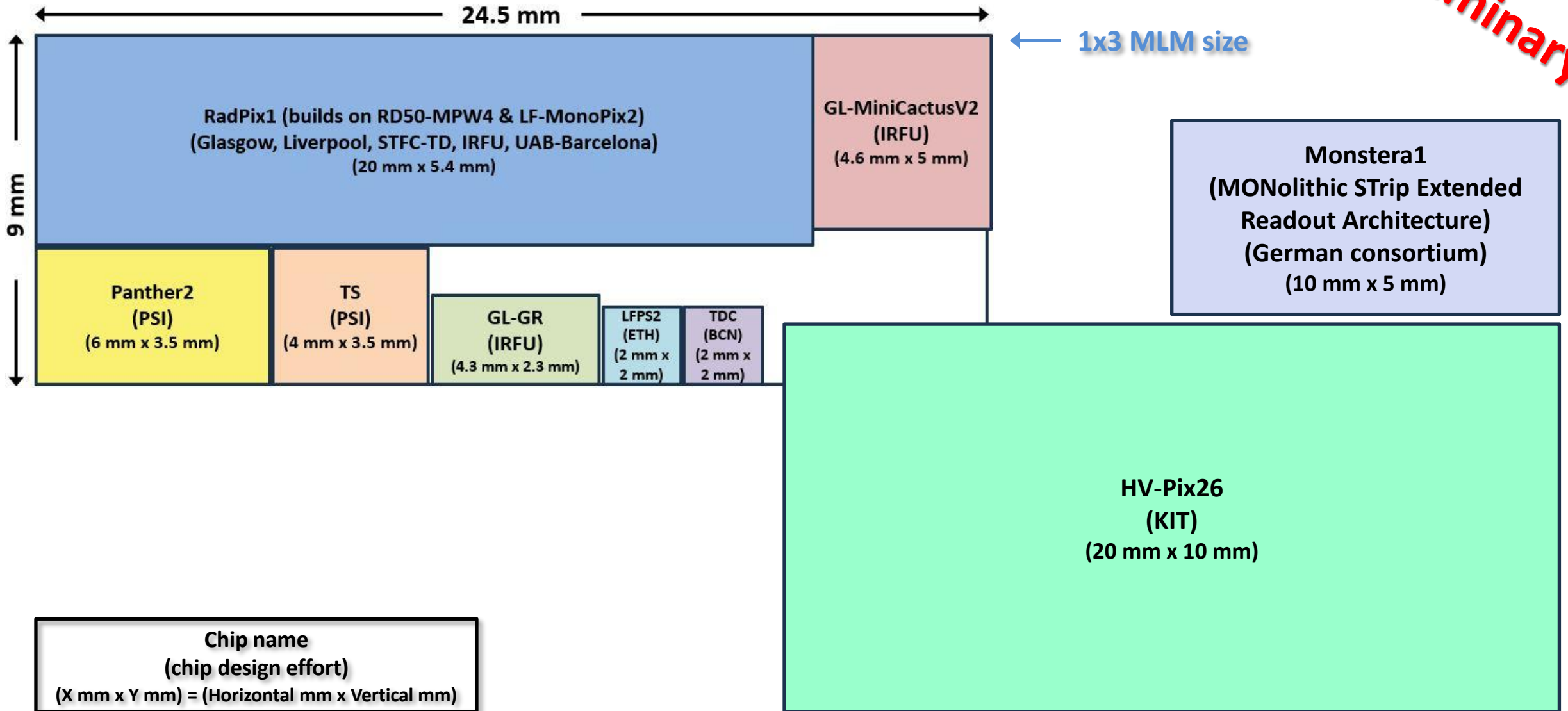
Preliminary



Chip name
(chip design effort)
(X mm x Y mm) = (Horizontal mm x Vertical mm)

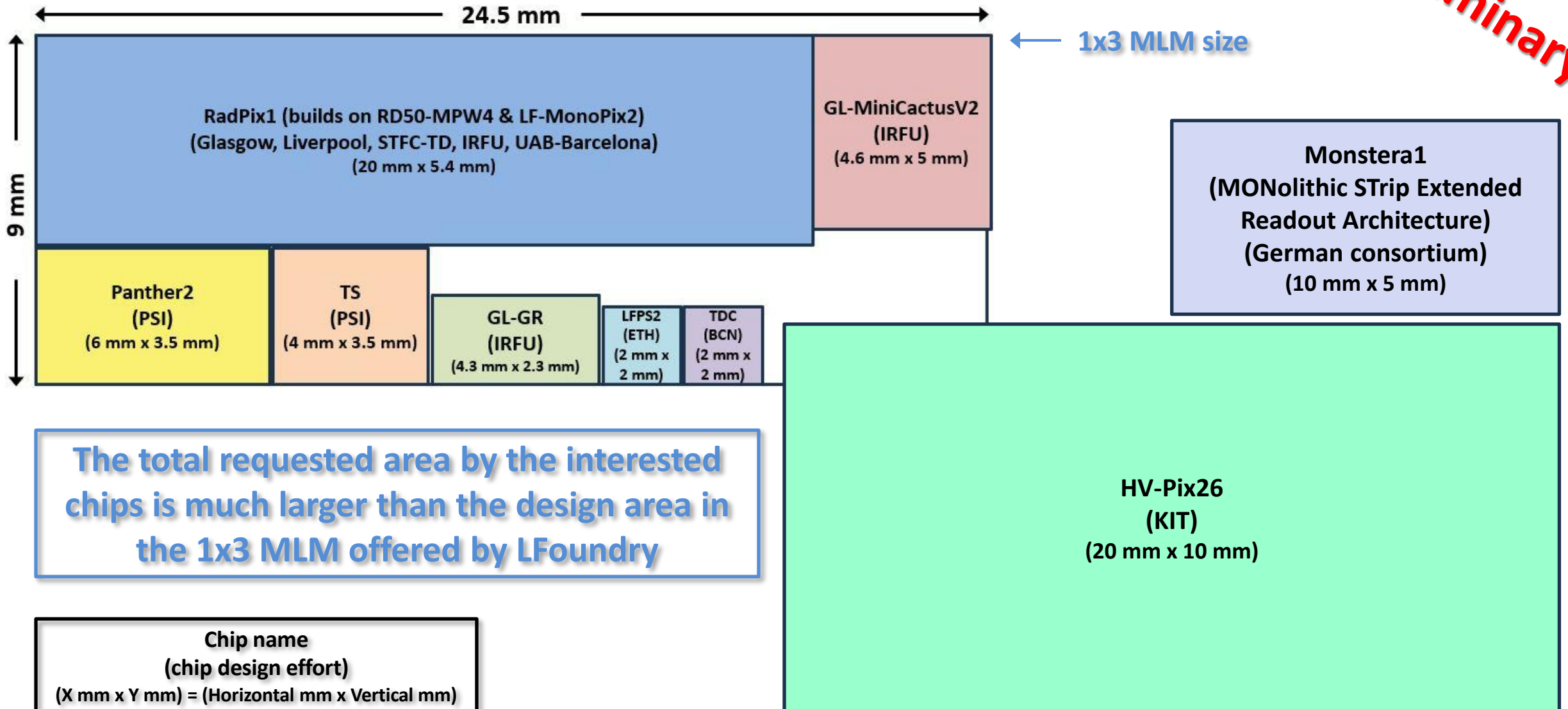
Interested chips (II)

Preliminary



Interested chips (II)

Preliminary



How to proceed

- **Potential solutions**
 - Discuss with LFoundry the possibility of doing a **full mask-set (engineering run)**
 - An engineering run offers $\sim 3x$ the area of an MLM run.
 - Note: some design teams are concerned that the large number of chips and design teams may introduce new complexities and risk delaying the submission, which conflicts with their tight timelines.
 - Explore the option of splitting the submission into **two separate runs**, spaced in time.
- This is currently ongoing, however it must be handled carefully to avoid confusing the foundry.
- Plan to submit a **Collaboration Common Fund (CCF)** to help cover the submission costs.

Interested chips

Many thanks for providing material!

GL-MiniCactusV2

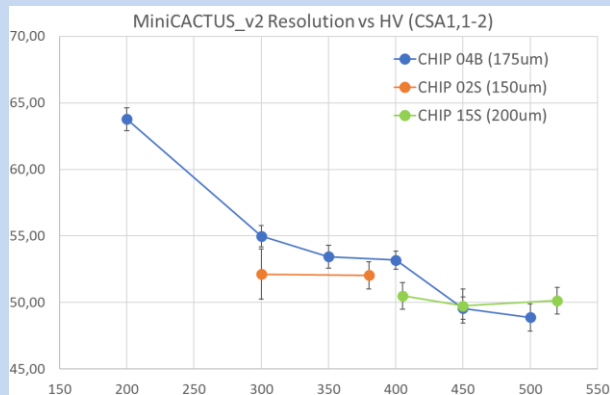
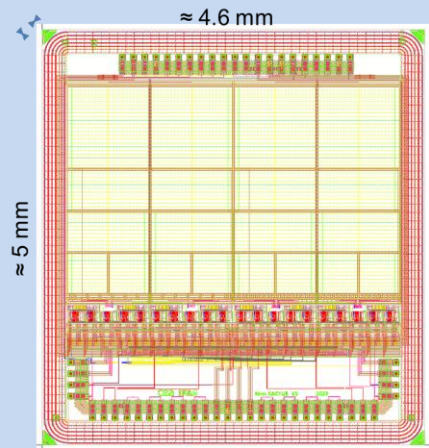
Design team: Yavuz Degerli^a, Fabrice Guilloux^a, Raimon Casanova^b
IRFU^a, IFAE^b

GL-MiniCactusV2

- Study of diodes with intrinsic amplification and integrated FE
- 4.6 mm x 5 mm chip
- Integrated slow control
- Programmable FE
- Two customer-layers needed for gain layer
- Special passivation also needed (use of MT layer)
- Two columns of pixels, organised in half columns
- Precision timing (< 50 ps)

Evaluation plans

- In lab: 90-Sr and IR laser
- Test beam
- Signal amplitude and time resolution measurements

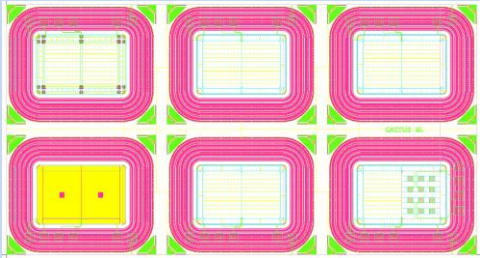


See two next presentations:

- “Testbeam results of the MiniCactus V2 timing demonstrator”, J. Pinol
- “Development of sensors with intrinsic gain in LFoundry 150 nm technology”, P. Schwemling

GL-GR

Design team: Yavuz Degerli^a, Fabrice Guilloux^a, Raimon Casanova^b, Pablo Fernandez^c, Juan Ignacio Drovandi^c, Archie Hanlon^d, Eva Vilella^d
IRFU^a, IFAE^b, IMB-CNM^c, Uni. Liverpool^d



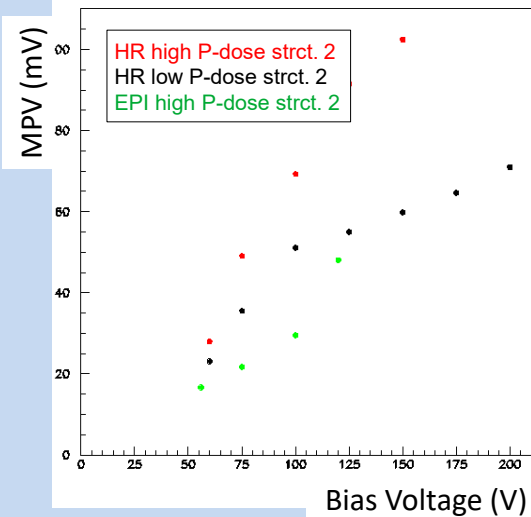
4.3 mm x 2.3 mm

GL GR

- Improved Gain Layer test structures
- Need two customer reserved layers for gain layer implementation
- 6 diodes, each split in half diode
- Precision timing

Evaluation plans

- In lab: 90-Sr and IR laser
- IV
- Measurements of amplitude vs HV

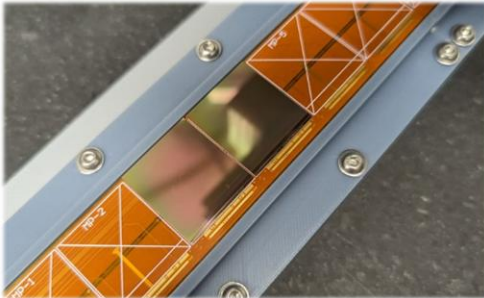
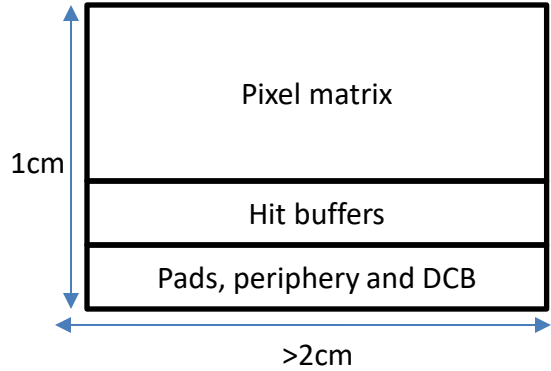


See two next presentations:

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- “Development of sensors with intrinsic gain in LFoundry 150 nm technology”, P. Schwemling

HV-Pix26

Design team: Nicolas Striebig, Alexander Elsenhans, Christian Krämer, Richard Leys, Ilona Münnich, Miaoran Sun, Yue Su, Bowen Xu, Ivan Peric (KIT, Karlsruhe, Germany)



HVC MOS Sensor MuPix for Mu3e



HVC MOS Sensor AstroPix for Compton telescope

Motivation:

HV-CMOS sensors are being developed for use in several cutting-edge applications, including particle physics experiments, a planned Compton telescope, and ion beam therapy.

The **LFo foundry** technology provides several key advantages:

Use of substrates with resistivity $> 2 \text{ k}\Omega$, capability for full substrate depletion, integration of CMOS electronics within a deep n-well, availability of a deep p-well.

These features enable high performance and flexibility, making the technology well-suited for a range of demanding detector applications

Specifications:

- Low-power operation
- Fully depleted thick substrate – essential for Compton telescope applications
- Daisy-chain readout, serial powering, module compatibility

Chip components:

- Pixel matrix, digital hit buffers, digital control block (DC B)

Applications:

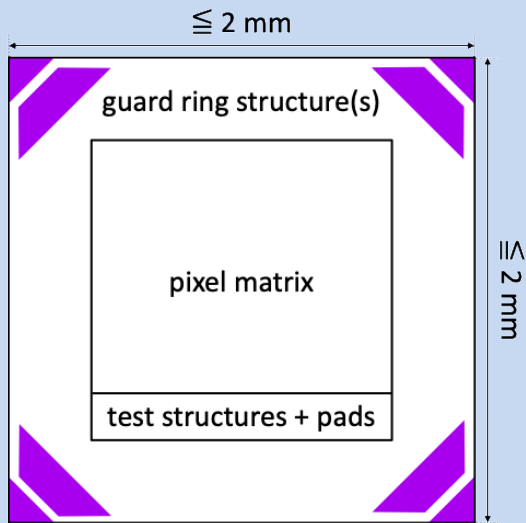
- Use in particle physics experiments, gamma space telescope, beam monitoring for ion therapy

Evaluation plans:

- Performance will be characterised through laboratory measurements and test beam studies, including activities within the DRD project: “HV-CMOS Pixel Detector Demonstrator with Serial Powering.”

LFPS2

Design team: M. Franks, B. Ristic, M. Backhaus
ETH Zurich

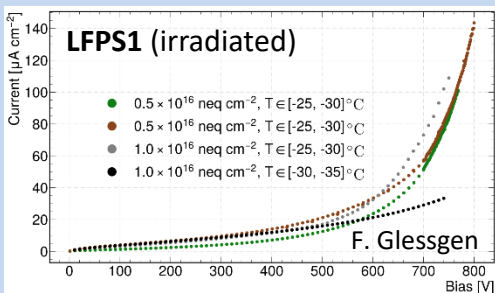


LFPS2

- **Motivation:** Exploration of CMOS chips with AC-coupled pixels as passive sensors in hybrids
- **Specifications:** Minimum 2 mm × 2 mm area (flexible), 1 or more substrate resistivities
- **Description:** Passive sensor with AC-coupled pixels, compatible with 28 nm readout chips for hybridisation
- **Research goals:** Evaluate alternate hybridisation methods, demonstrate a radiation tolerance suitable for CMS L2 after LS4, or FCC-ee

Evaluation plans

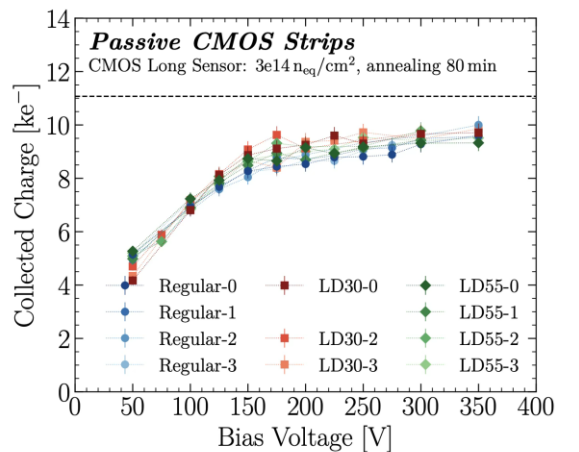
- I-V measurements
- Hybridisation
- ROC + sensor characterisation
- Irradiation campaign
- Test beams



Monstera1

Design team: Ivan Peric, KIT, NN, Bonn

Depending on availability
5mm x 10 mm would be nice



Monstera1

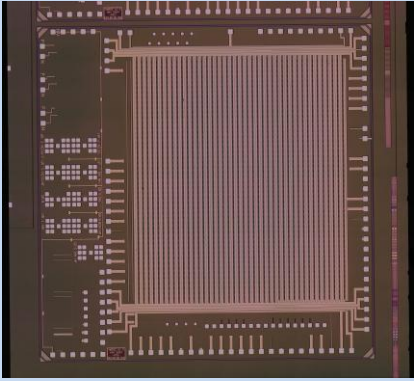
- MONolithic STRip Extended Readout Architecture
- Existing (passive) CMOS strip sensors extensively studied, results well published (e.g. NIM A 1061 (2024) 169132, NIM A 1064 (2024) 169407)
- Up to 60 strips with $75 \mu m$ width based on an existing CMOS strips design
- Each strip will have a front-end directly implemented making this an “active strips sensor”
- Front-end design will be based on the Telepixon2 design with implemented amplifier and comparator.

Evaluation plans

- Testing in the lab with the usual techniques (incl. source measurements)
- Test beam studies

Panther2 + TS

Design team: A. Ebrahimi^a, A. Ghimouz^a, H. Kästli^a, B. Meier^a, E. Monteil^a, T. Rohe^a, P. Sander^b
PSI^a, ETHZ^a



Panther2

- DMAPS with time of arrival measurement
- $\sigma(t) < 1\text{ns}$
- PSI experiments
- Low rate, low radiation
- Test structures
 - GRs
 - Edge TCT

Evaluation plans

- Characterization with newly commissioned DAQ system in lab and test beam
- Measurement of $\sigma(t)$ versus
 - Frontend flavour (3)
 - Chip settings
 - Position of track

Previous R&D – Panther1

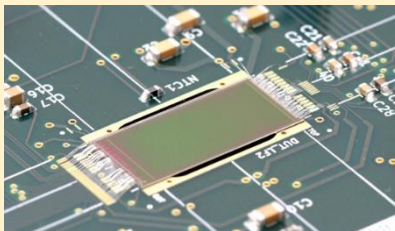
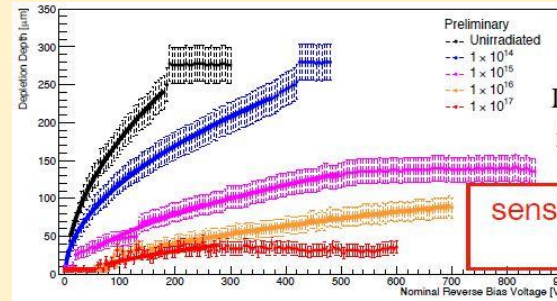
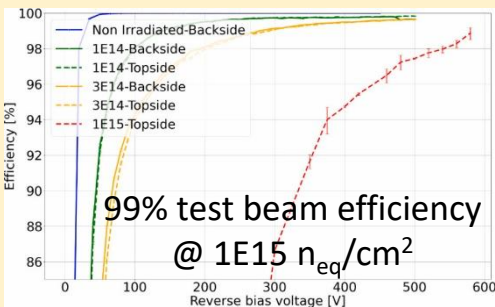
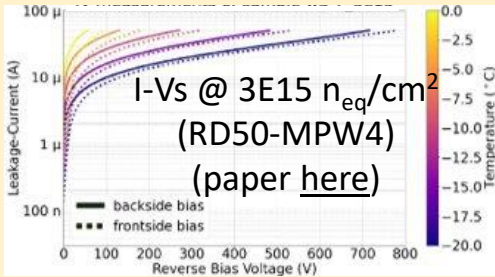
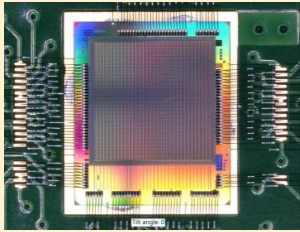
- First prototype submitted 2024
- Currently under test
- **Panther2** will be similar in size, improved sensor/front-end performance

RadPix

Previous R&D

RD50-MPW4

- 62 μm x 62 μm pixels
- 64 x 64 pixels matrix
- Digital RO in sensing diode
- In-pixel low-noise
- Large digital periphery
- Large power consumption
- Improved (wide) chip rings
- $V_{\text{BD}} > 600$ V, small I_{LEAK}
- Backside HV biasing
- 280 μm thickness
- 2 $\text{k}\Omega\cdot\text{cm}$ HR substrate



LF-MonoPix2

- 150 μm x 50 μm pixel (UKRI-MPW1=RD50-MPW4's brother)
- 340 x 56 pixels matrix
- Digital RO in sensing diode
- Large sensor capacitance (noise)

Depletion depth $\leq 1\text{E}17 \text{ n}_{\text{eq}}/\text{cm}^2$

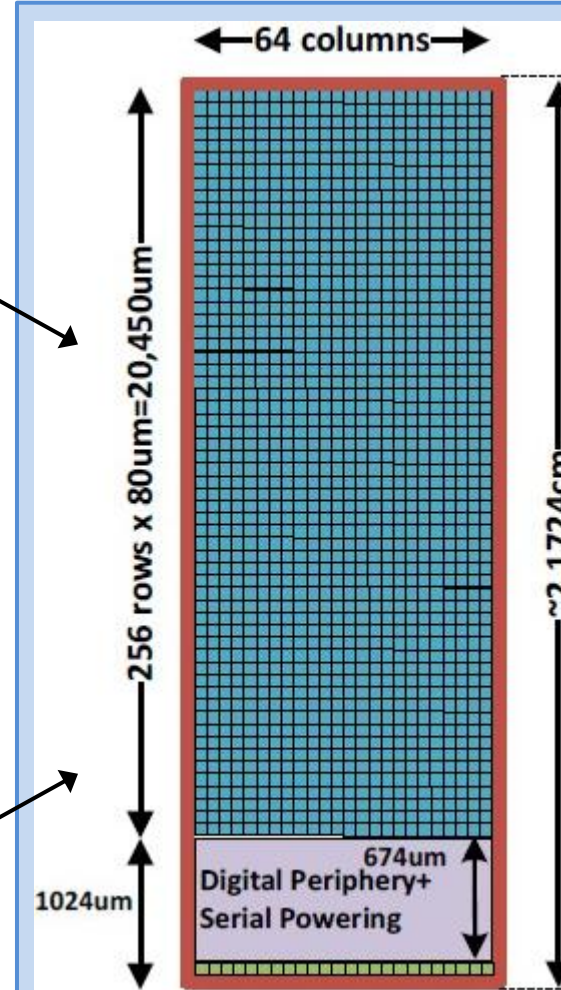
Design team: S. Benhammadi^a, R. Casanova^b, Y. Degerli^c, H. Elnashari^d, N. Guerrini^a, T. Gao^e, F. Guilloux^c, K. Hennessy^f, S. Powell^f, E. Vilella^f, C. Zhang^f
STFC TD^a, UAB^b, IRFU-CEA^c, Uni. Glasgow^d, Uni. Cambridge^e, Uni. Liverpool^f

RadPix1

- 80 μm x 80 μm pixels
- 256 x 64 pixels matrix
- Digital RO in sensing diode
- In-pixel low-noise
- Optimised digital periphery
- 1.28 Gb/s serial link
- Serial powering
- 150 mW/cm^2 power consumption
- Optimised (narrow) chip rings
- Large V_{BD} , small I_{LEAK}
- Backside HV biasing
- 100-200 μm thickness
- $5\text{E}15 \text{ n}_{\text{eq}}/\text{cm}^2$ target

Evaluation plans

- I-V curves
- Pixel matrix with test pulses and radioactive sources
- Chip periphery
- Serial powering with >1 chip
- Irradiation studies and test beam evaluation



Summary

- We are organising a DRD3 community shared submission in the 150 nm High Voltage CMOS process (LF15A) from LFoundry.
- This joint submission will include several chips designed by the DRD3 community.
- We are discussing with LFoundry the submission details, including the submission area.
- The chip design work is currently ongoing and the tape-out is tentatively planned for March 2026.