

Development of sensors with intrinsic gain in LFoundry 150 nm technology

Monday, 10 November 2025 15:15 (20 minutes)

One of the limitations of monolithic sensors is their signal over noise ratio, which constrains strongly the downstream front-end electronics, especially for timing oriented sensors, and leads to architectures that are quite power hungry. Present monolithic designs have been shown to reach a 50 ps time resolution for MIPs, with a power consumption of several hundreds of mW per cm^2 .

A possible way to improve further the time resolution, and also to reduce the power required to operate the fast front-end needed for good timing performance, is to implement directly inside the sensor a charge multiplying layer in the form of a PN junction (DJ-LGAD concept). Given sufficient polarization, a large electric field develops in this PN junction, leading to avalanche multiplication of collected charge carriers.

Six different test structures, with slightly different architectures of the gain layer, have been produced in 2024 using the LFoundry 150 nm LF15A process. Two epi wafers and two HR wafers have been produced, with two different sets of doping parameters for the gain layer. The doping parameters of the gain layer and its geometry have been optimized beforehand using TCAD simulations.

IV measurements, and first test results obtained with IR light and Strontium beta particles will be presented, showing that a gain of about 10 can be obtained.

Type of presentation (in-person/online)

online presentation (zoom)

Type of presentation (I. scientific results or II. project proposal)

I. Presentation on scientific results

Authors: HANLON, Archie William (University of Liverpool); VILELLA FIGUERAS, Eva (University of Liverpool (GB)); GUILLOUX, Fabrice (Université Paris-Saclay (FR)); Dr PELLEGRINI, Giulio (Centro Nacional de Microelectrónica (IMB-CNM-CSIC) (ES)); HAMMERICH, Jan (University of Liverpool); MEYER, Jean-Pierre (Université Paris-Saclay (FR)); PINOL BEL, Joaquim (IFAE); FERNANDEZ-MARTINEZ, Pablo (IMB-CNM, CSIC); Prof. SCHWEMLING, Philippe (Université Paris-Saclay (FR)); CASANOVA MOHR, Raimon (IFAE - Barcelona (ES)); GRINSTEIN, Sebastian (IFAE - Barcelona (ES)); TERZO, Stefano (IFAE Barcelona (ES)); DEGERLI, Yavuz (CEA Saclay)

Presenter: Prof. SCHWEMLING, Philippe (Université Paris-Saclay (FR))

Session Classification: WG/WP1 - CMOS technologies