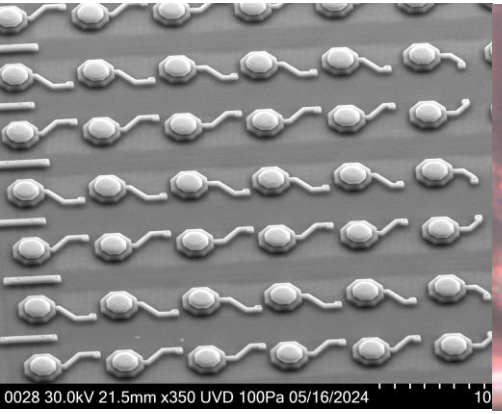
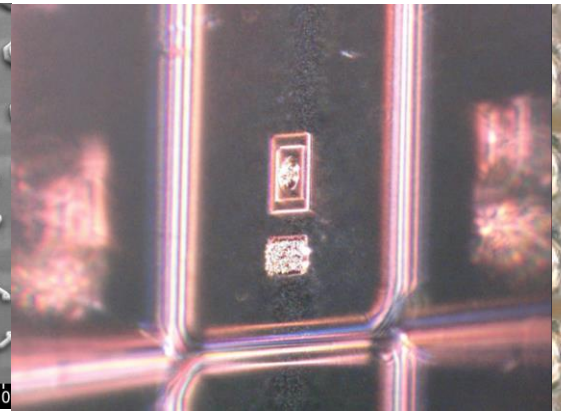
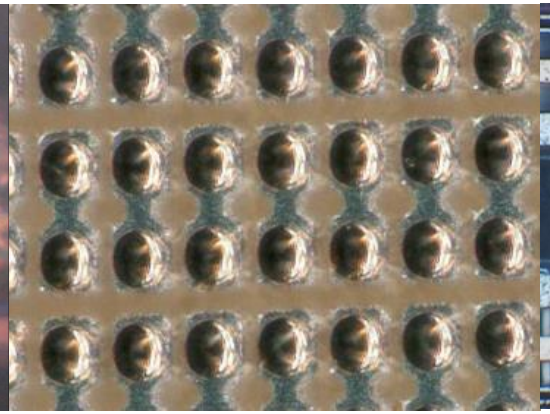
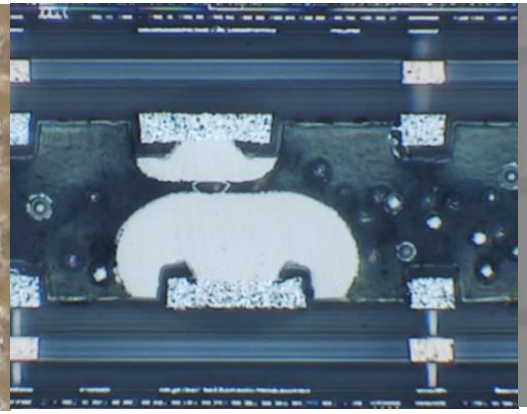
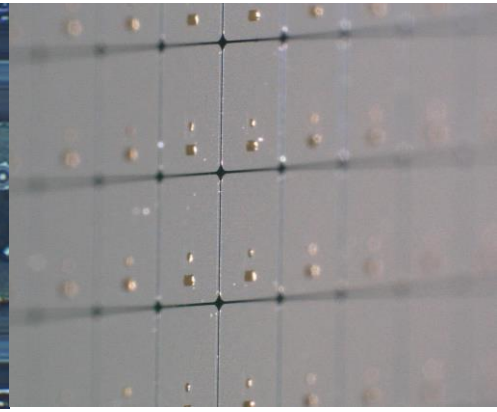
EP-DT
Detector Technologies

EP R&D

In-house Flip-Chip Hybridisation Updates



4rd DRD3 week

10-14 Nov. 2025

Giovanni Calderini[2], Dominik Dannheim[1], Ahmet Lale[1], Moritz Lauser[1,4], Mateus Vicente Barreto Pinto[3], Abhishek Sharma

1: CERN 2: LPNHE-Paris, Centre National de la Recherche Scientifique
3: Universite de Geneve 4: KIT - Karlsruhe Institute of Technology

Flip-chip hybridisation

Goal:

- Development of single-die hybridisation techniques that offer the community a reliable solution for prototyping and sensor/ASIC development
- Flexible processes adaptable to various project needs
- Maximum in-house to ensure short turnaround times and rapid adjustments

Flip-chip hybridisation using a semi-automatic bonding machine

- Precise temperature, pressure and alignment control (post bonding accuracy from 1 to 2 µm)
- Heating up to 400 ℃ and force applied up to 100 kgf

Flip-chip bonder SET ACCµRA100 used for flip-chip

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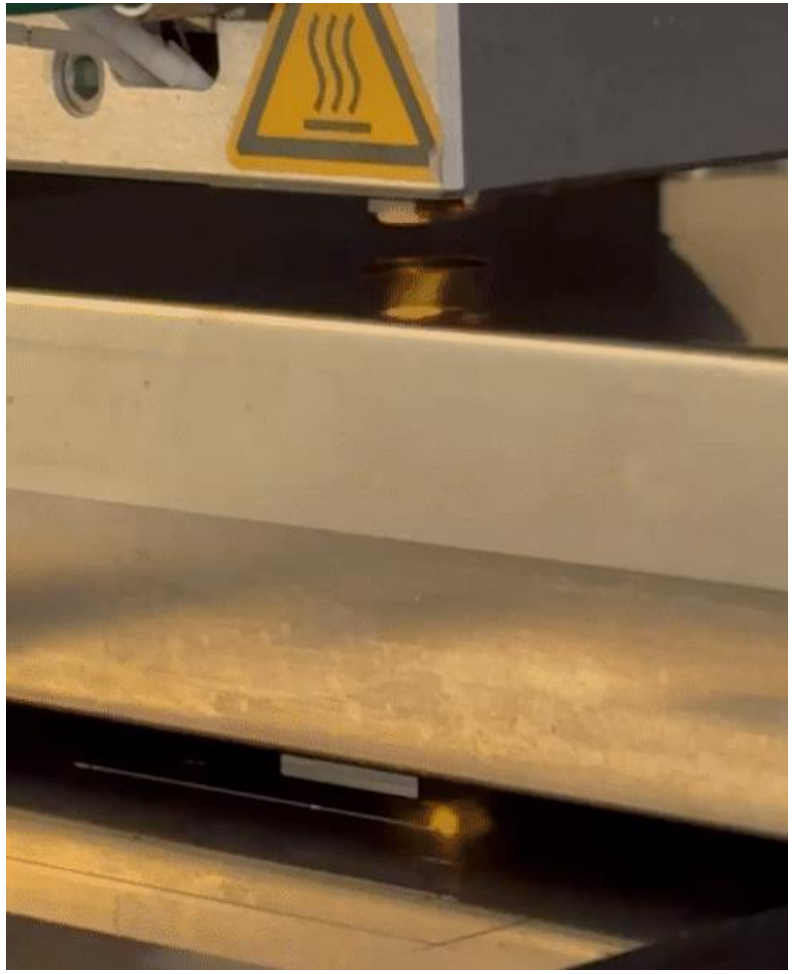

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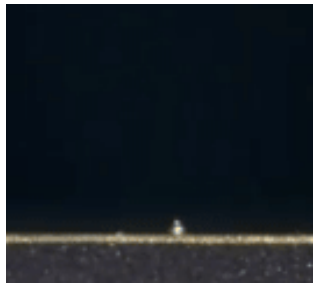

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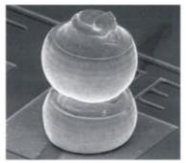

Stacked Gold studs

(Pictures from Hybrid SA)

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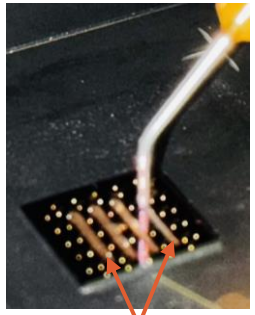

Adhesive between gold studs

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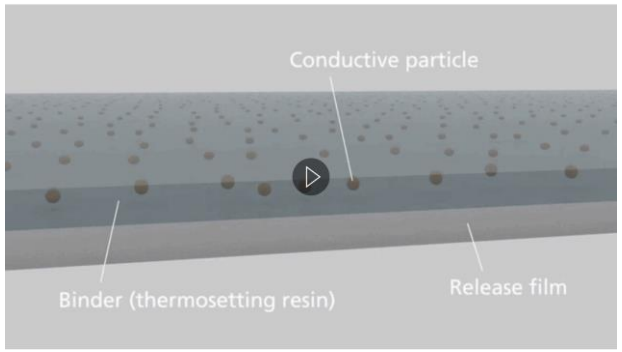
1) ACF lamination on the ASIC or the sensor

ACF Composition



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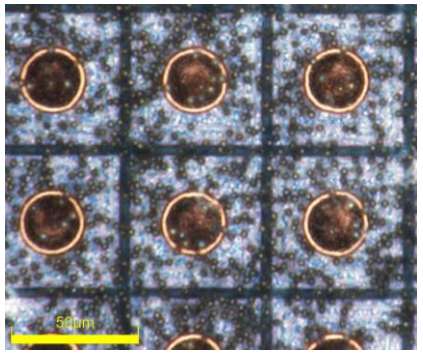

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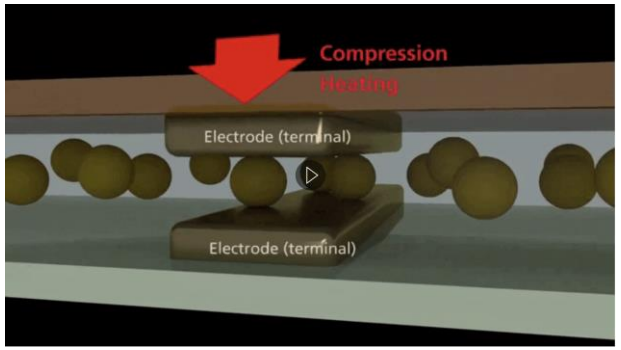

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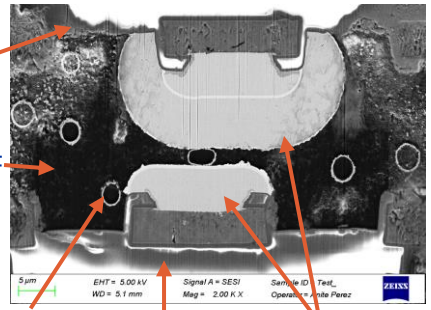

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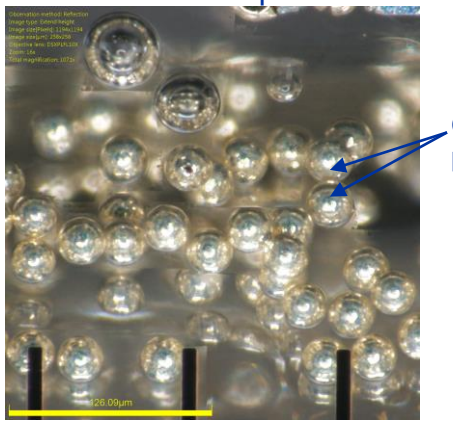

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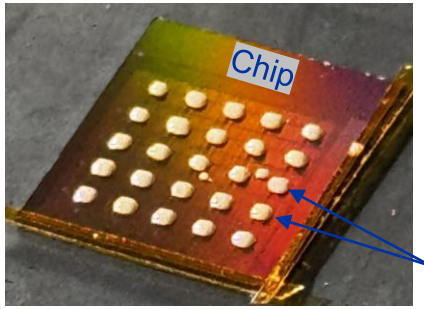

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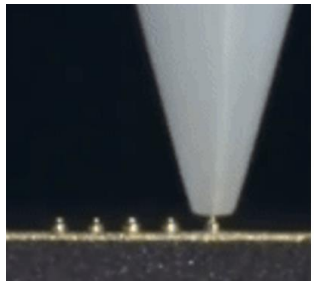

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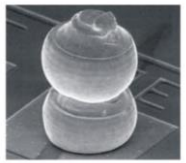

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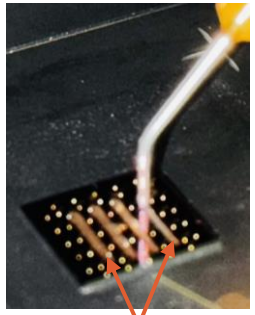

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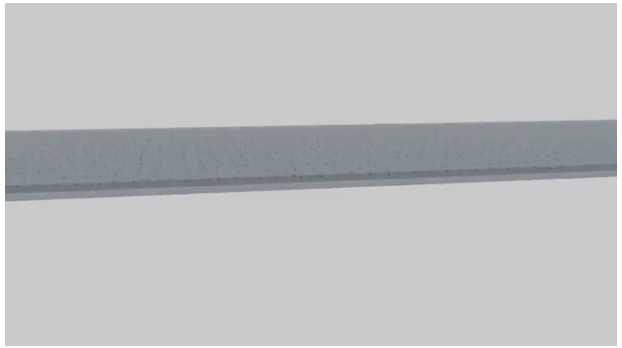

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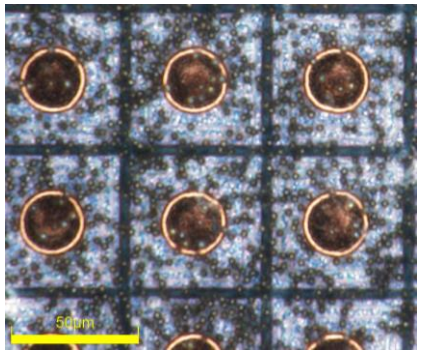

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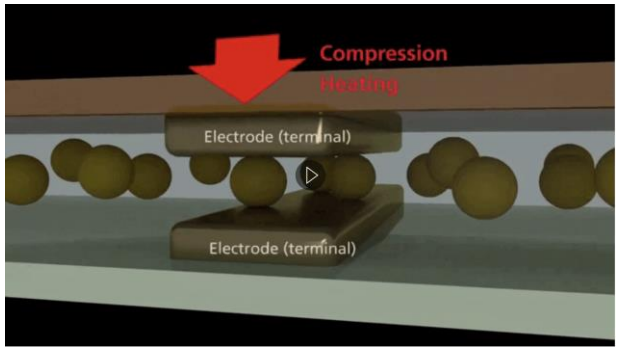

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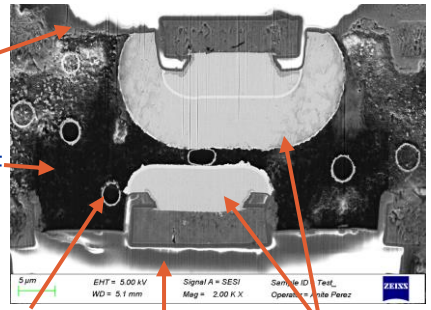

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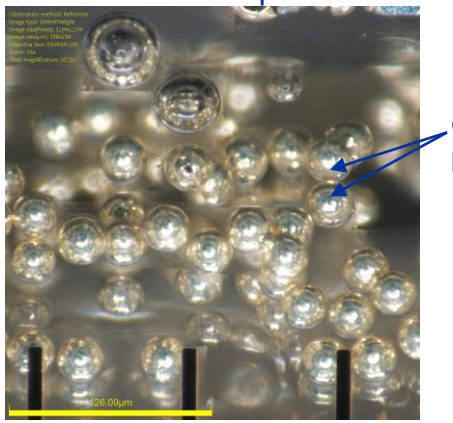

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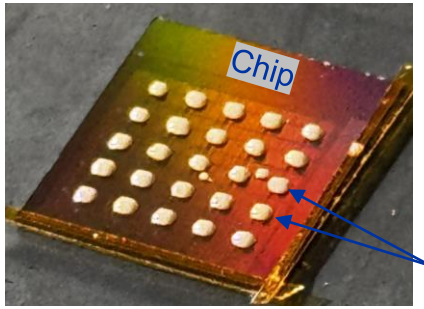

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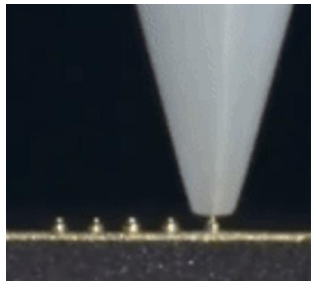

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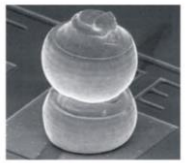

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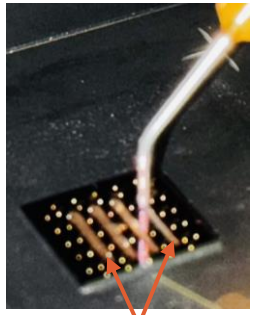

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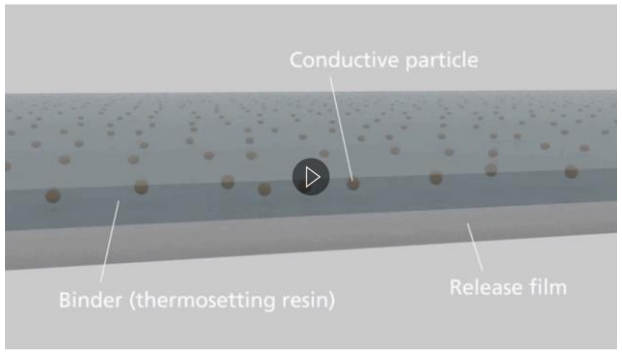

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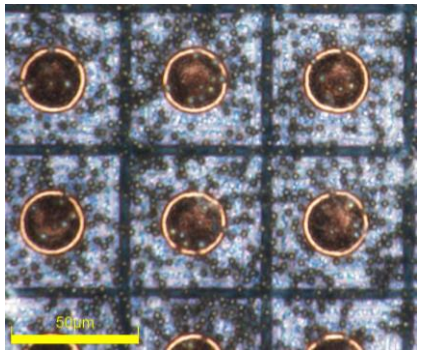

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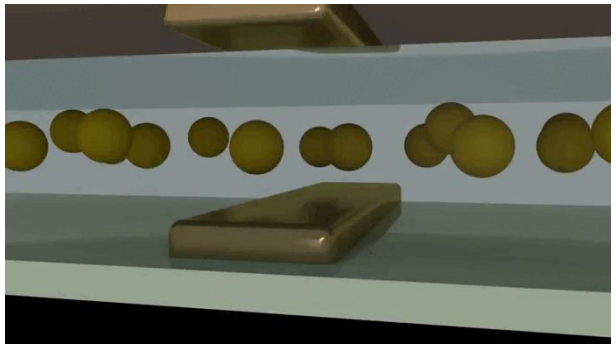

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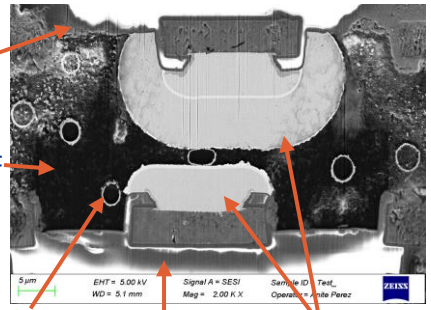

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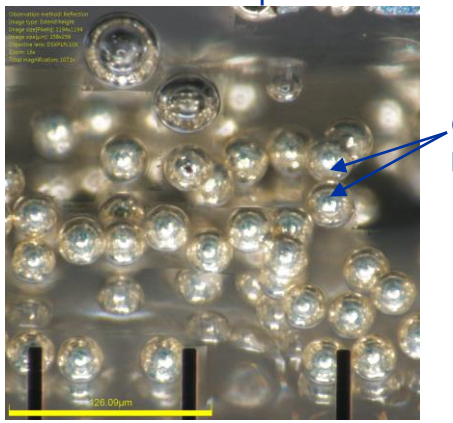

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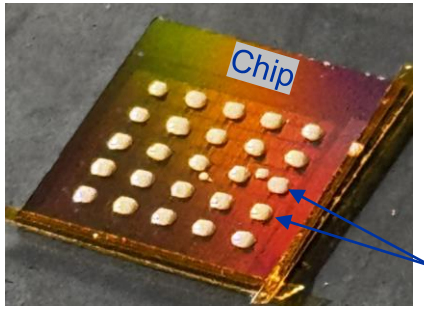

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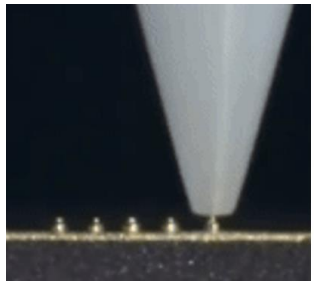

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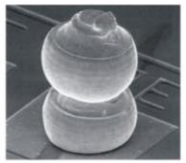

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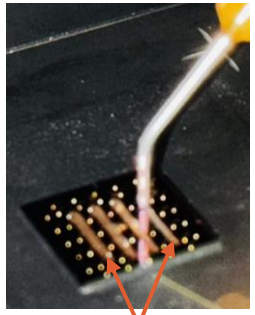

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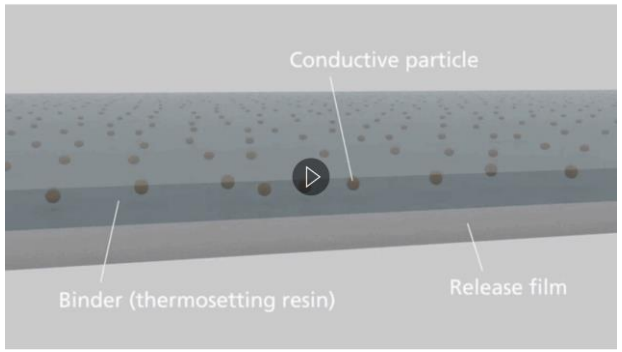

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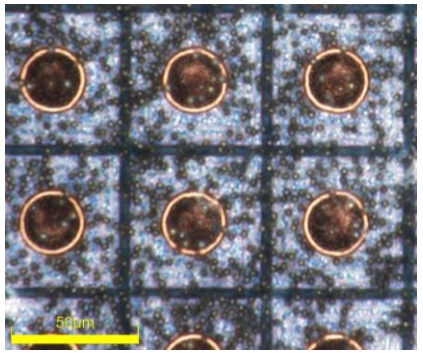

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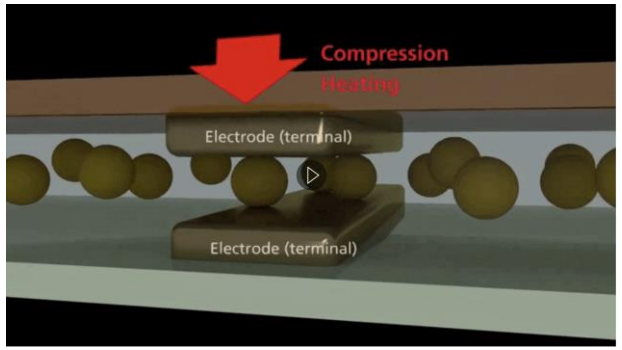

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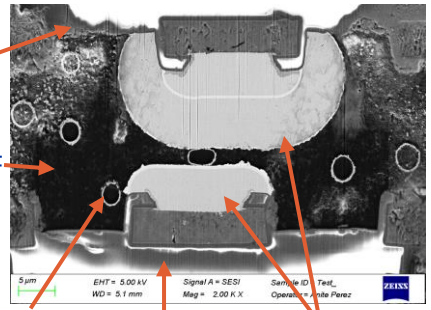

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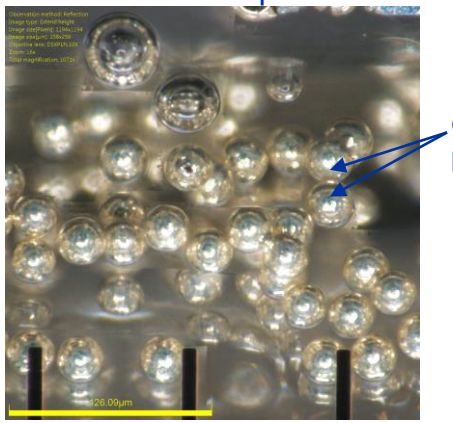

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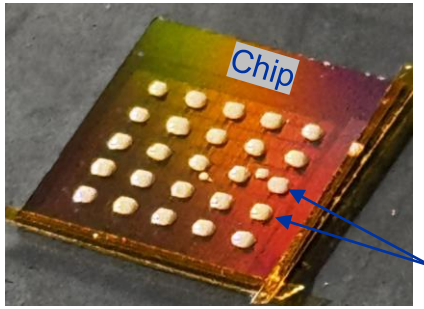


3) Flip-chip bonding

Hybridisation of test chips without UBM, with ACP

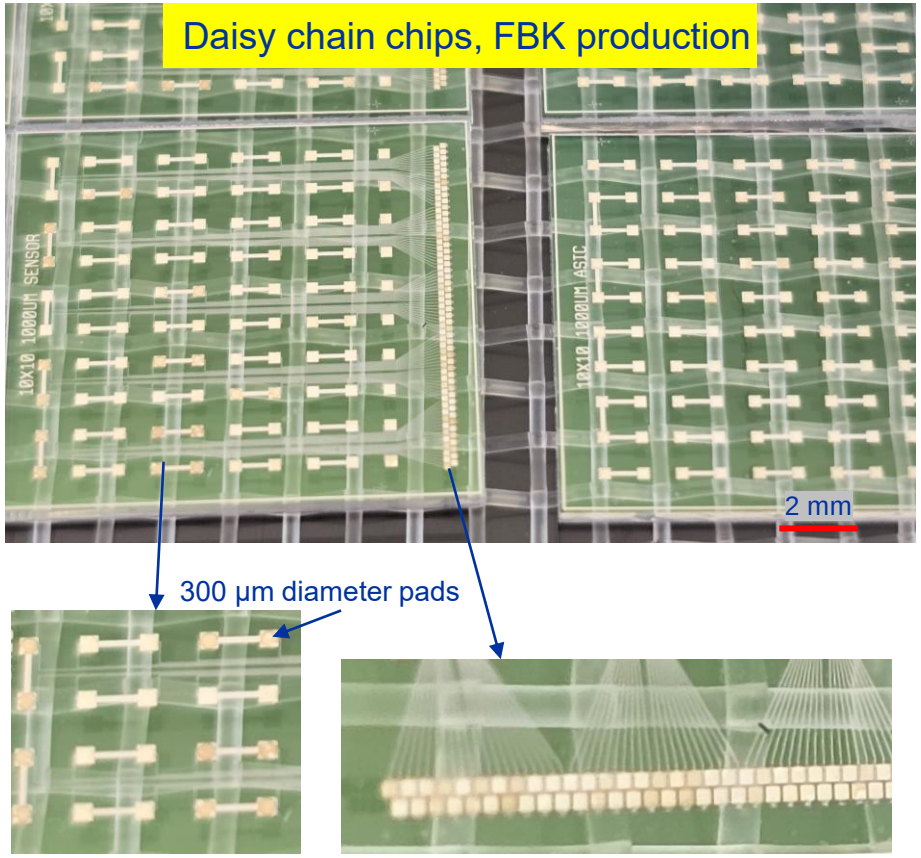
Hybridisation of chips without UBM, with ACP

(ACP: Anisotropic Conductive paste)

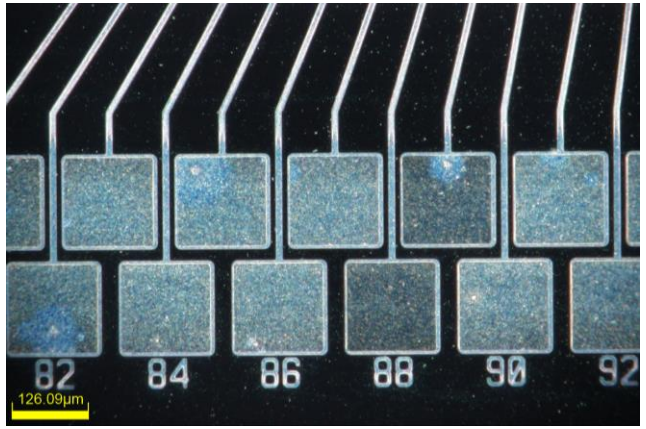
Objective: Evaluate the feasibility of hybridizing chips without UBM and assess the potential advantages of using spiky particles. A lower contact resistance is expected on bare aluminum pads, as the spikes may penetrate the native oxide layer.

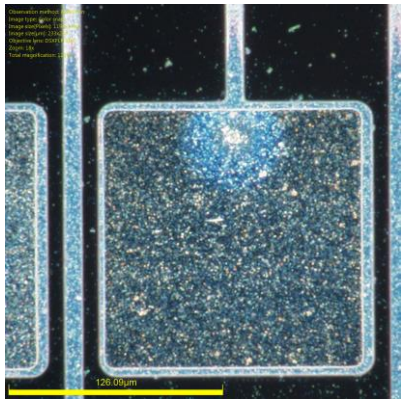
2 daisy chain test assemblies done, chips <u>without plating/UBM</u>:

- 1 10x10 1mm pitch, ACP with regular 30 µm particles
- 1 10x10 1mm pitch, ACP with spiky 30 µm particles

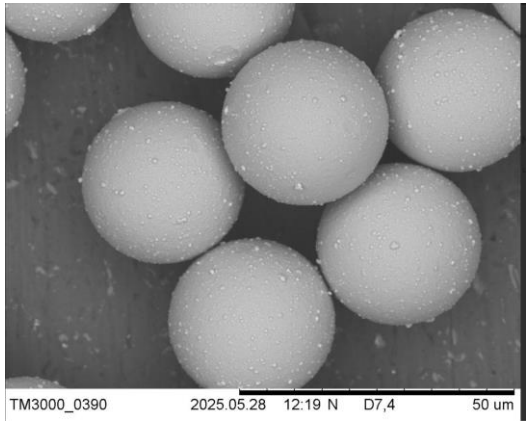


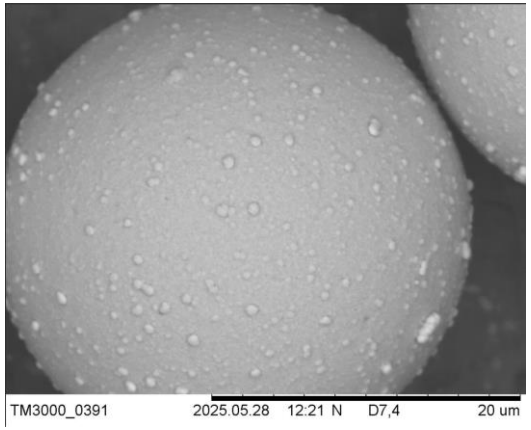
Highly oxidised pads
(not deoxidised on purpose)





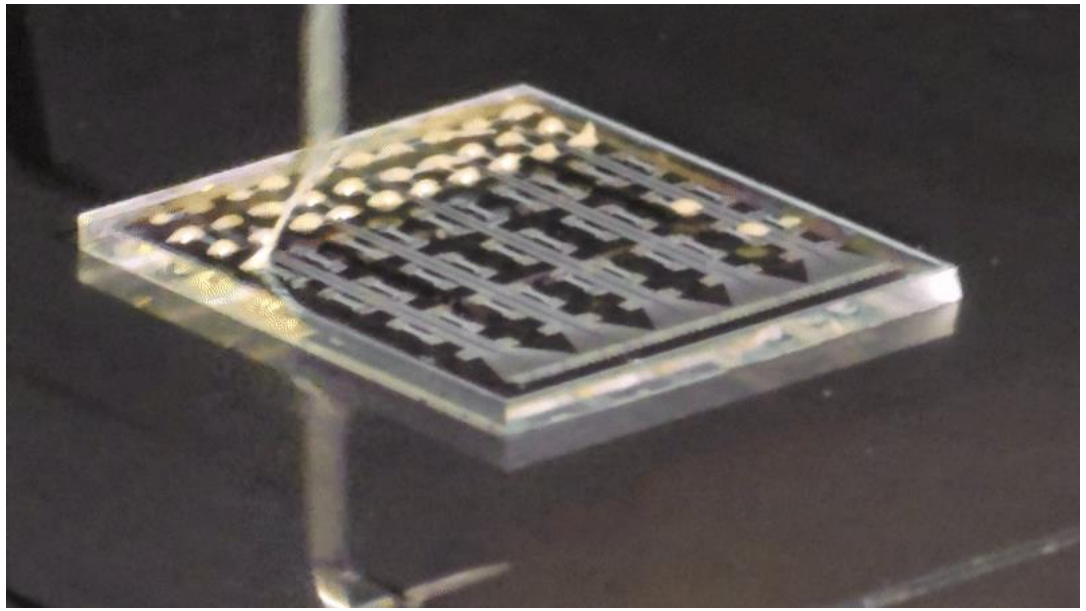
30 µm spiky particles



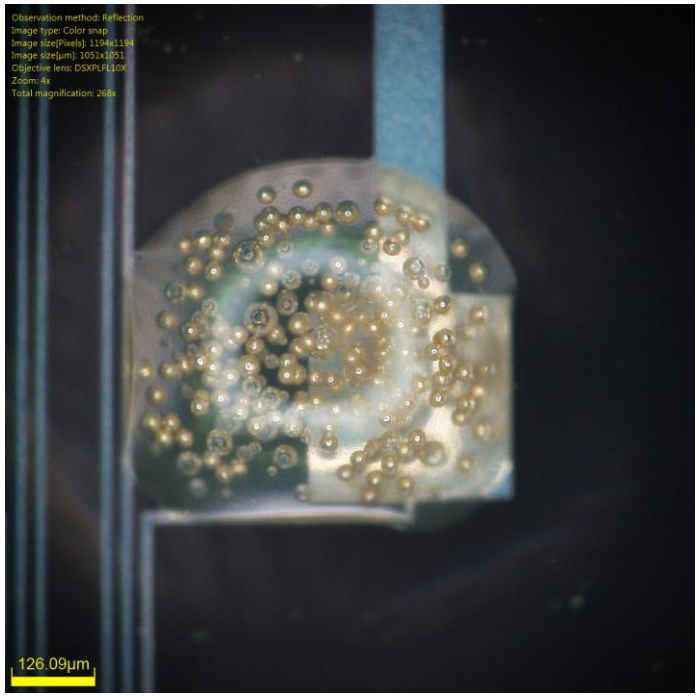


Hybridisation of chips without UBM, with ACP

Araldite 2011 + conductive microparticles
2 mixes prepared, one with regular particles,
One with spiky particles



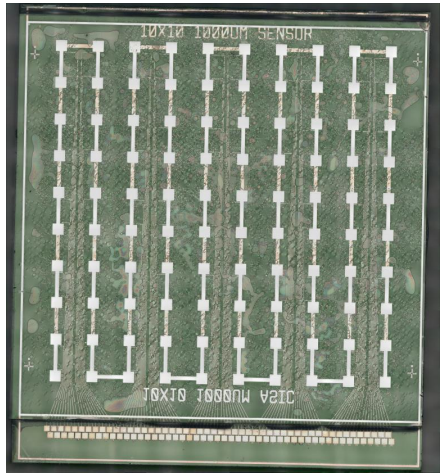
Dispense of ACP on aluminium pads (chip size 11 mm x 12 mm)



Drop of ACP on a pad

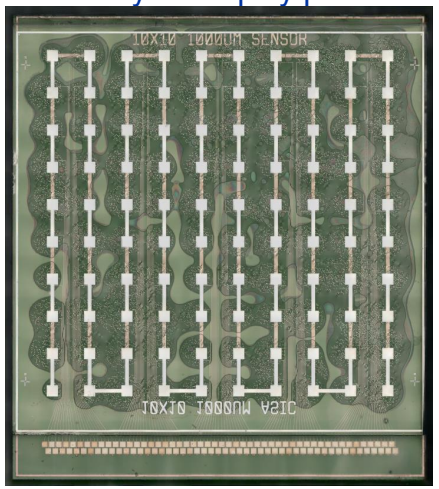
Hybridisation of chips without UBM, with ACP

Assembly with regular particles

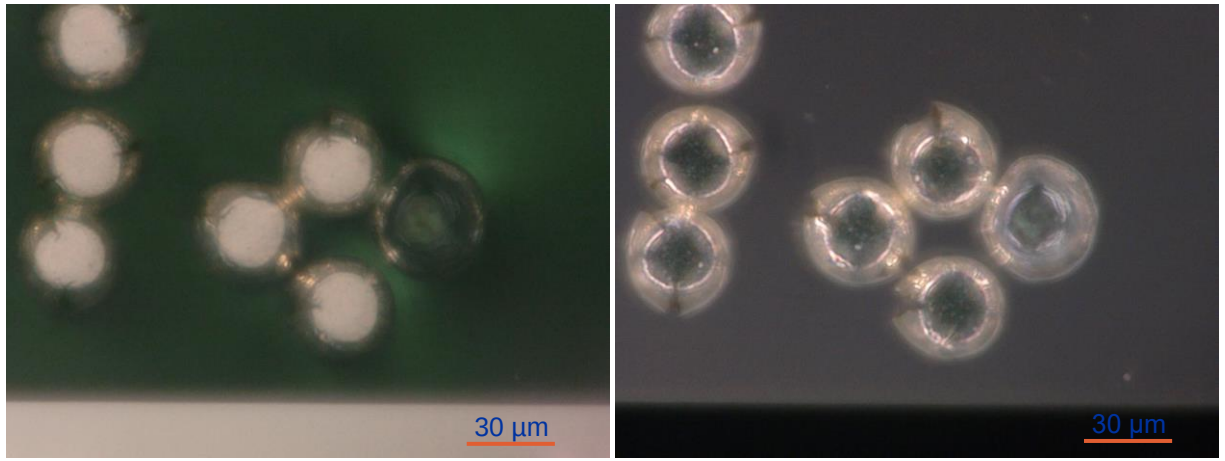


11 mm

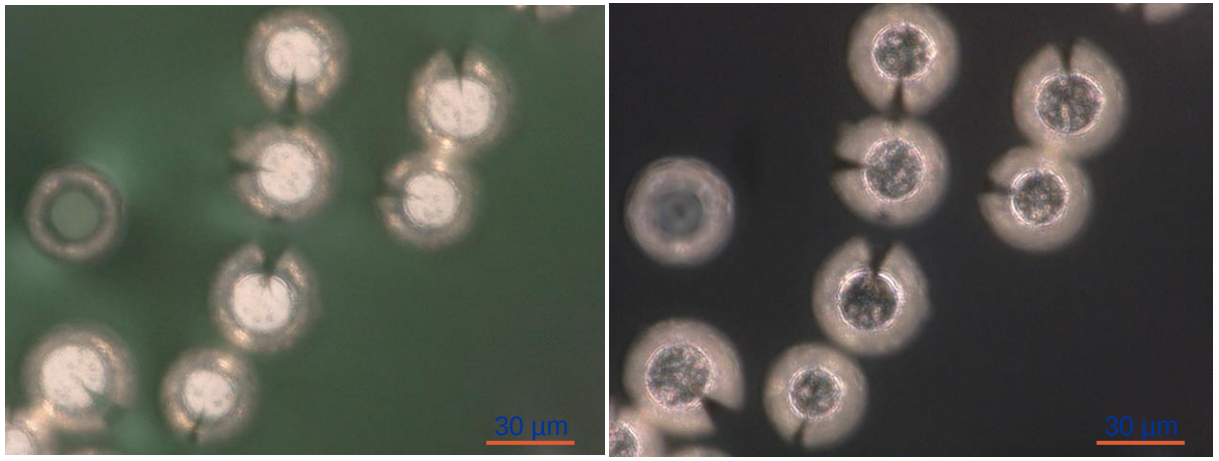
Assembly with spiky particles



After Flip-chip bonding



Smashed regular particles after bonding



Smashed spiky particles after bonding

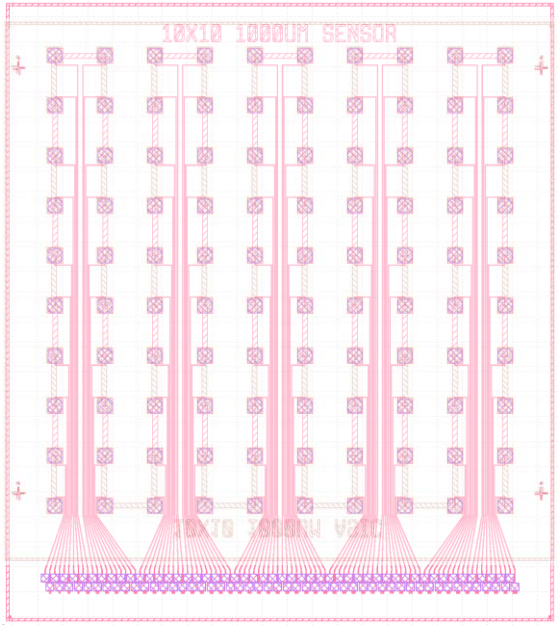
~20 particles per connection, estimated from optical microscopy.

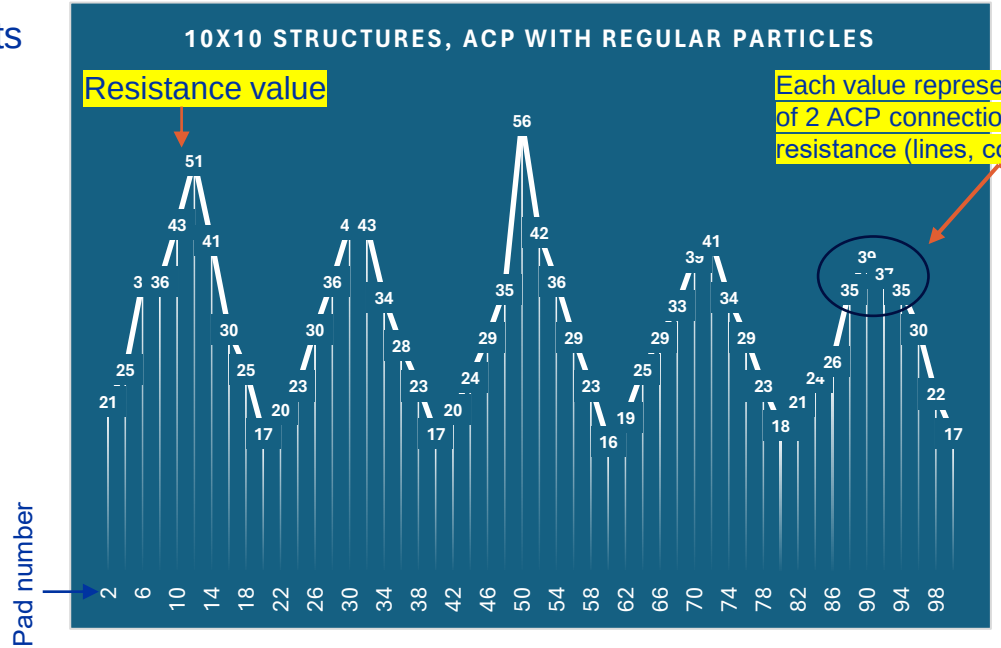
Flip-chip parameters: 20kg, 100°C, 7min

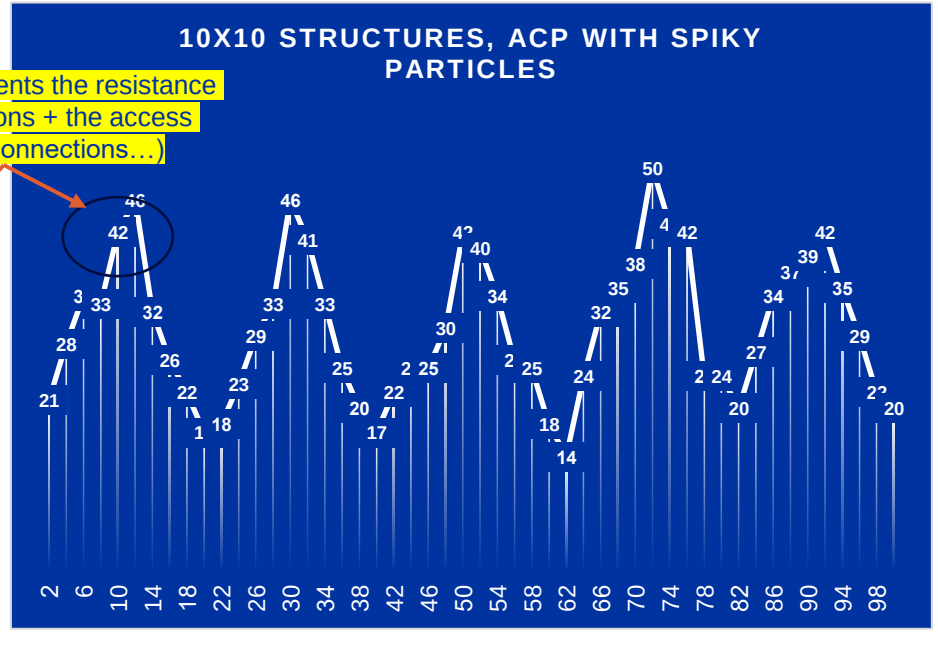
Electrical characterisations

- 2 wires resistance measurements with a probe station

10x10 daisy chain test structures (GDS)







- Full chain (between first and last pad , chain of 100 ACP connections): 785 ohm
- Full chain minus the resistance of the lines (32 ohm): 753 ohm
- Mean value of the resistance per connection: 7.5 ohm

- Full chain (between first and last pad, chain of 100 ACP connections): 606 ohm
- Full chain minus the resistance of the lines (32 ohm): 574 ohm
- Mean value of the resistance per connection: 5.7 ohm

Conclusion:

- Ongoing work
- Assemblies done with ACP, on chips without UBM/ENIG (aluminium pads), without cleaning or deoxidation
- 100% connection yield obtained for both assemblies.
- Average resistance per connection 24% lower for the assembly done with spiky particles, based on 100 connections on each assembly, to be confirmed with more samples.
- That shows the possibility of hybridisation directly with ACP, without any UBM
- Aging studies to be done to assess the reliability of the connections

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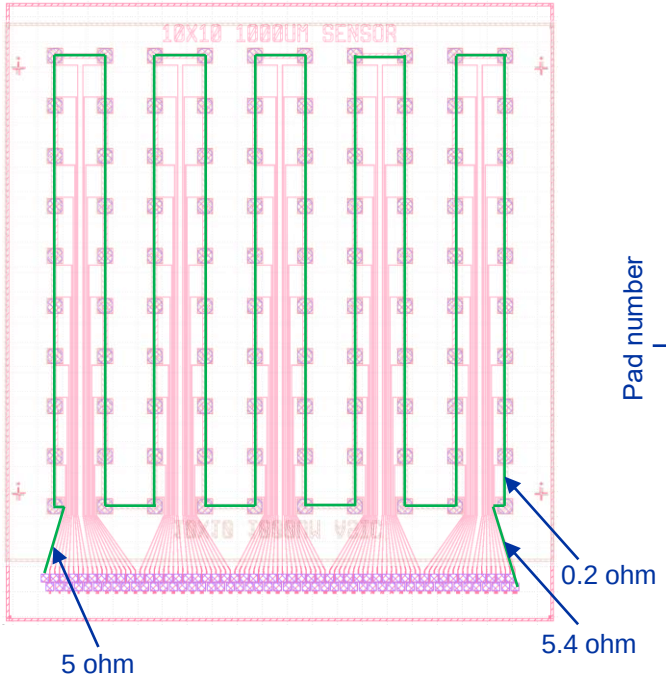

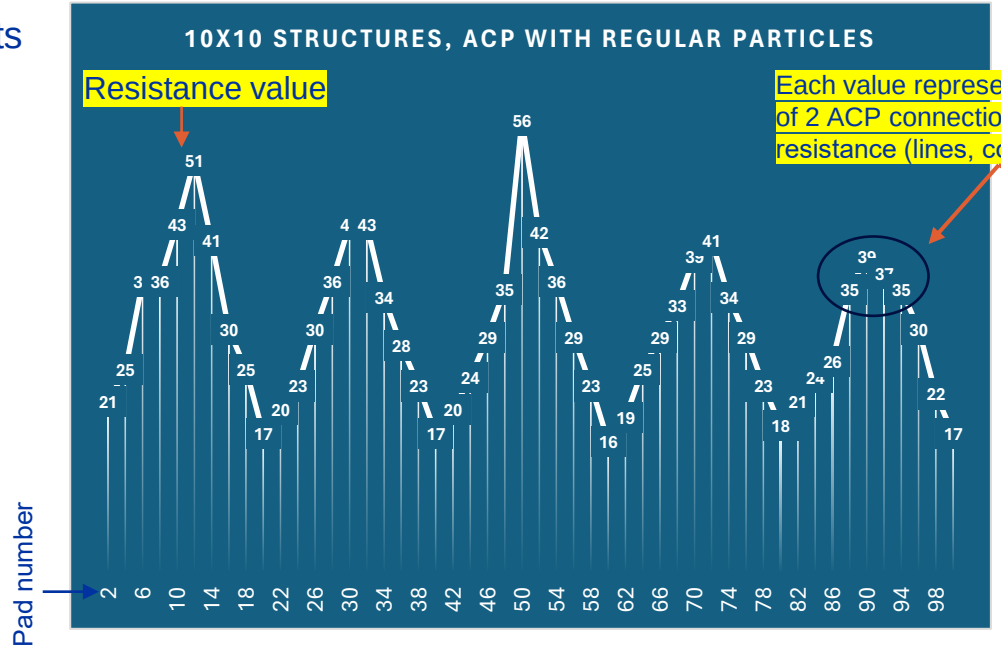

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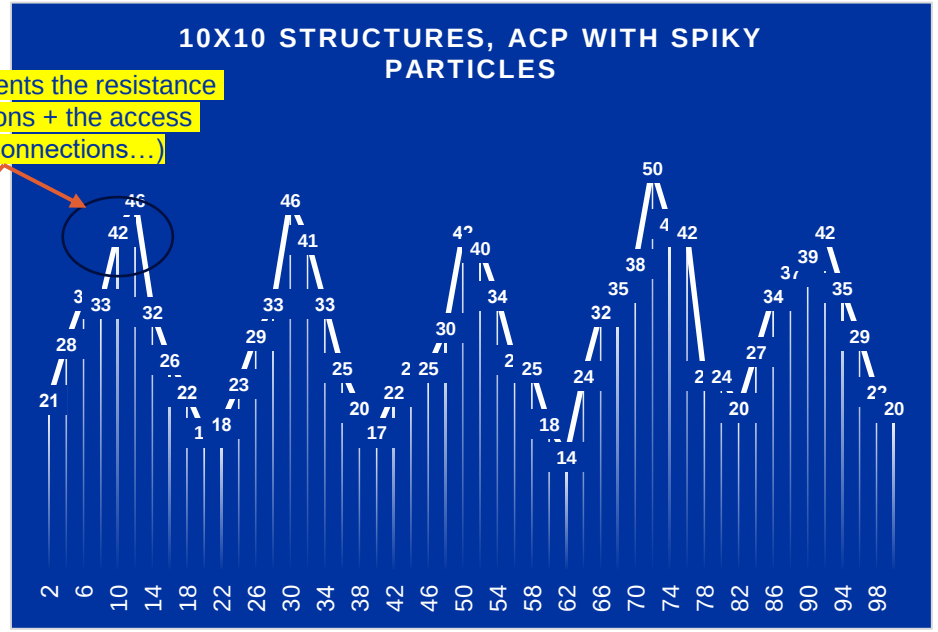

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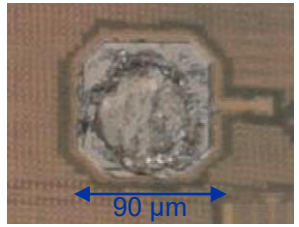
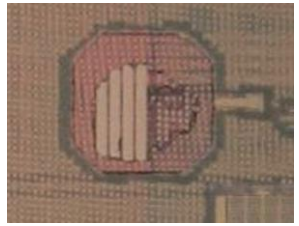
Hybridisation of LATIC ASICs and Ti-LGAD sensors, with ACP

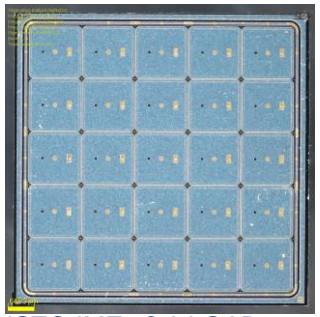
LATIC/LGAD Hybridisation with ACP

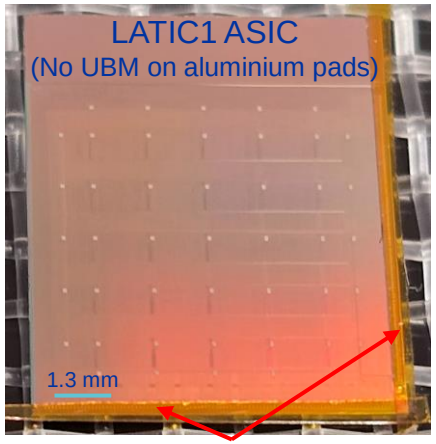
- Hybridisation of LATIC ASICs (130 nm TSMC) with USTC-IME v2.1 LGAD sensors (1.3 mm pitch)
- Previously 100% connection yield obtained with gold-studs and non-conductive adhesive (3rd DRD3 week, Ahmet LALE)
- Recently, problems with stacked gold-studs deposition on these chips
- ACP hybridisation under study as alternative to gold studs (in-house, cheaper)



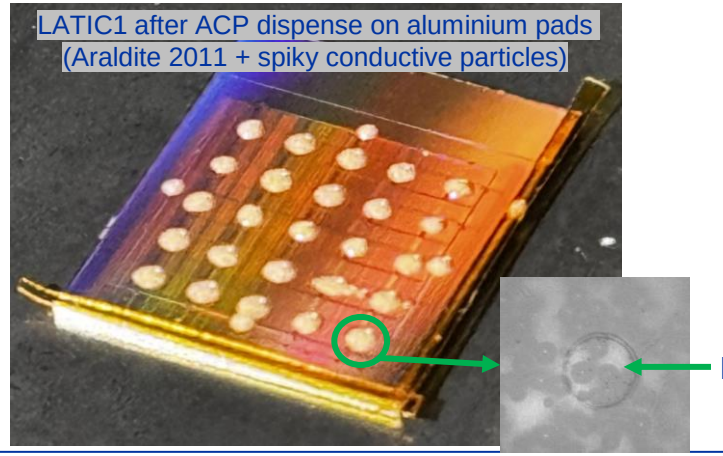
Gold stud adhesion issue


Pad delamination issue
after gold stud deposition


USTC-IME v2.1 LGAD sensor

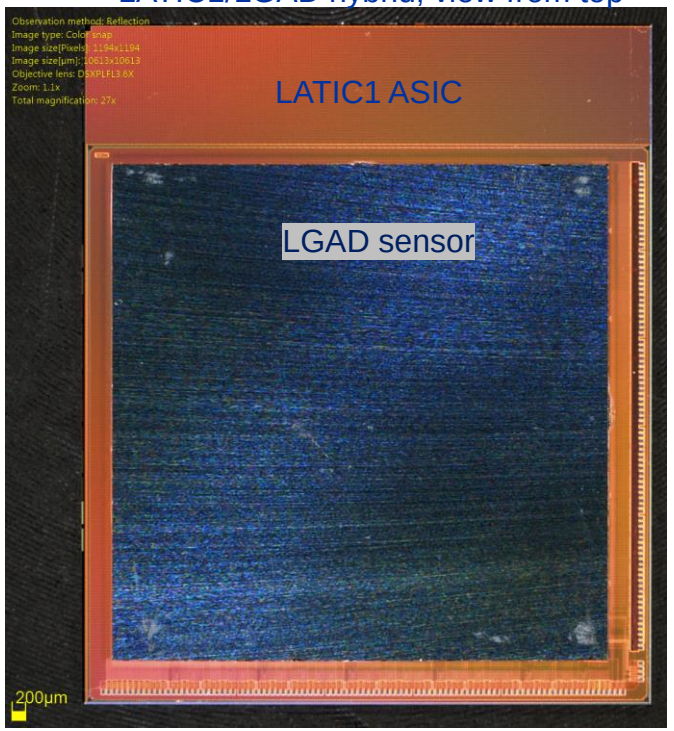


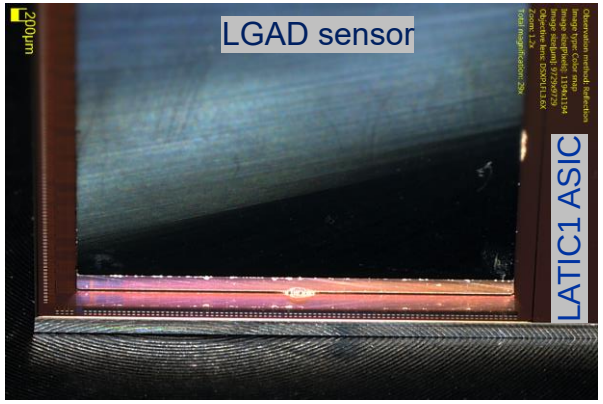
Wire-bonding pads protected
with ≈0.5 mm width Kapton tape

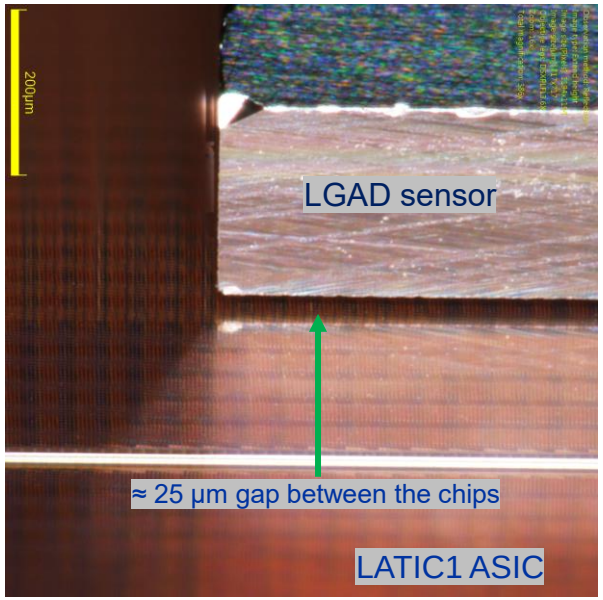


Pad (90 µm diameter)
Few particles on each
pad before bonding

LATIC1/LGAD hybrid, view from top



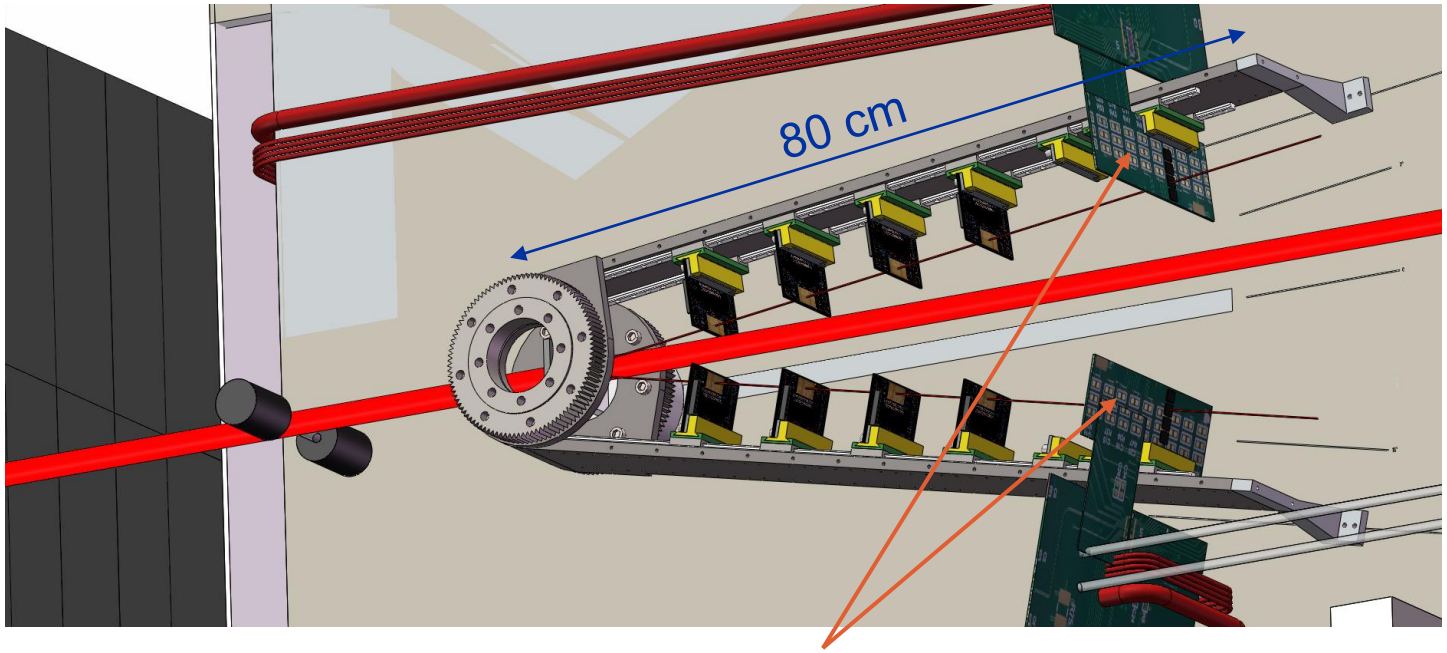


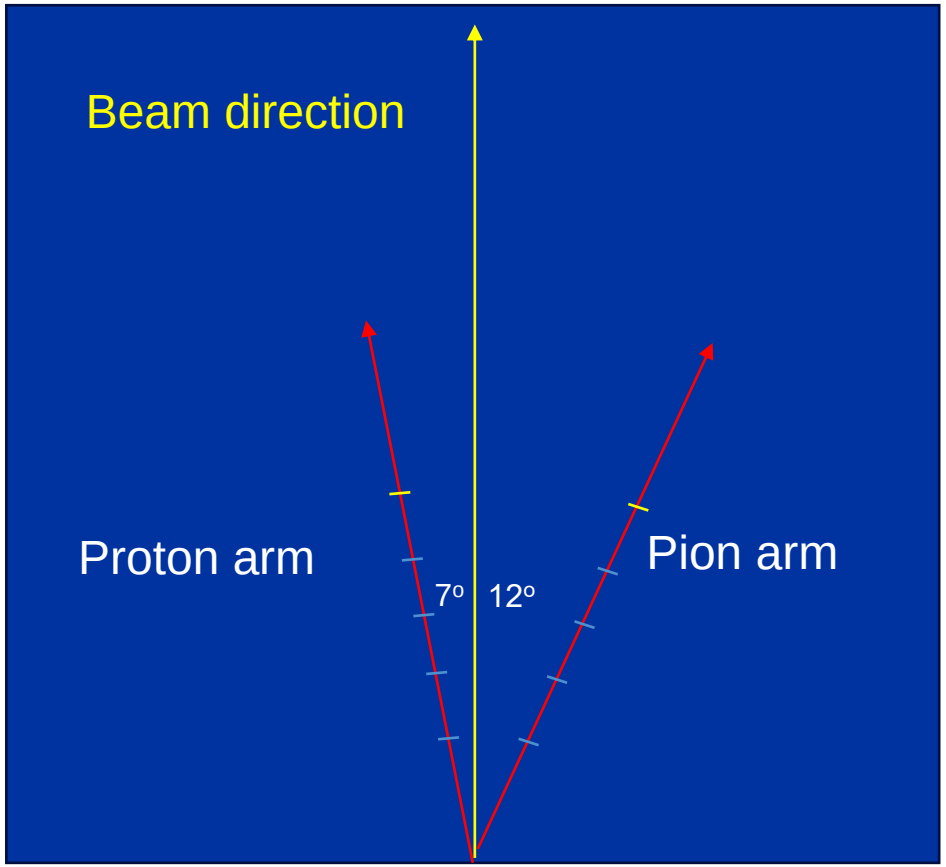


- 2 hybrids done
- Tests in progress at USTC

Near term target: hyperon-nucleon spectrometer

Oxygen ion beam on Carbon target





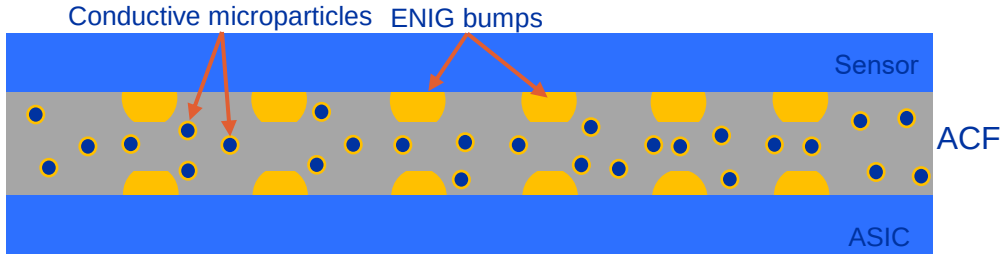
LGAD: USTC-IME 5x5 prototypes
ASIC: USTC LATIC chips
Total number of hybrids: 2x3x4
Timeline: start detector assembly in Feb 2026

Collaboration: IMP, USTC, CCNU (Center China Normal University), Tsinghua University (Beijing)

(Slide from Yanwen Liu (USTC))

ACF material with reduced thickness

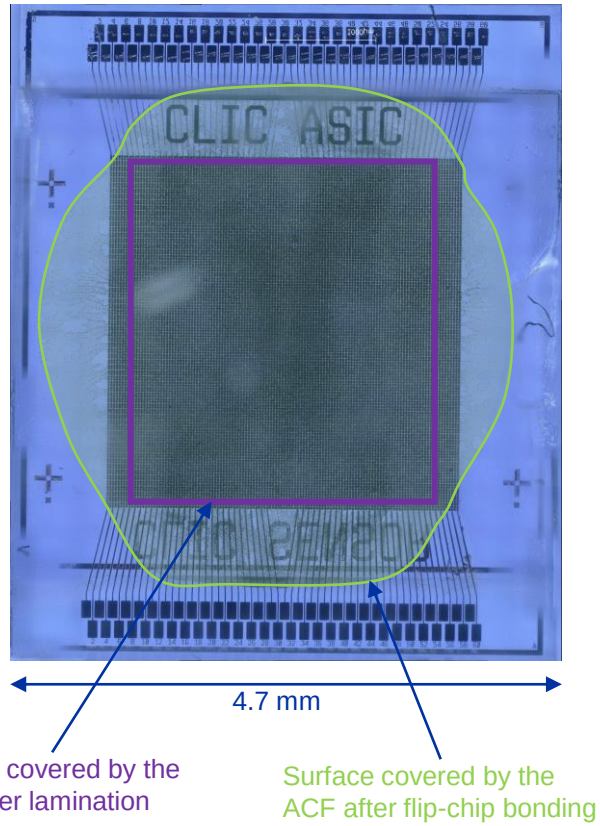
ACF material with reduced thickness



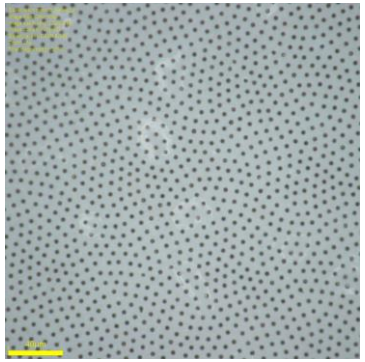
Too thick ACF => Connection problems, especially on large chips

- This problem is solved on small devices by applying a high force during flip-chip bonding, thereby expelling the excess ACF outside the assembly.
- However, this approach is not feasible for large chips, as the force required to expel the excess ACF becomes too high. Another issue is that the distribution of conductive particles is altered and becomes uneven when the ACF is displaced (problem for chips with small pads).
- A new ACF material has been procured, 9 µm thick instead of the 18 µm used until now. An improved interconnection yield is expected, especially for large chips.

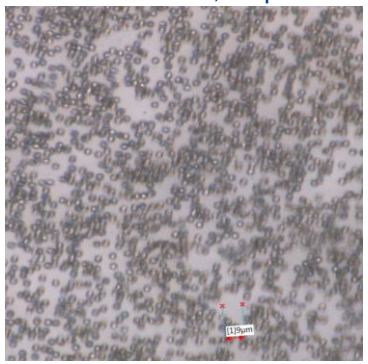
Optical microscope image of the assembly



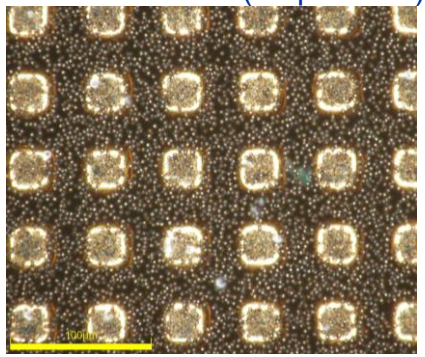
New ACF, 9 µm thick



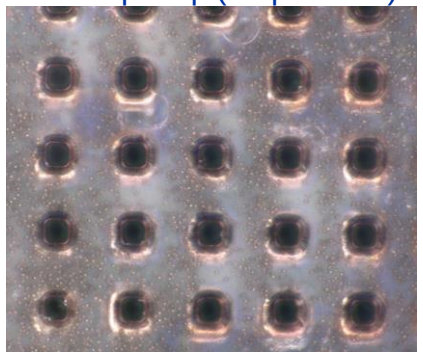
ACF used until now, 18 µm thick



After lamination (18 µm ACF)



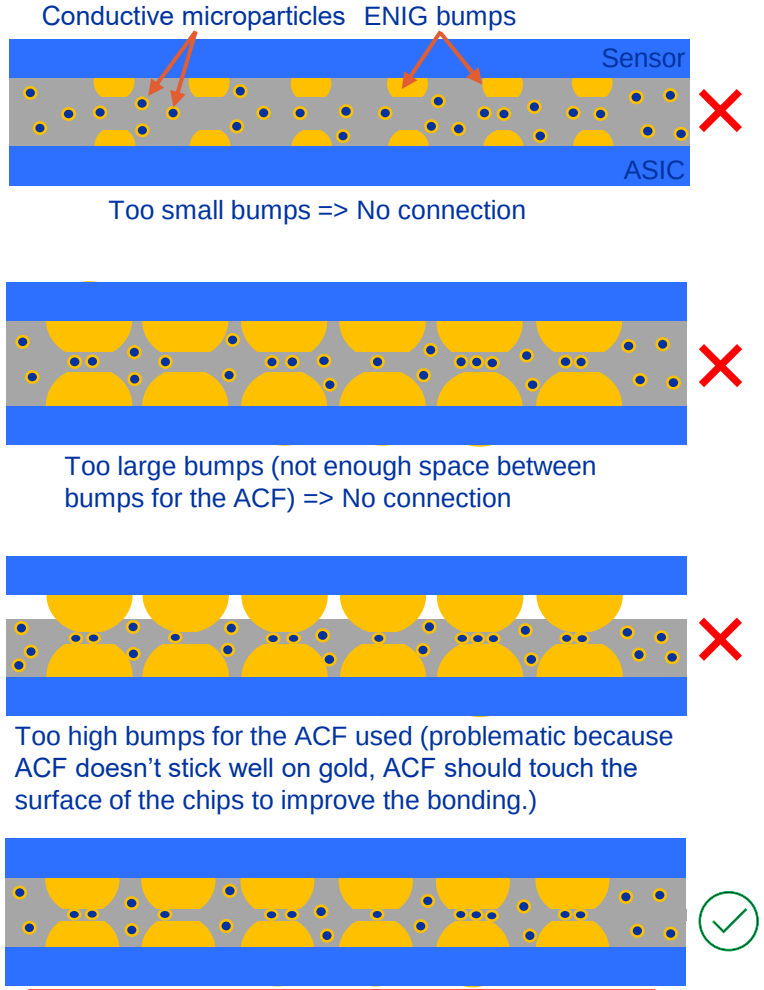
After flip-chip (18 µm ACF)



ENIG Bump height vs ACF thickness optimisation

ENIG Bump height vs ACF thickness optimisation

Bump height vs ACF height optimisation



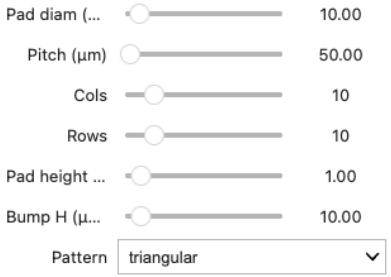
Too small bumps => No connection

Too large bumps (not enough space between bumps for the ACF) => No connection

Too high bumps for the ACF used (problematic because ACF doesn't stick well on gold, ACF should touch the surface of the chips to improve the bonding.)

The goal: bump size adapted to ACF thickness => Good bonding and electric connections

Development of a simulation code for isotropic ENIG growth on chip pads.




```
Pad diameter = 10.0 µm, Pitch = 50.0 µm, Pattern = triangular
Cols x Rows = 10 x 10, Pad height = 1.0 µm
Bump height H = 10.0 µm
→ Volume d'un bump : 5347.003 µm³
→ Volume total bumps : 534700.296 µm³
→ Volume libre entre bumps : 1776183.729 µm³
→ Épaisseur idéale ACF : 8.204 µm
```

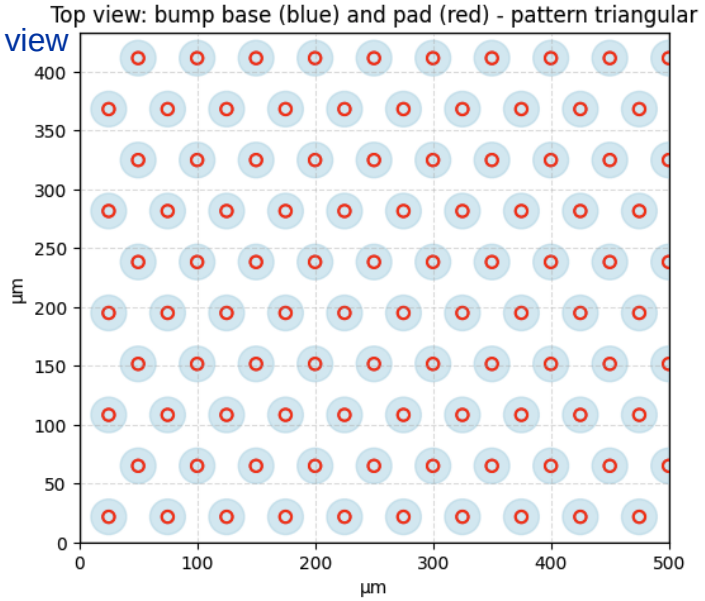
Inputs:

- Pad opening diameter
- Initial height of the pad
- Pitch
- Number of columns
- Number of rows
- Pattern of the pixel matrix (square/triangular)

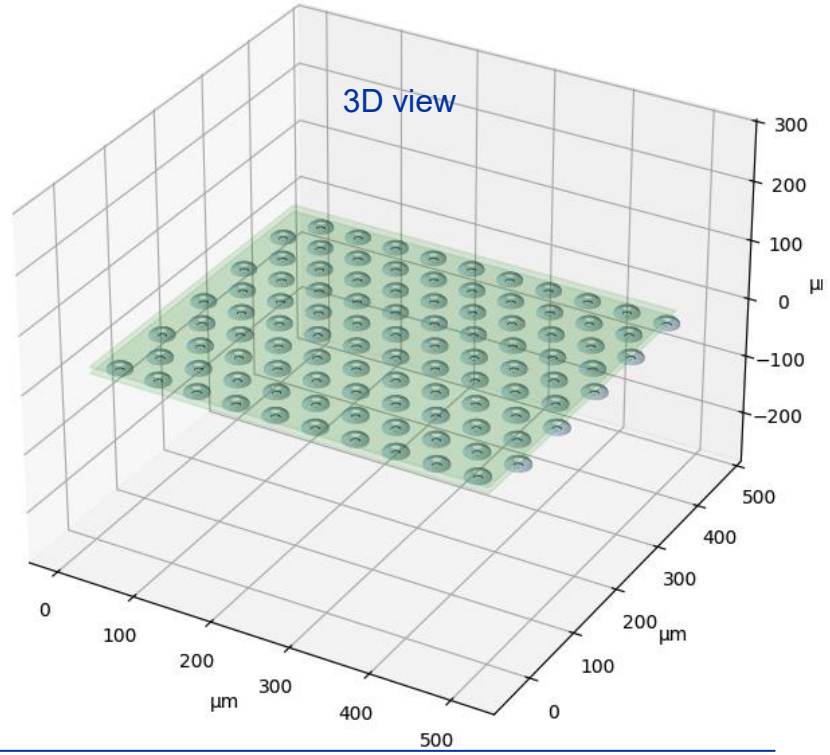
Outputs:

- Optimum height (which maximises the volume available for the ACF)
- Maximum volume between the bumps
- 2D top view of the optimal bumps
- 3D view of the optimal bumps
- Curves showing the evolution of the free volume between the bumps and the maximum ACF thickness that can fit between them

2D top view

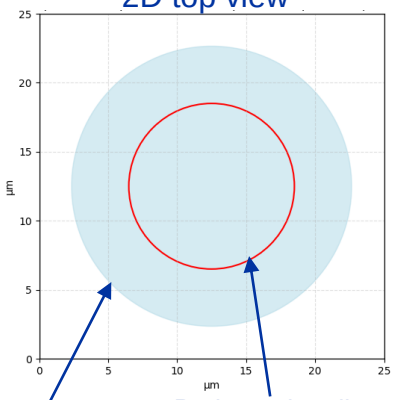


3D view

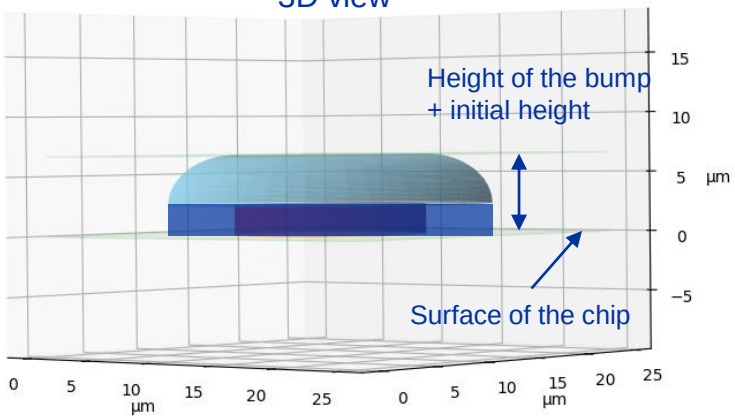


ENIG Bump height vs ACF thickness optimisation

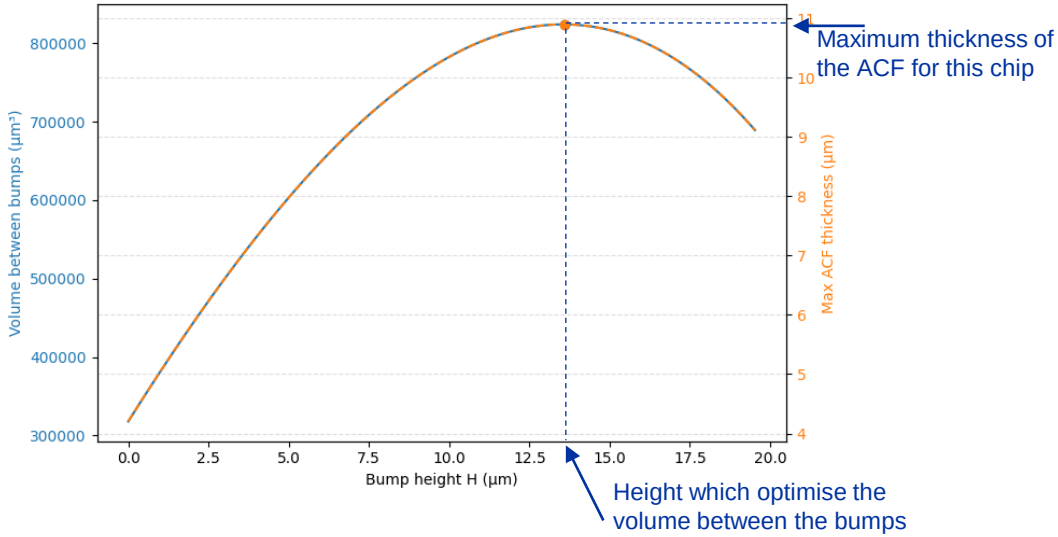
2D top view



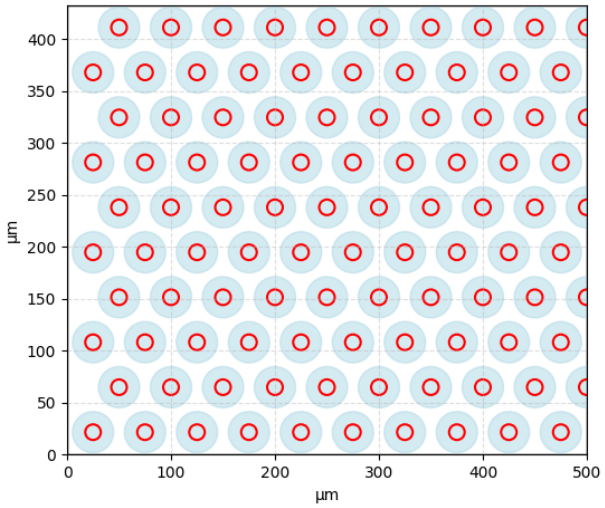
3D view



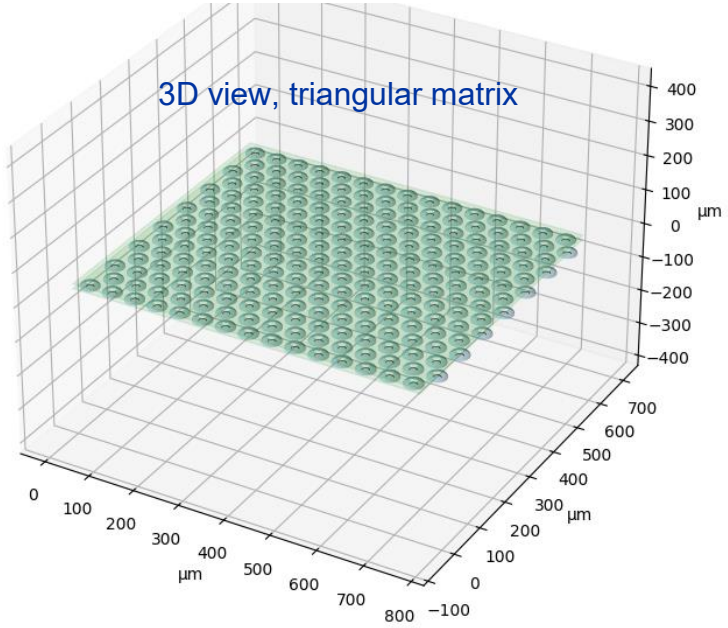
Evolution of the volume between the bumps and the maximum ACF thickness vs bump height



2D top view, triangular matrix



3D view, triangular matrix



Few examples of calculations for previously ENIG plated chips

Chip name	Pitch	Pad opening (measured)	Optimum Bump height[1]	Max ACF thickness
Timespot	55 µm	15.9 µm	13.6 µm	10.9 µm
Timepix3	55 µm	14 µm	16.6 µm	9.4 µm
XPOLL-III	50 µm (triangular)	18 µm	11.6 µm	5.8 µm
ColorPix2	70 µm	40 µm	11.2 µm	5.9 µm

1) Bump height which maximises the volume available for the ACF

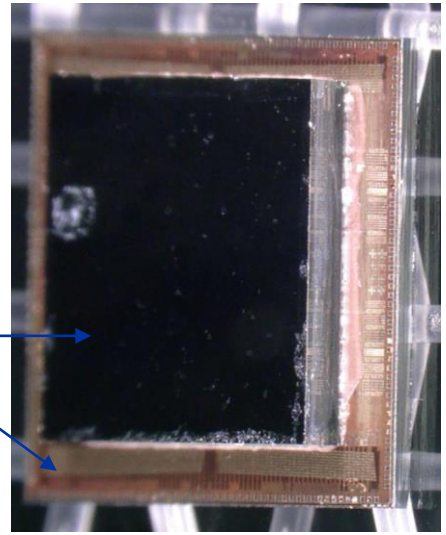
- Dedicated program developed to determine the optimal ENIG bump height and ACF thickness for each chip we want to hybridise

Examples of recent hybridisations

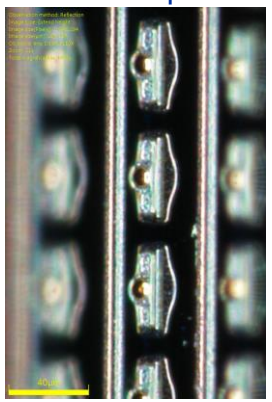
Assemblies done with new ACF

IGNITE ASIC / Si 3D trench sensor hybrid

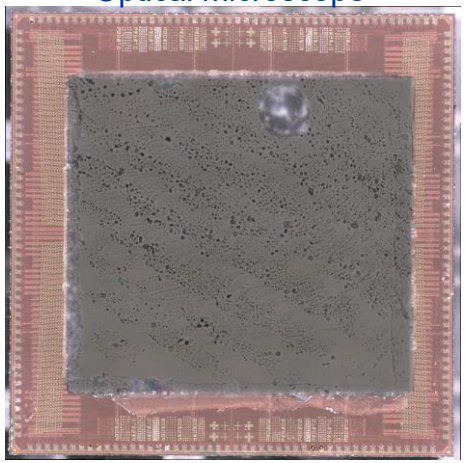
Optical microscope, tilt 40°



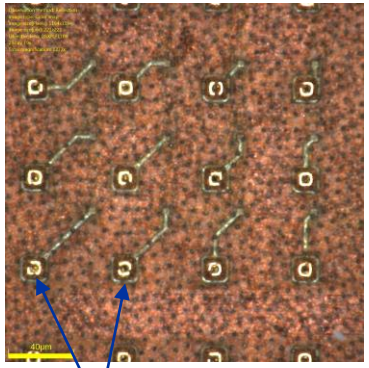
ENIG bumps on sensor, optical microcope



Optical microscope



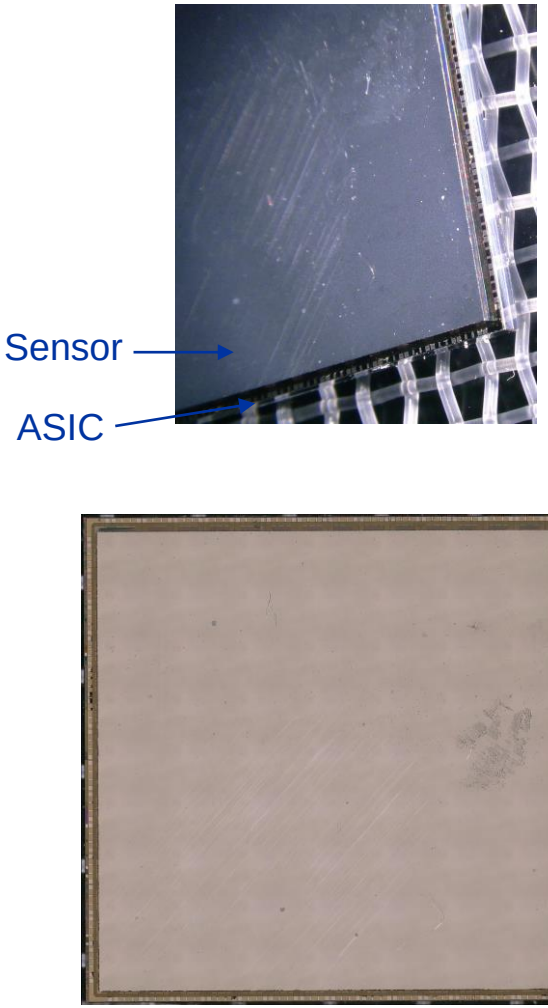
ASIC after ACF lamination



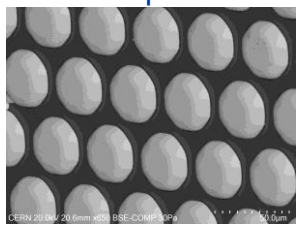
Wirebonded
Not tested yet

Collaboration with INFN Cagliari (Angelo LOI, Adriano LAI)

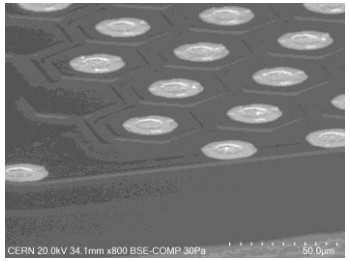
XPOLL-III / Silicon sensor hybrid



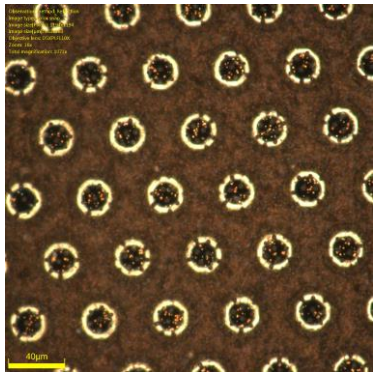
ENIG bumps on ASIC



UBM on sensor



ASIC after ACF lamination

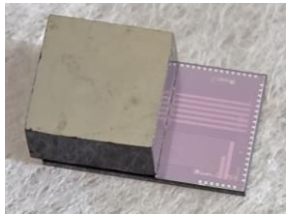


Not tested yet

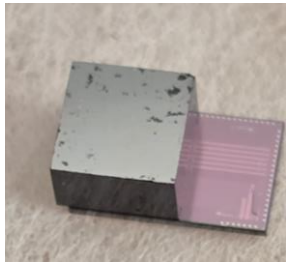
Collaboration with INFN Pisa (Massimo Minuti)

Colorpix2 /CZT hybridisation with non-conductive adhesive (collaboration with Czech Technical University in Prague, Peter Svihra)

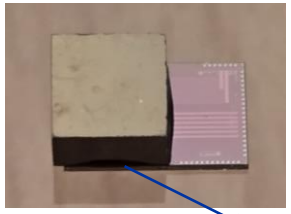
3 hybridisations, Colorpix2 ASIC / CZT sensor



Gold studs on ASIC

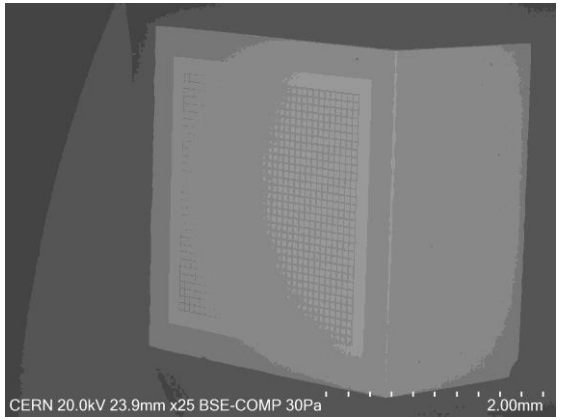


Gold studs on ASIC

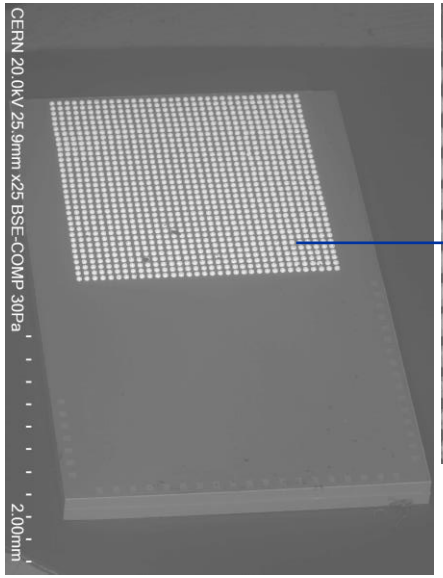


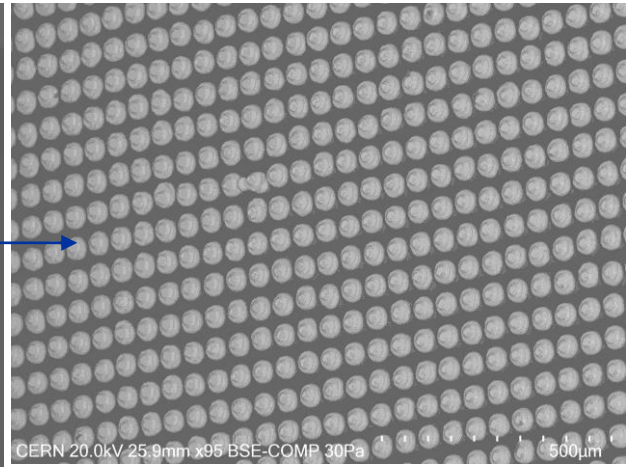
ENIG bumps on ASIC

2 mm thick CZT

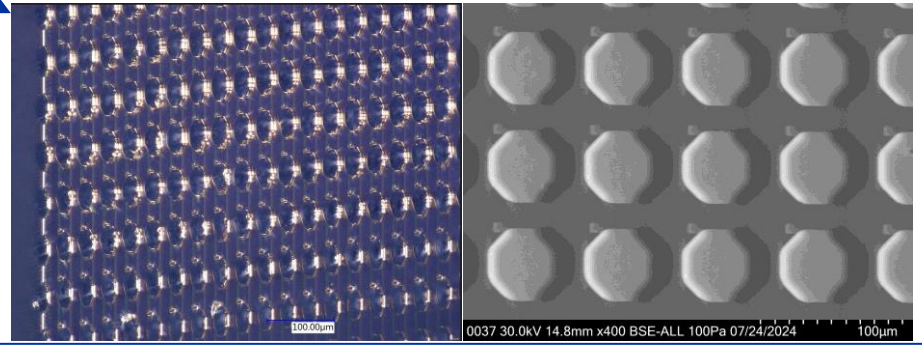


Gold studs deposited in Czech Republic

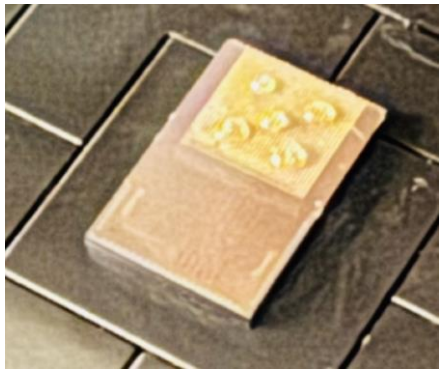




ENIG done at CERN on the ASIC



Araldite 2011 deposited on the gold studs



Flip-chip parameters: 3kgf, 80°C, 30 min

Tests of the hybrids are ongoing

KEK-AC-LGAD/SiGe-ASIC Hybridisation with ENIG and ACF

SiGe ASIC and KEK AC-LGAD sensor

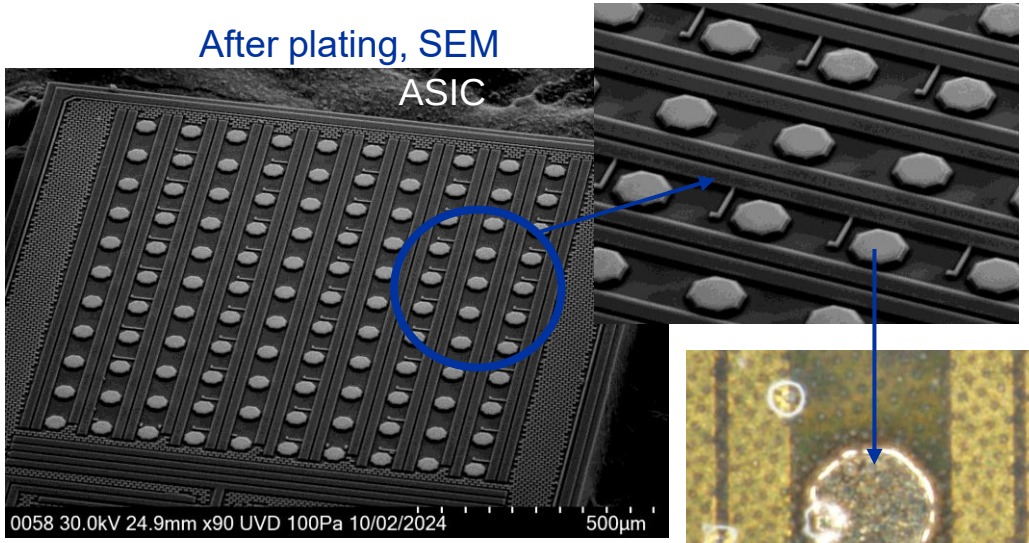
Functional chips
100 µm pitch, 40 µm diameter pads

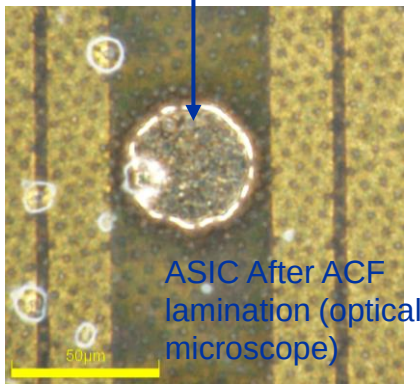
Good ENIG results:
- 100% of pads plated (110 pads)

Collaboration with KEK (Koji NAKAMURA) and University of Geneva (Lorenzo PAOLOZZI)

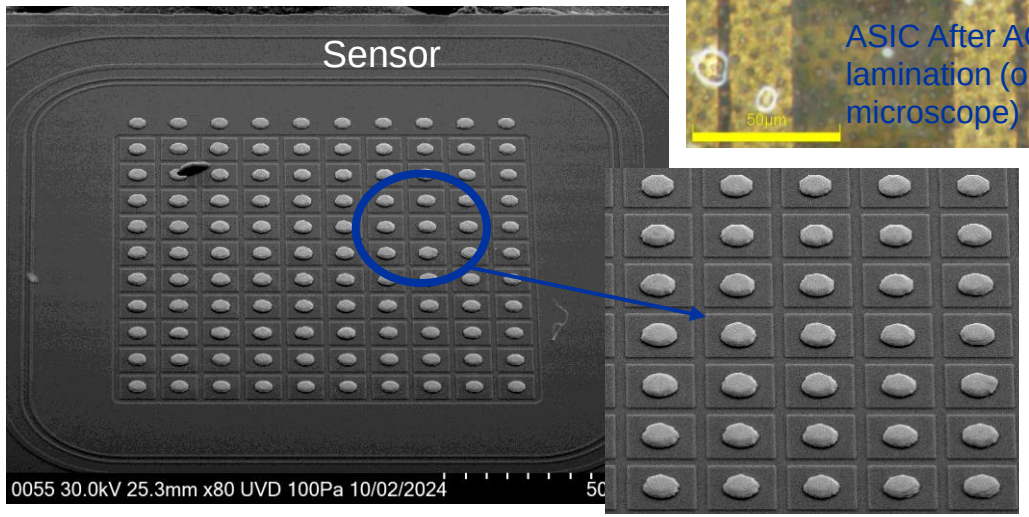
Tomoka Imamura, Sayueka Kita, Koji Nakamura, and Kazuhiko Hara, "Development of HPK Capacitive Coupled LGAD (AC-LGAD) detectors", PoS, vol. VERTEX2023, pp. 032, 2024

After plating, SEM



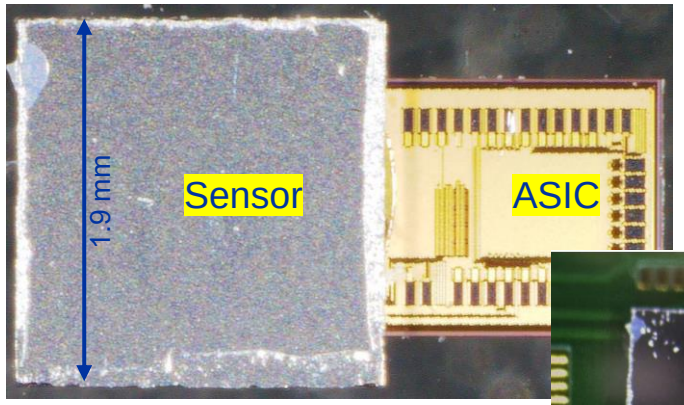


ASIC After ACF lamination (optical microscope)



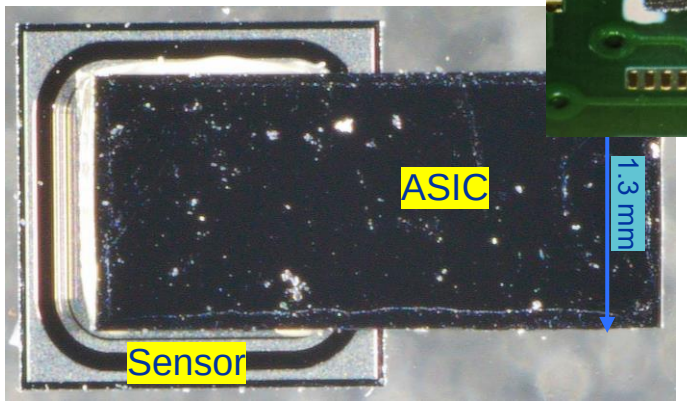
After flip-chip hybridisation

Front side



After wire bonding

Back side



- Very small functional chips have been successfully plated and hybridized. That allowed our colleagues to test their chips
- Characterization of the hybrid partially done. Only 3 pixels tested due to ASIC issues, all connected. More info here: https://indico.phy.ornl.gov/event/677/contributions/2714/attachments/2118/4703/horikoshi_AC-LGAD_Si-GeASIC_vertex2025_horikoshi.pdf

Summary:

- We tested the possibility of hybridisation using ACP on bare aluminium pads, 100% connection yield obtained on two samples. Ongoing work, aging test to be done.
- LATIC1/LGAD hybridisation with ACP after issues with gold stud deposition.
- First flip-chip tests with new ACF material, 9 µm thickness instead of 18 µm used until now.
- ENIG bump-height vs ACF thickness optimisation tool developed.
- Multiple assemblies done, pending test results.
- KEK-AC-LGAD/SiGe-ASIC hybrid partially tested due to ASIC issues. Good connections obtained on the 3 pixels tested.

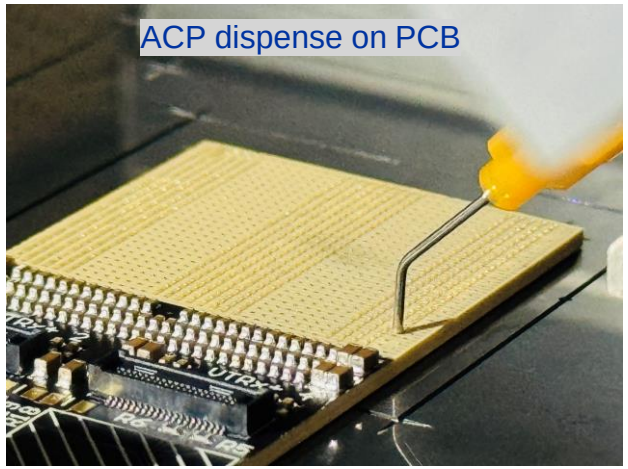
Timepix4 TSV (Through-Silicon-Via) flip-chip bonding with ACP

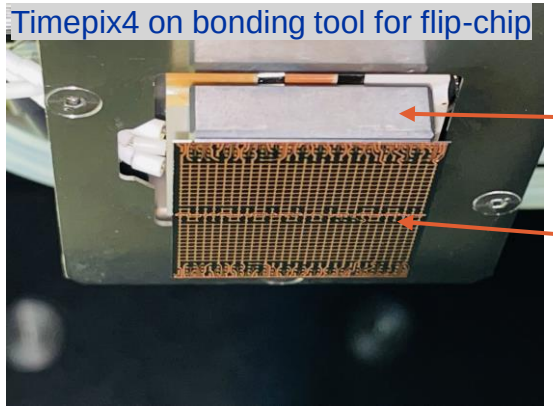
Motivation:

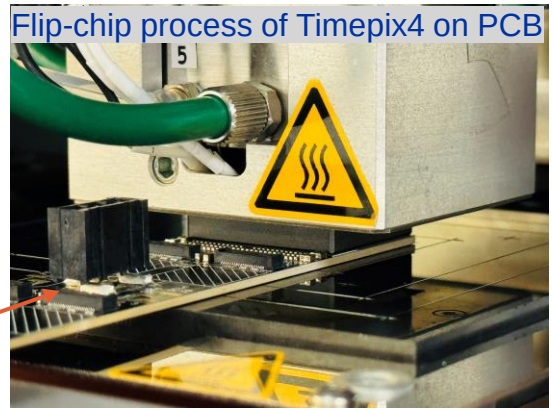
Replace wirebonds by enabling access to the active circuitry (located on the front side of the chip) from the bottom surface of the die using TSVs and ACP.

The ACP bonding process consists of the following steps:

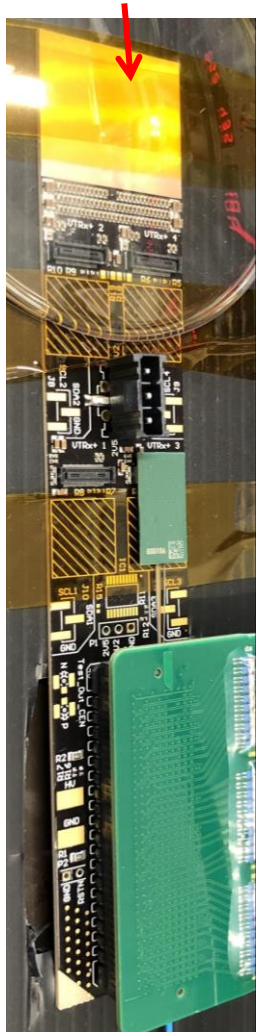
- Mixing the micro-particles with the liquid adhesive
- Dispensing the mix on the pads
- Alignment and flip-chip bonding





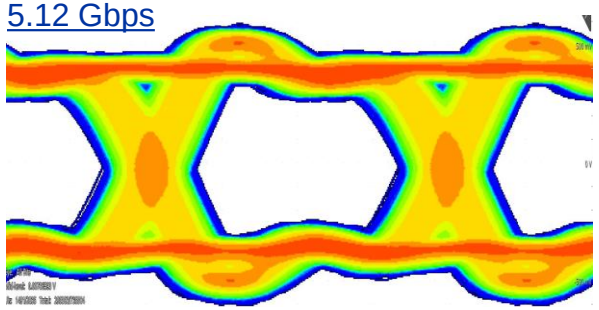


Timepix4 TSV, bonded on PCB with ACP glue

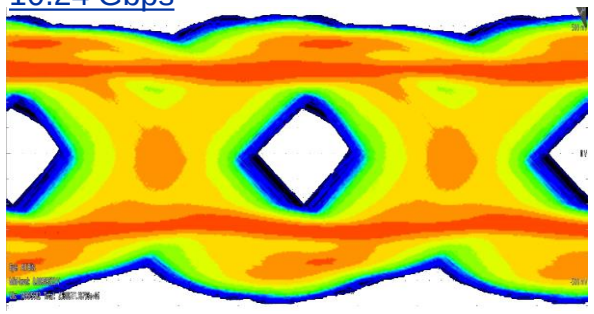


Eye Diagrams Through Optical Fiber

5.12 Gbps



10.24 Gbps

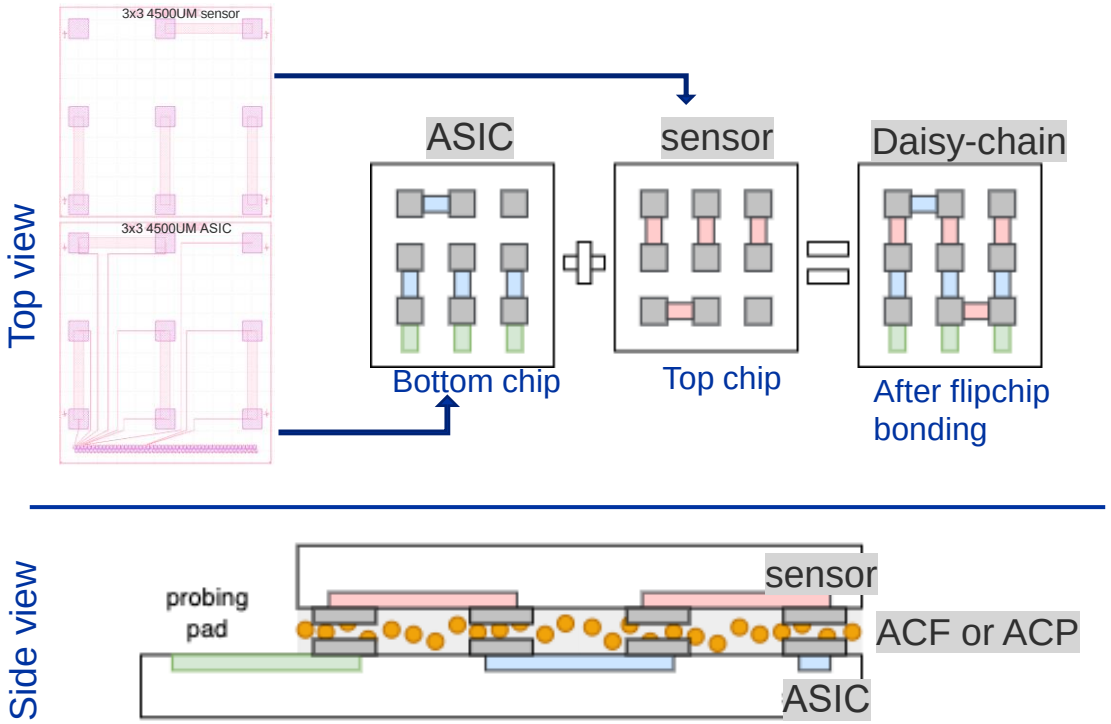


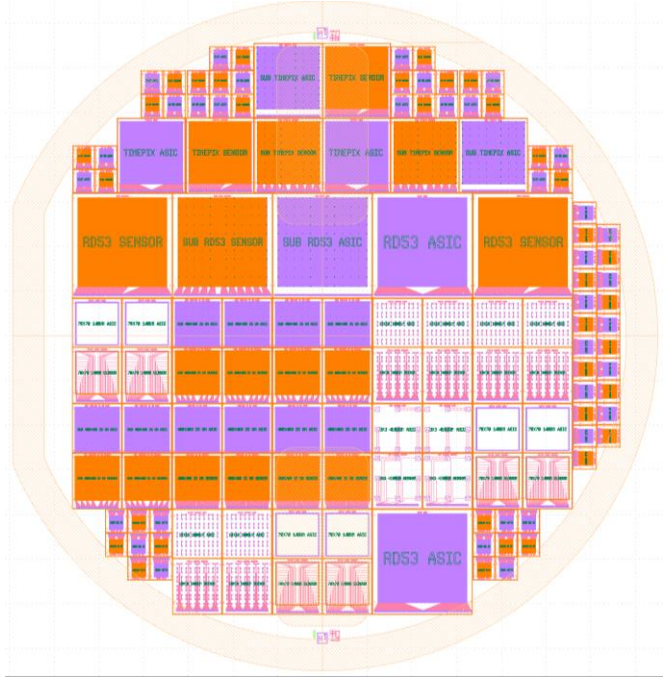
The eye diagrams show that the TSVs are powering the chip and delivering signal even at 10.24 Gbps. (The degradation observed in the 2nd eye diagram is due to limitations of the transceivers at this data rate).

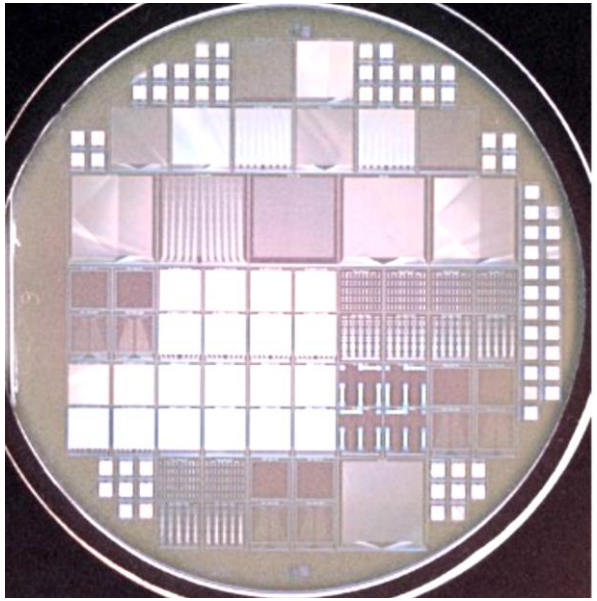
Conclusions:

- TSV with ACP is a possible alternative to wire-bonding.
- Powering and data transmission is proven at gigabit rates through TSVs and ACP bonding.

Test dedicated daisy-chain chips on quartz wafer







	pitch	size in mm	connections	per wafer	type	diceable
160x160 20um	20 um	3.2 x 3.2	25600	36	grid	no
CLICpix2	25 um	3.2 x 3.2	16384	34	grid	no
400x400 25um	25 um	20 x 20	640000	5	grid	yes
Timepix3	55 um	14 x 14	65536	4	grid	no
Timepix3 islands	55 um	14 x 14	65536	4	grid	no
RD53	50 um	20 x 20	160000	4	grid	no
RD53 islands	50 um	20 x 20	160000	2	grid	no
70x70 140um	140 um	20 x 20	2112	3	peripheral	yes
10x10 1000um	1000 um	20 x 20	400	3	grid	yes
3x3 4500um	4500 um	20 x 20	36	1	grid	yes

Daisy chain devices produced at FBK

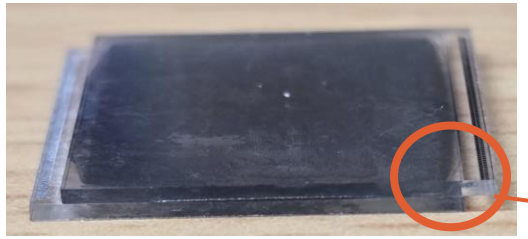
Designed to validate interconnect yield, electrical resistance, thermo-mechanical stress

- 6” quartz wafers, 625 µm thick
- Varying Bonding area, pad size and pitch, matching different target applications

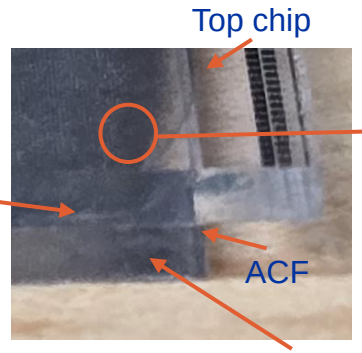
MS24: https://zenodo.org/records/7310324

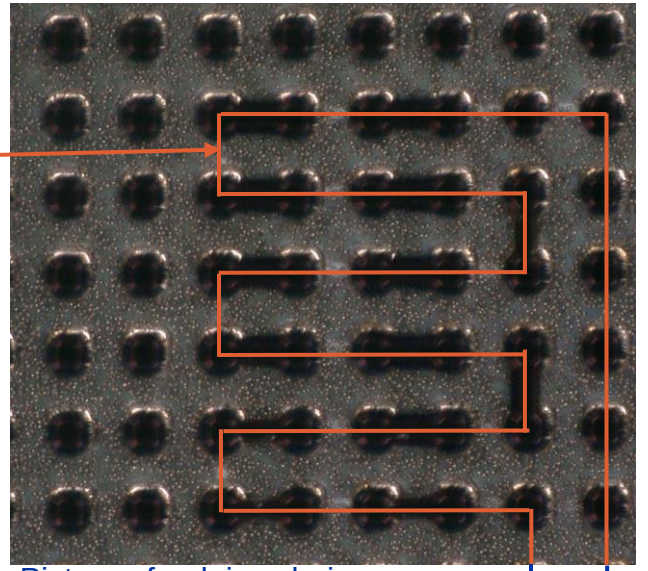
Characterisation of daisy-chain test structures

Anisotropic Conductive Film bonding

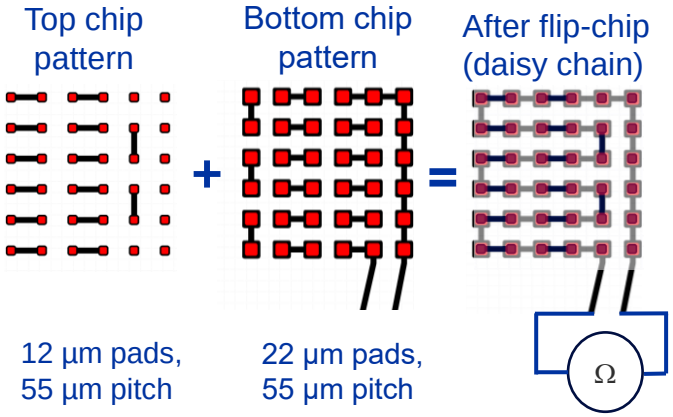


Timepix3 type daisy-chain test chips, flip-chip bonded with 18 µm ACF (3 µm particles)





Picture of a daisy-chain
28 connections in series



Resistance measurement (4-wire sensing)

After flip-chip bonding

- 96.8 % of pads connected

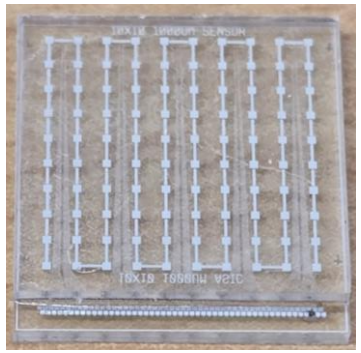
After thermal cycling (25 cycles from -55°C to 60°C, 10°C/min):

- 96.2 % of pads still connected

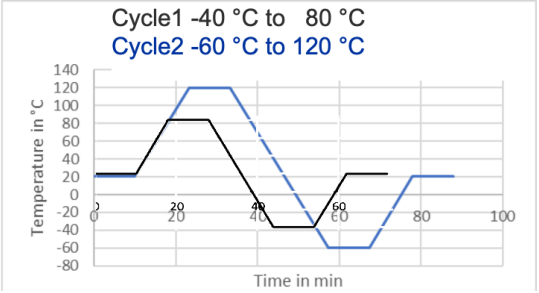
*Test chips produced at FBK with support from AIDAinnova

Anisotropic Conductive Paste bonding

Daisy-chain test chips with 10x10 connections, 300 µm pads, 1 mm pitch, flip-chip bonded with ACP (20 µm Ag particles)



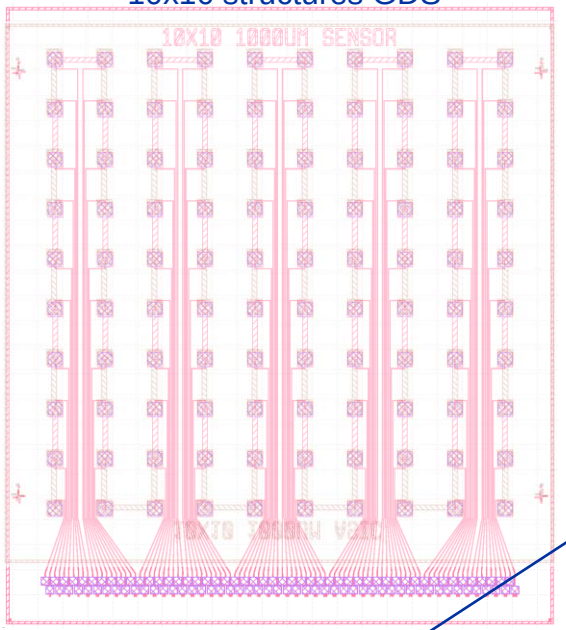
- 98.6 % of pads connected
- After thermal cycling (20 cycles from -40°C to 80°C): 96.8 % pads still connected
- After thermal cycling (20 cycles from -60°C to 120°C): 95.7 % pads still connected



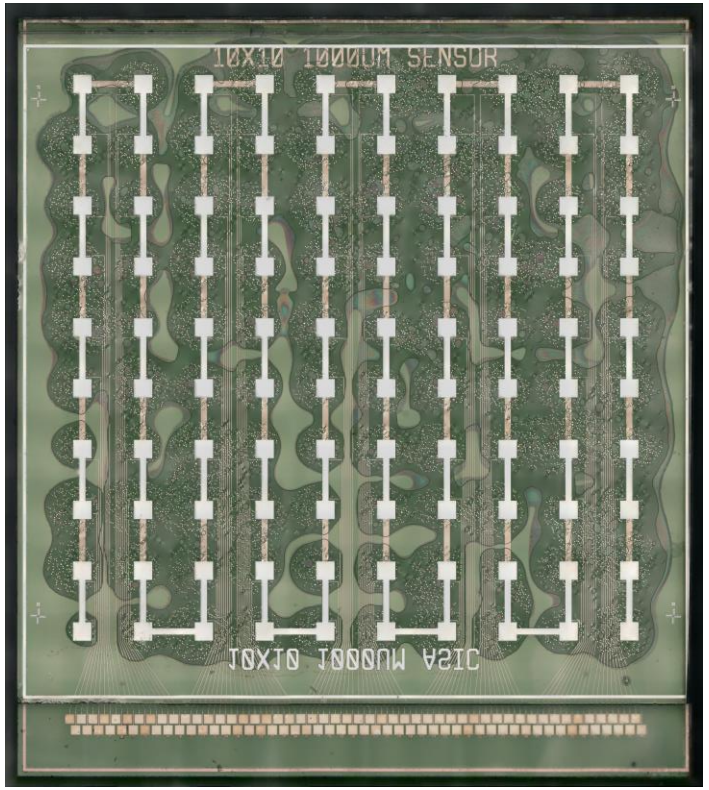
Electrical characterisations

- Probe station at building 14, 6th floor
- 2 wires resistance measurements

10x10 structures GDS



10x10 structures, ACP with spiky particles



Sum of the resistances (chains of 2) 1572 ohm
Full chain (between first and last pad, chain of 100 connections) 606 ohm
Full chain minus the resistance of the lines : 574 ohm
Mean value of the resistance per connection : 5.7 ohm

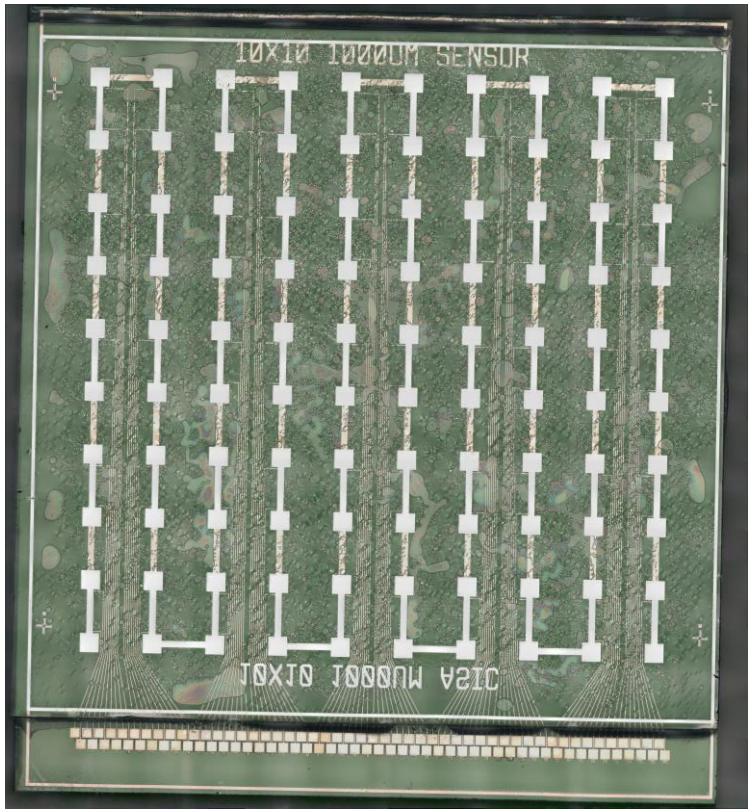
•$L = 700\ \mu m$
•$w = 100\ \mu m$
•$t = 1\ \mu m$
•Section : $A = w \times t = 1.0 \times 10^{-10}\ m^2$
•$\rho \approx 3.0 \times 10^{-8} \Omega$
•$R = 3.0 \times 10^{-8} \times 7 \times 10^{6} = 0.21 \Omega$ (0.2 ohm measured)

There are 99 sections between the connections,
Total resistance of the lines between the connections : 20.79 ohm

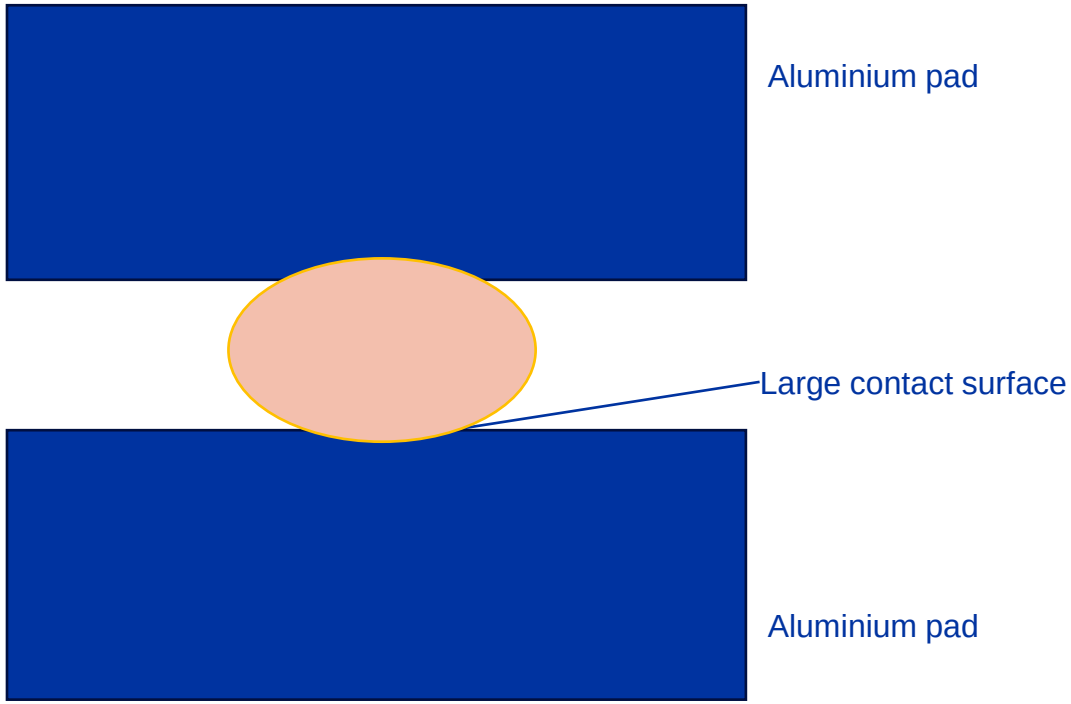
•$L = 1795\ \mu m$
•$w = 10\ \mu m$
•$t = 1\ \mu m$
•Section : $A = w \times t = 1.0 \times 10^{-11}\ m^2$
•$\rho \approx 3.0 \times 10^{-8} \Omega$
•$R = 3.0 \times 10^{-8} \times 1{,}795 \times 10^{8} = 5.385 \Omega$

There are 2 lines to access to the chain, the total resistance of these lines is 10.8 ohm

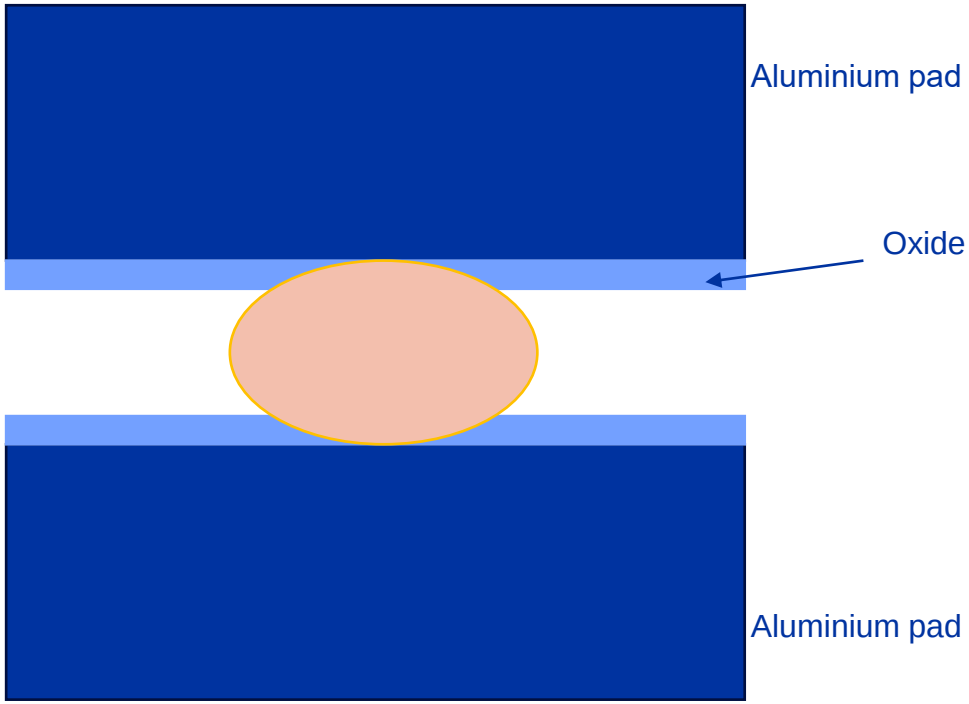
10x10 structures, ACP with regular particles



Sum of the resistances (chains of 2) 1571 ohm
Full chain (between first and last pad , chain of 100 connections) 785 ohm
Full chain minus the resistance of the lines : 753 ohm
Mean value of the resistance per connection : 7.5 ohm



Oxidised pad



Oxidised silver particles??

Introduction

Hybrid pixel detectors:

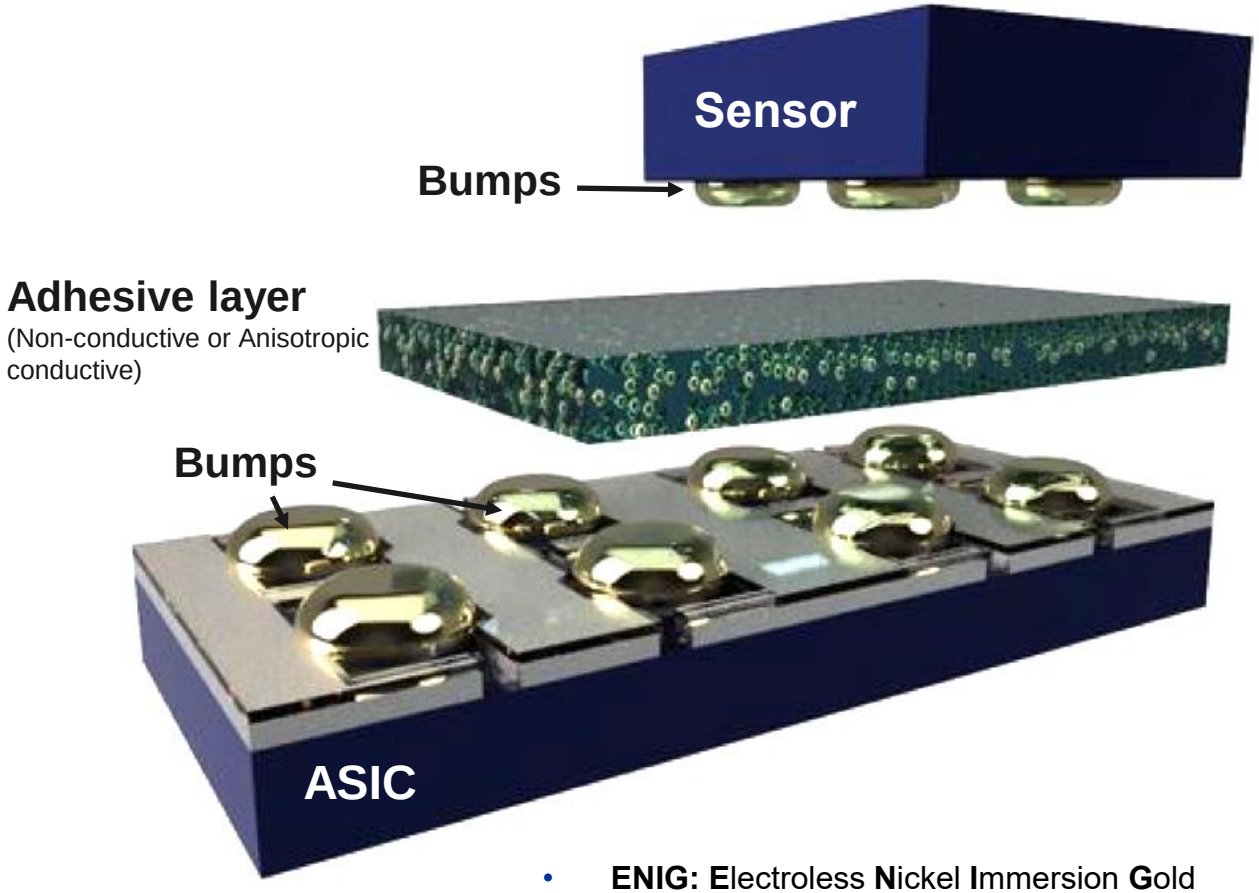
- Independent R&D of sensor and ASIC => Highly customizable and adaptable to specific applications
- Possibility to use different materials for the sensor and the ASIC (CZT, CdTe…)
- One ASIC can serve multiple sensor types, facilitating modularity and reuse
- Requires complex alignment and bonding steps
- The minimal pitch (pixel size) is limited by the size of the bumps connecting the chip

Development of in-house hybridization techniques in two main steps:

1. Bumping: creation of bumps on the pads of Sensor and ASIC with ENIG plating, gold studs…
2. Flip-chip assembly with an adhesive layer between the chips (anisotropic conductive or non-conductive adhesive)

Advantages:

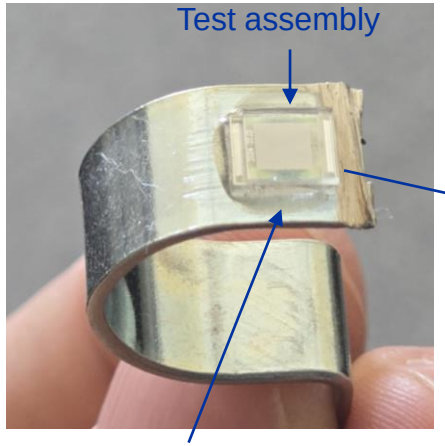
- Single die processing (important for chips from MPW)
- Easily adaptable to the application
- Low temperature process
- Maskless
- In-house (short turnaround time, quick adjustments)

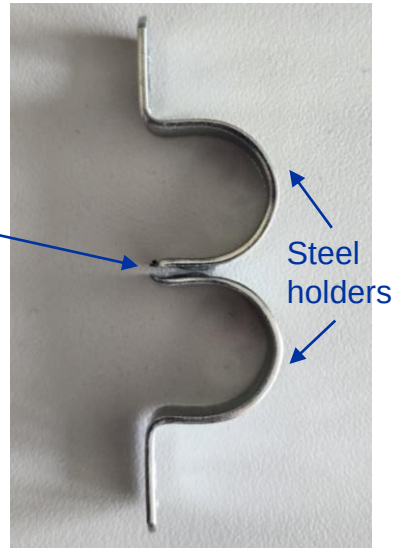


- **ENIG:** **E**lectroless **N**ickel **I**mmersion **G**old
- **ACA:** **A**nisotropic **C**onductive **A**dhesive
- **ACF:** **A**nisotropic **C**onductive **F**ilm
- **NCA:** Non-**C**onductive **A**dhesive

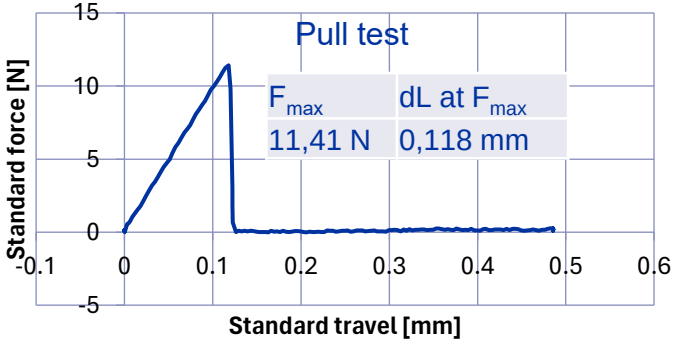
Flip-chip hybridisation of high connection density test chips

Separation of the chips using a pull tester to characterize the interface between them

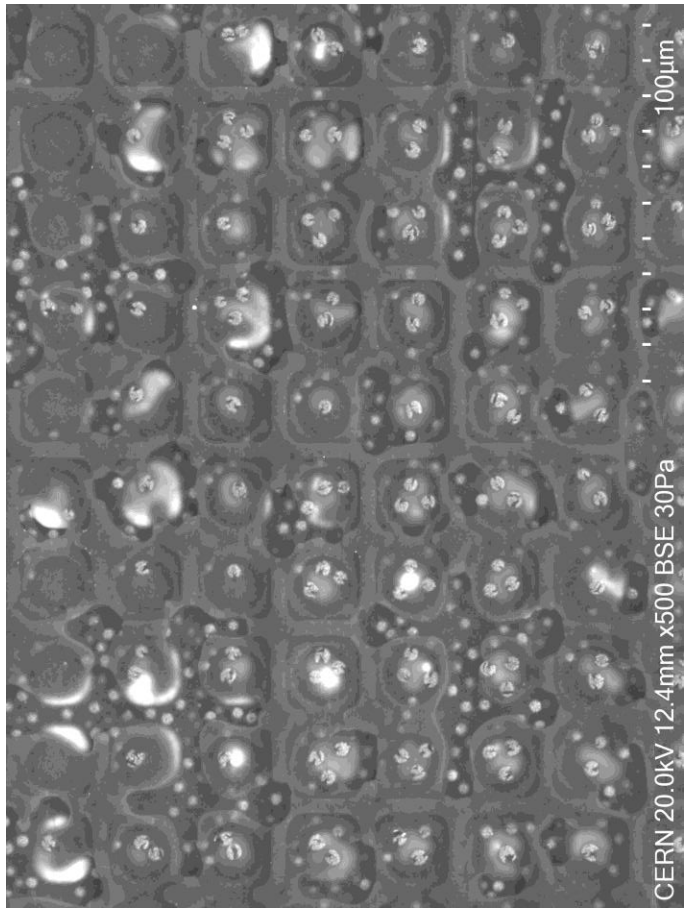




- Surface of the ACF gluing the 2 chips ≈ 15.5 mm^2
- Breaking force: 11.4 N
- Adhesion force of the ACF ≈ 0.73 N/mm^2 ≈ 7.2 kg/cm^2

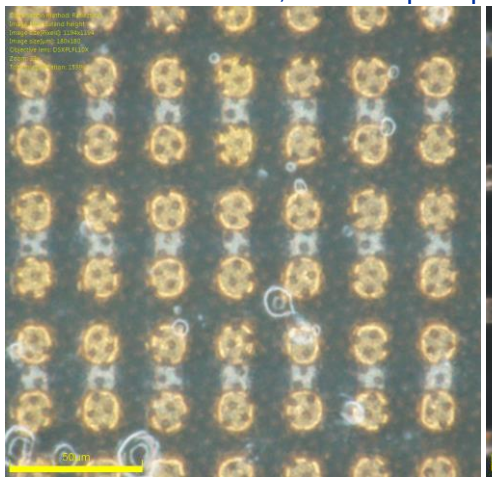


Observation of the chips interface (SEM)

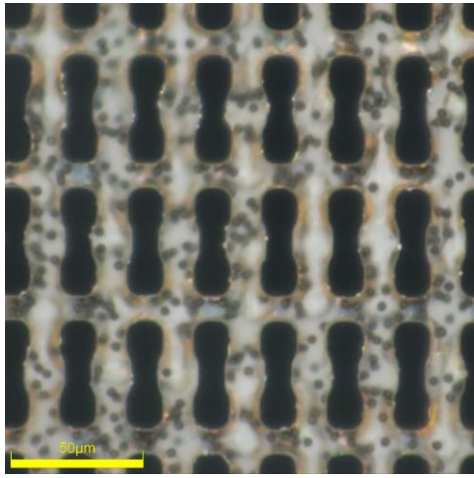


~90% of bumps with at least 1 conductive microparticle on them after separation.

After ACF lamination, before flip-chip



After flip-chip



Displacement of particles during the flip-chip bonding due to the non-adapted thickness of the ACF. The excess ACF flows toward the edges of the assembly. (The bump height is 4.5 µm on both chips, and the conductive particles are 3 µm in diameter, resulting in a total stack height of approximately 12 µm, significantly lower than the 18 µm thickness of the ACF.)

Conclusion:

First results for ACF bonding on chips with very small pads (10 µm) and pitch (25 µm), the process still requires further optimization to ensure reliability and yield at this scale.

Improvement areas identified:

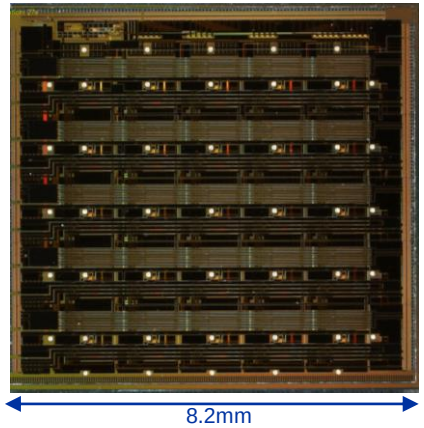
•Use a thinner ACF to reduce particle displacement during flip-chip bonding.

•Increase plating time to enlarge bump surfaces and improve the probability of capturing conductive particles.

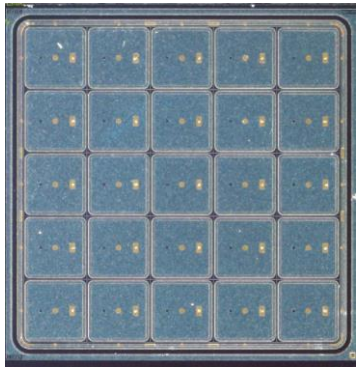
Gold-stud hybridisation of LATIC2 ASICS

- Hybridisation of 2 LATIC2 ASICs (130 nm TSMC) with 2 USTC-IME v2.1 LGAD sensors
- 5x5 pixels, 1.3mm square pitch
- Processing steps:
  - Deposition of double gold studs on LATIC2 ASICs at HybridSA
  - 10 min argon plasma cleaning for both ASICs and sensors
  - Applying Araldite 2011 glue on ASIC in 4 lines between gold studs
  - Flip-chip of ASIC and sensor, thermo-compression bonding with 5 kg force and 100°C for 7 min
  - Backside thinning of sensor (because of design issue preventing wire bonding for thick sensor)
- Test results for 1 hybrid (→ presentation by Zhuang Li in WG2 session):
  - Sensor IV not affected by flip-chip and wire bonding
  - 100% interconnection yield for 24 functioning channels (1 channel with ASIC issues)
  - First performance results with electrical pulses, laser and Sr90

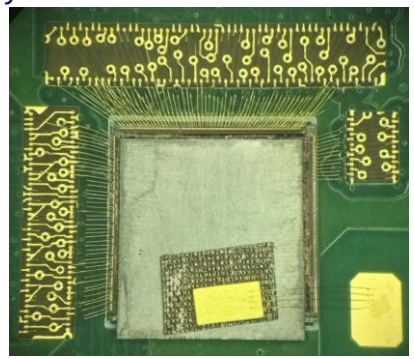
Double gold studs on LATIC2 ASIC



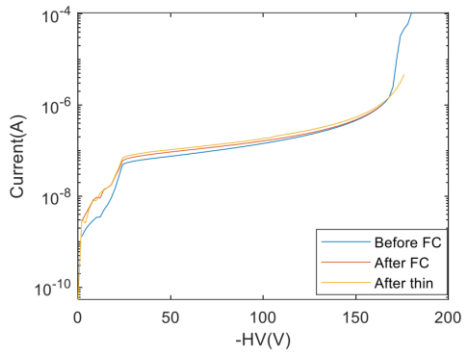
USTC-IME v2.1 sensor

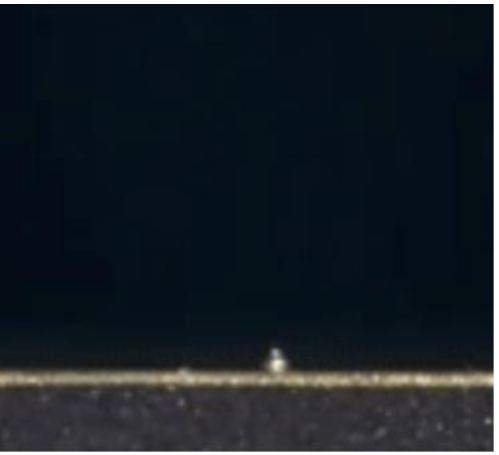


Hybrid wire bonded to PCB



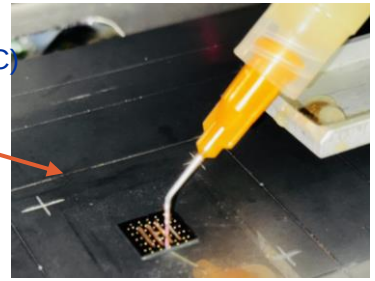
Sensor IV before and after processing



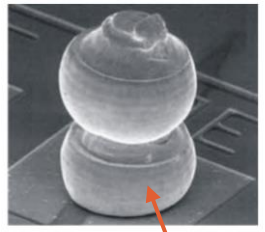


Gold studs are deposited one by one
https://www.youtube.com/watch?v=ICRDBpmev4o&t=42s&ab_channel=TPT-Wirebonder

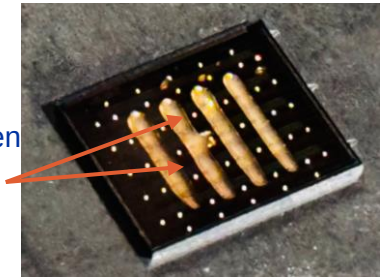
NCP (Araldite 2011) dispense before flip-chip (on LATIC2 ASIC)



Stacked Gold studs



NCP between gold studs



35 µm gap between ASIC and sensor avoid sparks at the edges of the chips.

Conclusion:

- The hybridisation process using double gold studs was applied to a new chip.
  An excellent connection yield was achieved, allowing our colleagues to successfully test their new chips.