

# Fabrication Progress and Performance Characterization of SICAR

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*The 4th DRD3 week*

## ● Key Process Characteristics

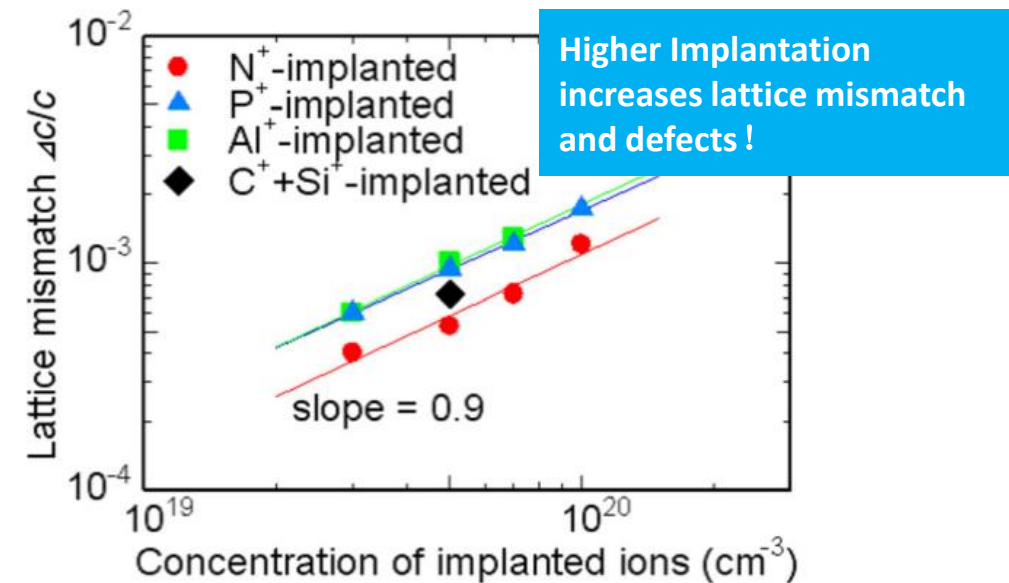
- Full epitaxial growth including N- active region, N+ gain layer and P++ layer
- Etching termination with Field plate
- No high temperature ion implantation and high temperature post-annealing

## ● Advantages

- Avoiding Implantation-Induced Lattice Damage and mismatch
- Enhanced Crystallinity
- Single Crystal Quality

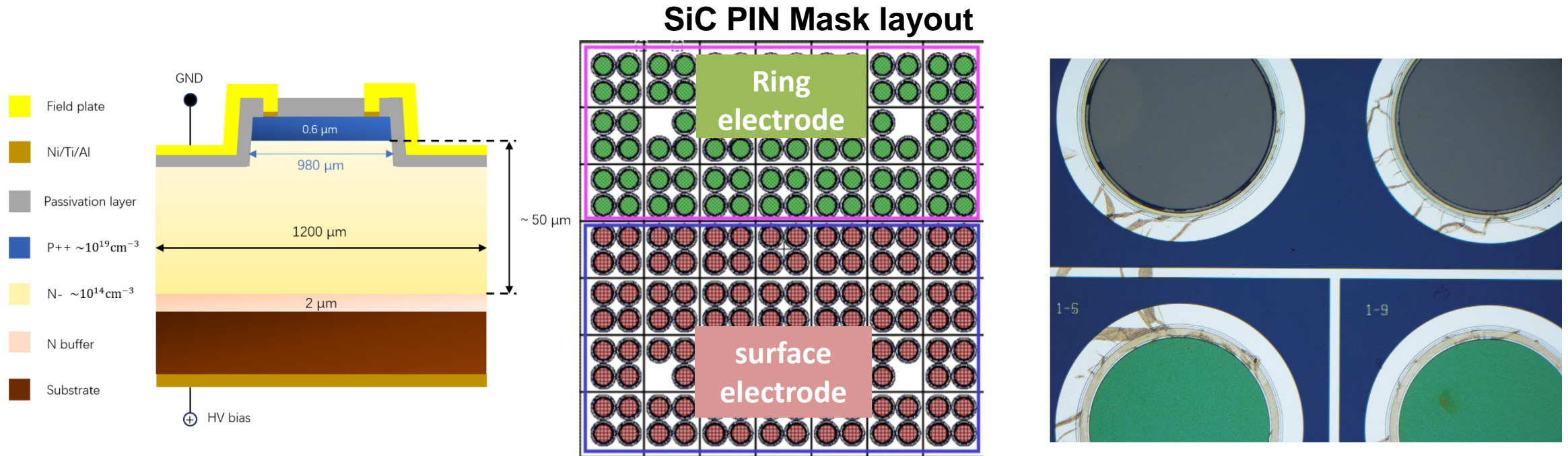
## ● Disadvantages

- Incompatible with other termination techniques (JTE/guard ring)



<http://dx.doi.org/10.1063/1.4720435>

- Devices completed in Aug.
- **Lift-off Failure due to Incomplete Photoresist Removal** → **Yield Dropped to 25%**

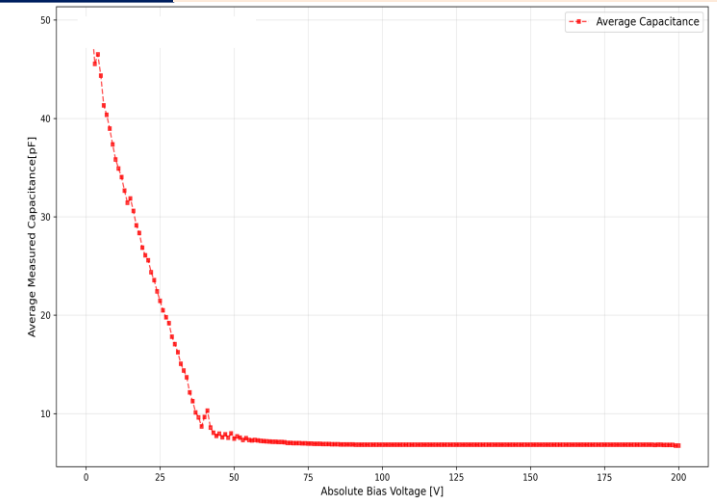
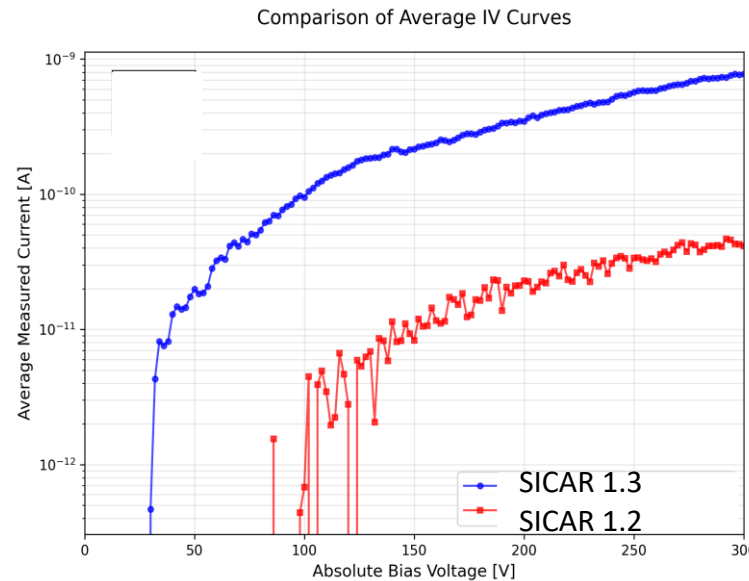
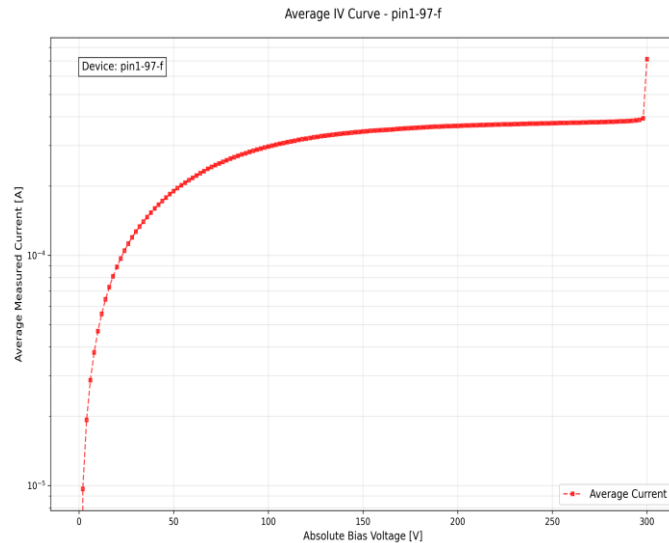


- PR Lift-off challenges caused by deep etch termination
- Residual PR left on the metal

- The CV characteristics of SICAR 1.3 are unchanged from SICAR 1.2.

- Full depletion voltage ~ 95V
- The doping concentration of active region ~  $1.8 \times 10^{14} \text{ cm}^{-3}$
- The full depletion depth reaches ~ 29  $\mu\text{m}$

- PR residue affected the leakage current in most of devices.



Quantity too low to distribute to WG6-SiC-LGAD project members

- The leakage current of most devices reach over 100  $\mu\text{A}$  at 50 V.

- The current of some devices is on the order of nA at 300 V.
- ~2 Orders of Magnitude Higher Current vs. SICAR 1.2

## ● Dose Rate calibration

### • Principle:

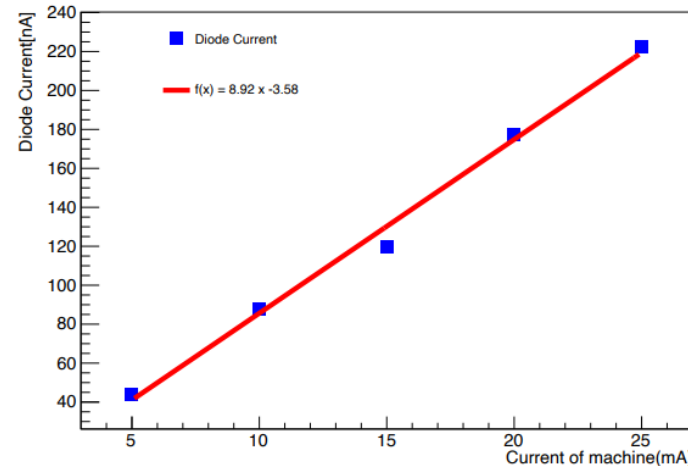
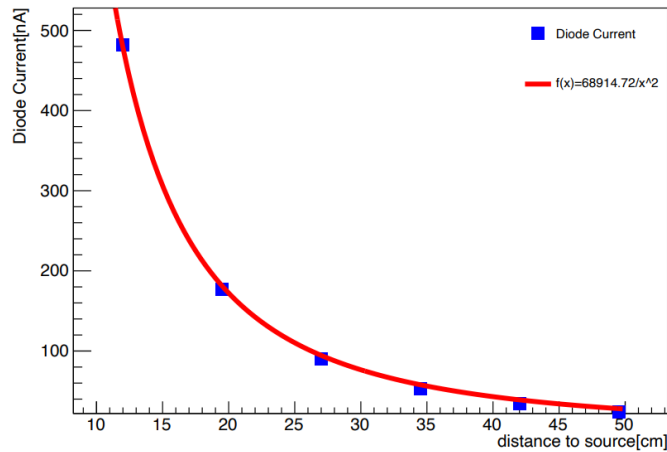
✓ DR (Dose Rate of X-ray) :  $kD \times ID$

✓  $kD$  (Current-to-Dose Coefficient) =  $52.0725 \frac{\text{rad}}{\text{min} \times \text{nA}}$  (Provided by CERN)

✓  $ID$ : Measured diode current via KEITHLEY SourceMeter

• Check the inverse square relation between diode current and distance

• Check the linear relation between diode current and X-ray current



• Machine: MultiRad 160 @ 40keV



- **X-ray Dose**

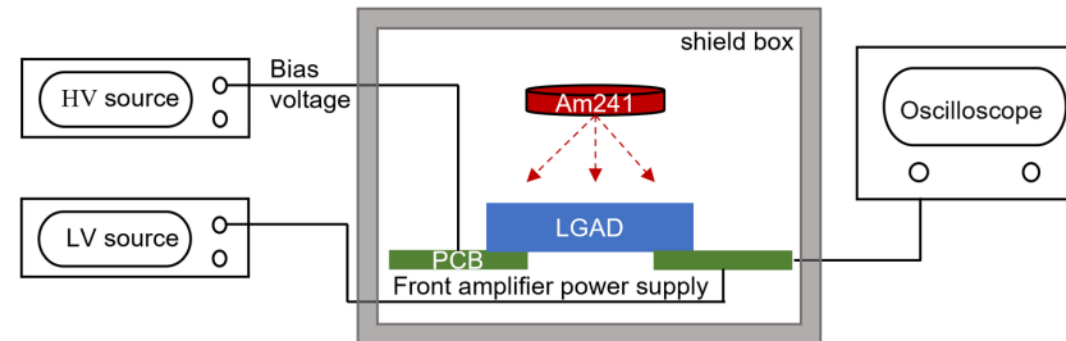
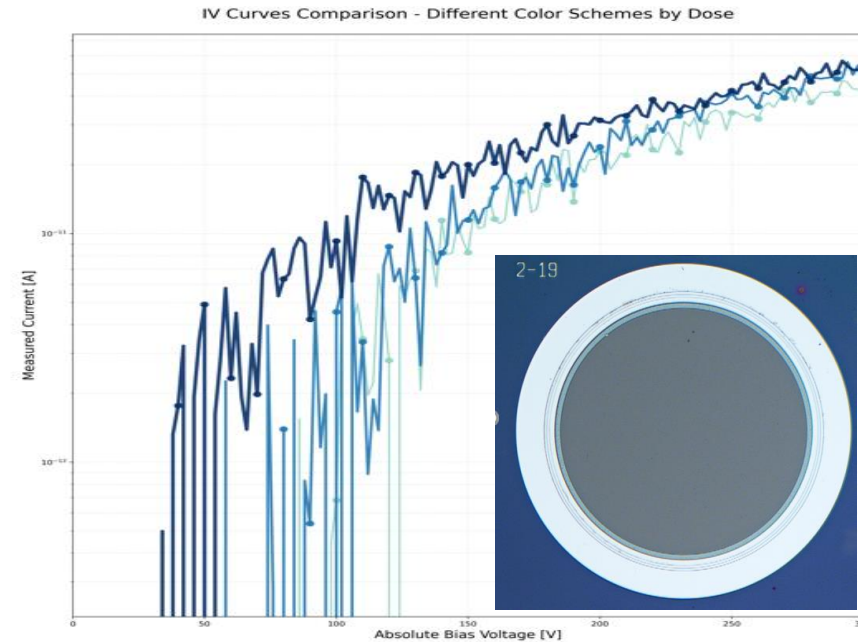
- 0.5MGy/1MGy/2MGy

- **Leakage current**

- Negligible increase with rising radiation dose

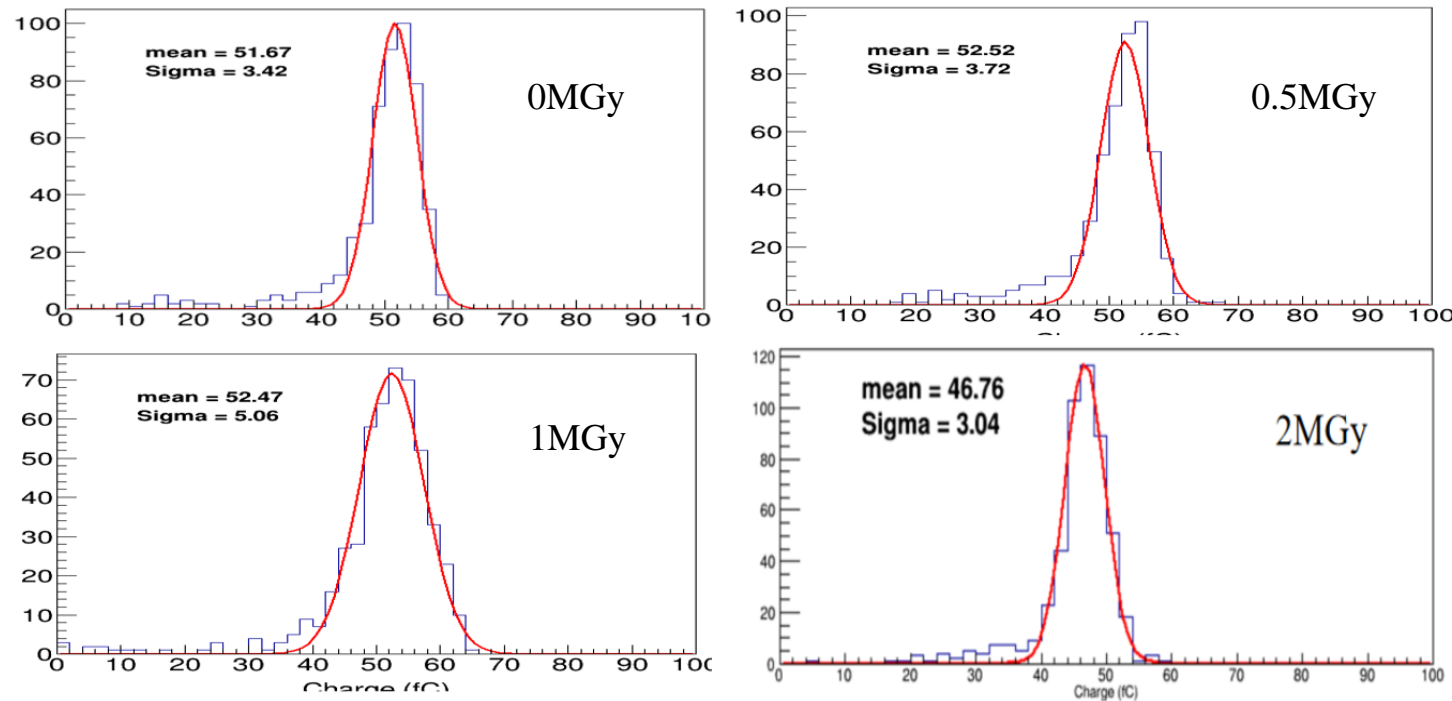
- **Alpha source setup**

- Americium-241
- In shield box
- No 2<sup>nd</sup> amplifier
- UCSC test board



- Alpha source measurement

- CCE remains stable with the increased irradiation from 0MGy to 1MGy
- The charge collection at 2 MGy decreased by 11.5% compared to that at 1 Mgy
- Promising X-ray radiation hardness

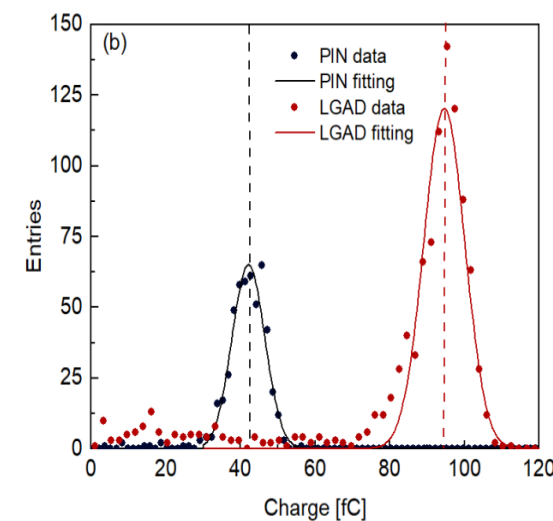
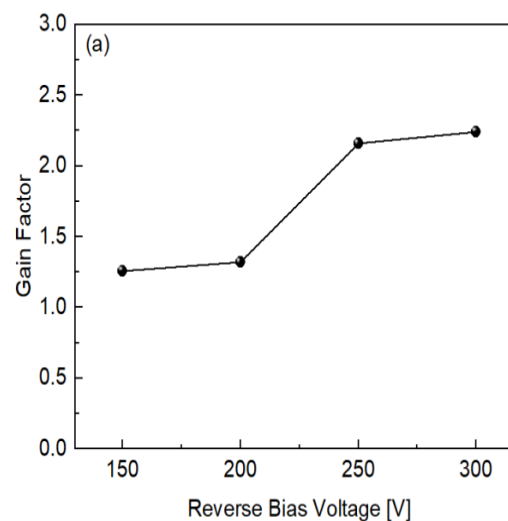
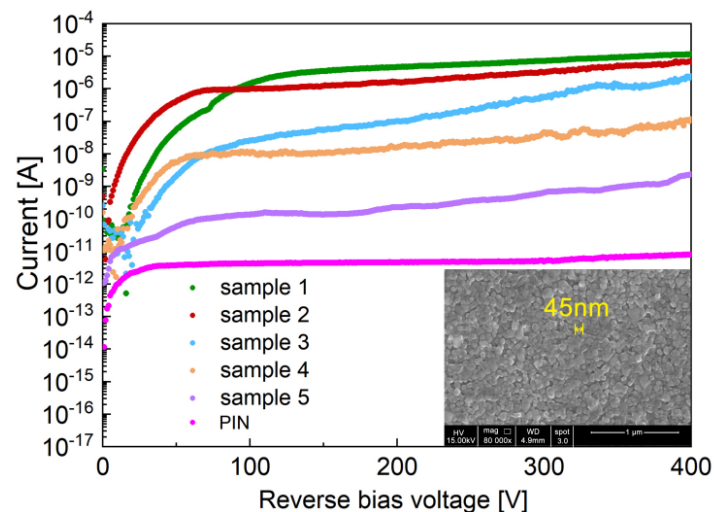
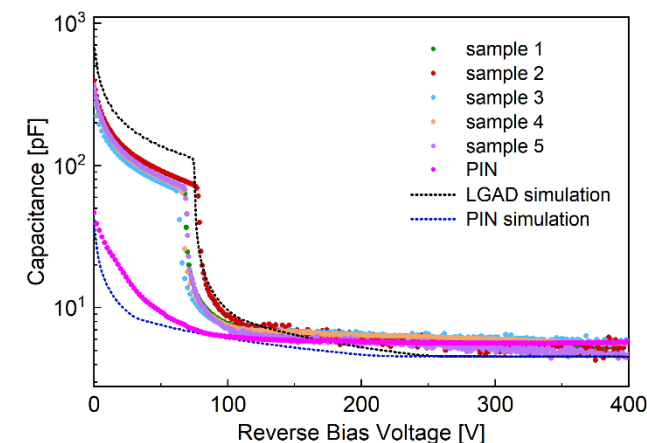
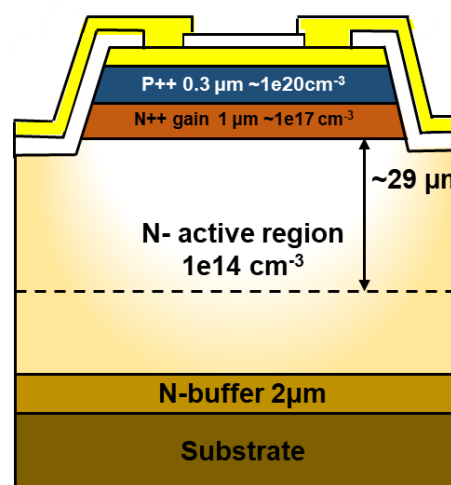


- The next plan is to validate the X-ray hardness using the beta source

## ● Structure and characteristics of SICAR1\_LGAD

- N- active region: thickness  $\sim 50 \mu\text{m}$ ,  $N_d \sim 3.8 \times 10^{14} \text{ cm}^{-3}$
- N++ gain layer : thickness  $\sim 1 \mu\text{m}$ ,  $N_d \sim 1 \times 10^{17} \text{ cm}^{-3}$
- The full depletion depth reaches  $\sim 29 \mu\text{m}$
- Depletion voltage of the gain layer  $\sim 75\text{V}$
- Full depletion voltage  $\sim 150\text{V}$
- Gain factor  $\sim 2$  @  $300\text{V}$  (Calibrated by Alpha source CCE)

LGAD-1 epitaxial structure



● The consistency needs to be improved!

● The gain factor needs to be increased!

[1] [10.1109/TNS.2024.3471863](https://arxiv.org/abs/10.1109/TNS.2024.3471863)

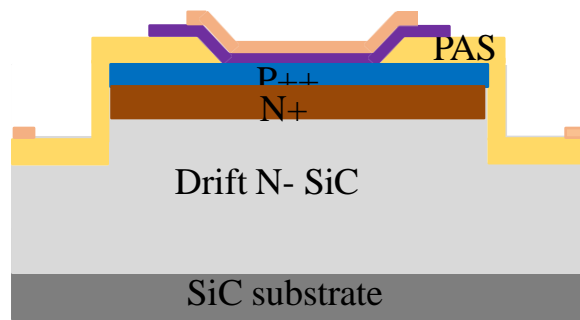
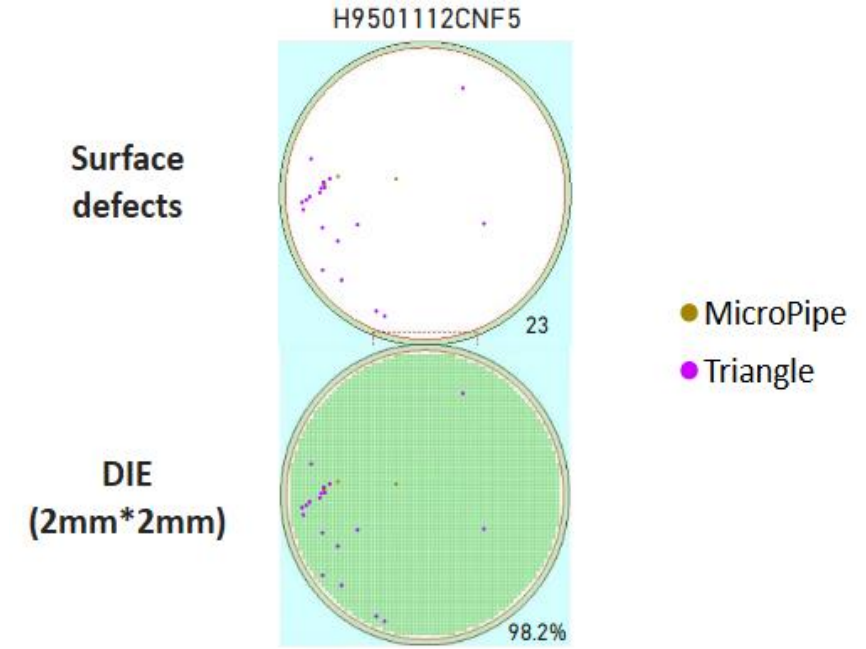
[2] [arXiv:2507.12238 \(2025\)](https://arxiv.org/abs/2507.12238)

## ● Epitaxial wafer of SICAR2\_LGAD (6-inch)

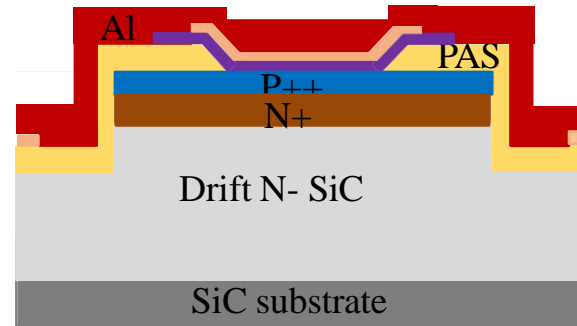
- Epi wafer yield: 98.2%
  - ✓ N- active region: thickness  $\sim 50 \mu\text{m}$ ,  $N_d \sim 1e14 \text{ cm}^{-3}$
  - ✓ N++ gain layer : thickness  $\sim 0.5 \mu\text{m}$ ,  $N_d \sim 4e17 \text{ cm}^{-3}$
  - ✓ P++ layer : thickness  $\sim 0.3 \mu\text{m}$ ,  $N_a \sim 1e19 \text{ cm}^{-3}$
- Objective: gain factor  $> 10$  @ 300V

## ● Optimize the process flow to enhance the yield rate

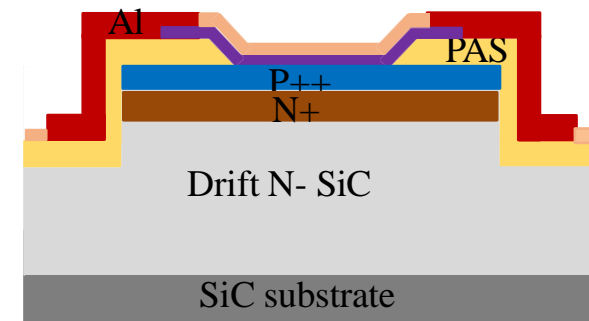
- Adopt Wet Etch for Metal Pads
- Bypassing lift-off challenges caused by deep etch PR residues



Dry Etch Opening



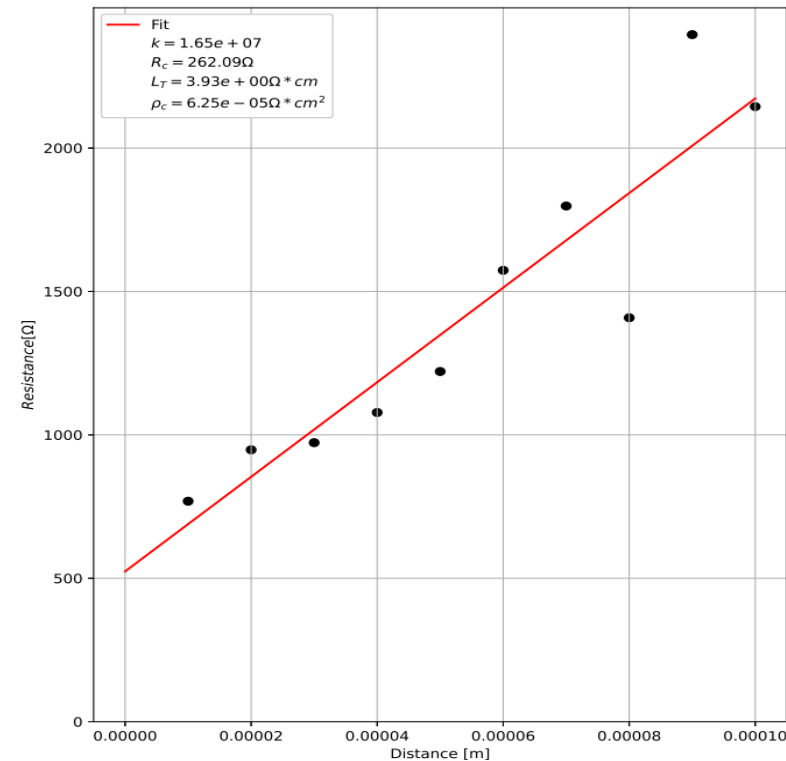
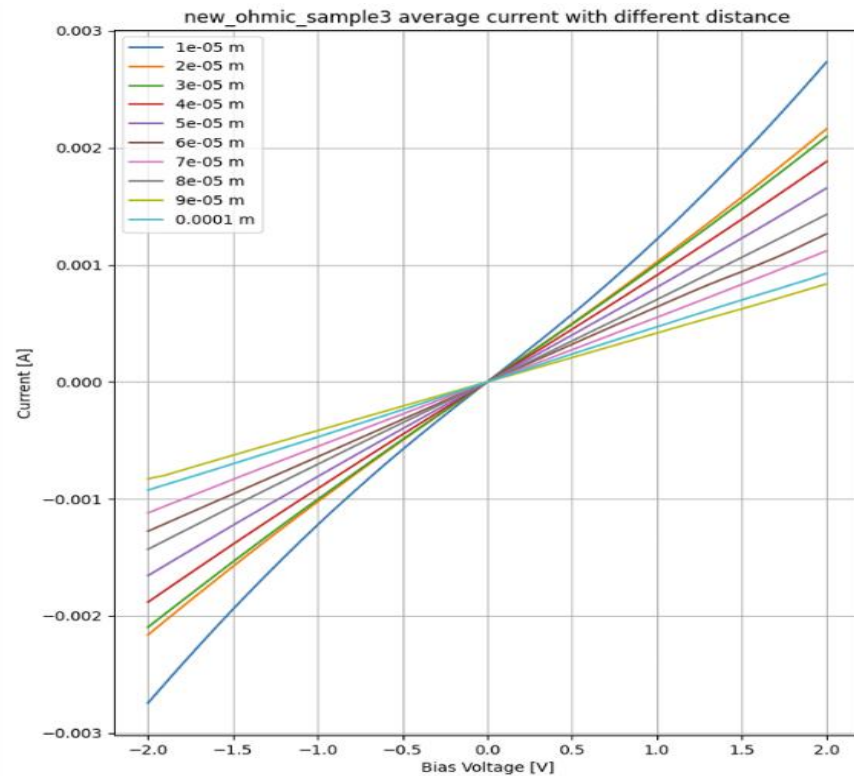
Aluminum Pad Deposition



Wet Etch Aluminum Pad

## ● Optimize the p-type ohmic contact

- Transfer Length Method (TLM)
- Optimal Process : Ni/Ti/Al Annealing (850° C, 5 min)
- Achieving  $\rho_c = 6.25 \times 10^{-5} \Omega \cdot \text{cm}^2$  contact resistivity

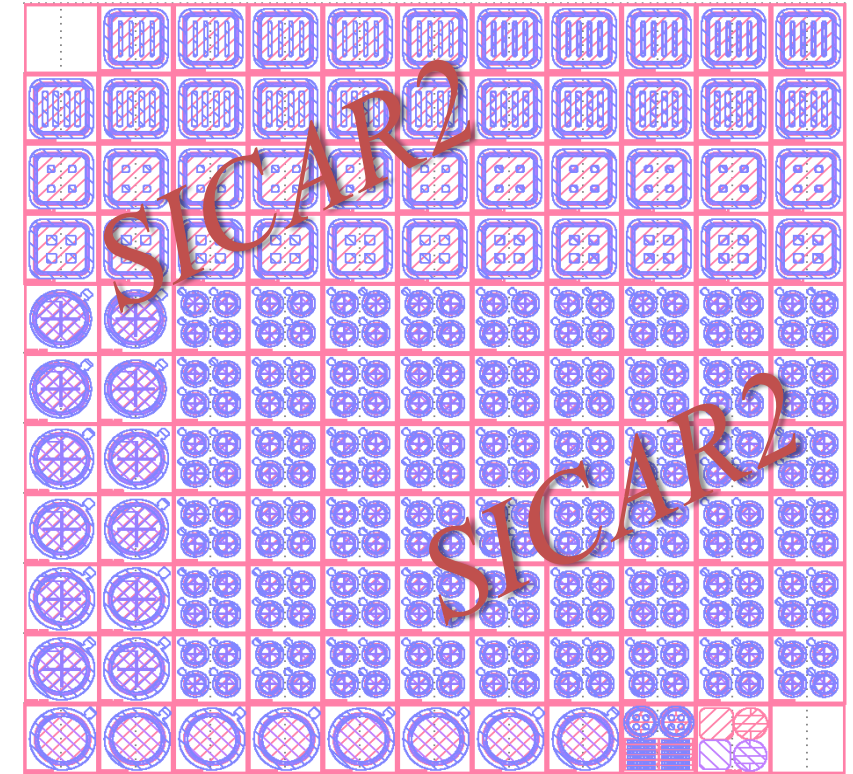


## ● Transitioning SICAR2\_LGAD to a 350nm MOSFET Process Platform

- Replacing Contact with Stepper Lithography
  - ✓ Higher resolution, essential for defining finer features
  - ✓ Offers better overlay accuracy, crucial for multi-layer devices
  - ✓ Reduces defect density by eliminating contact with the mask
- Single Reticle Field: 2cm × 2cm
  - ✓ Die per Reticle Field: 117
  - ✓ 20 dies: diode (1,750 μm diameter)
  - ✓ 54 dies: 216 diodes (740 μm diameter)
  - ✓ 43 dies: Pixel/strip AC-LGAD
  - ✓ 4 dies: test structure
- Wafer (6-inch) Capacity: 30 Reticles — 3510 dies

## ● Open for collaboration without an NDA

## ● Feedback on device design and process is welcome



- **Problems Discovered in the Etch Termination Structure**

- RIE-Induced Micro-trenching
- Consistent ~300 nm trench depth at termination interface
- Compromised breakdown voltage and long-term reliability

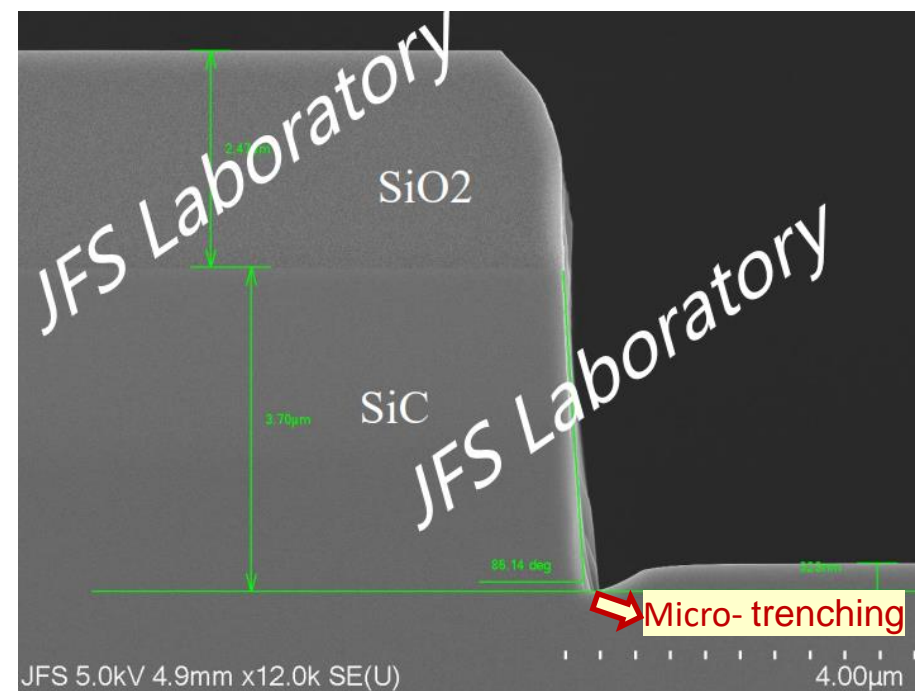
- **ICP Etch Process Evaluation**

- **Etch Termination: Unsuitable for Large-Area Devices**

- Significantly Higher Risk of Defects
- Major Challenges in Etch & Deposition Uniformity

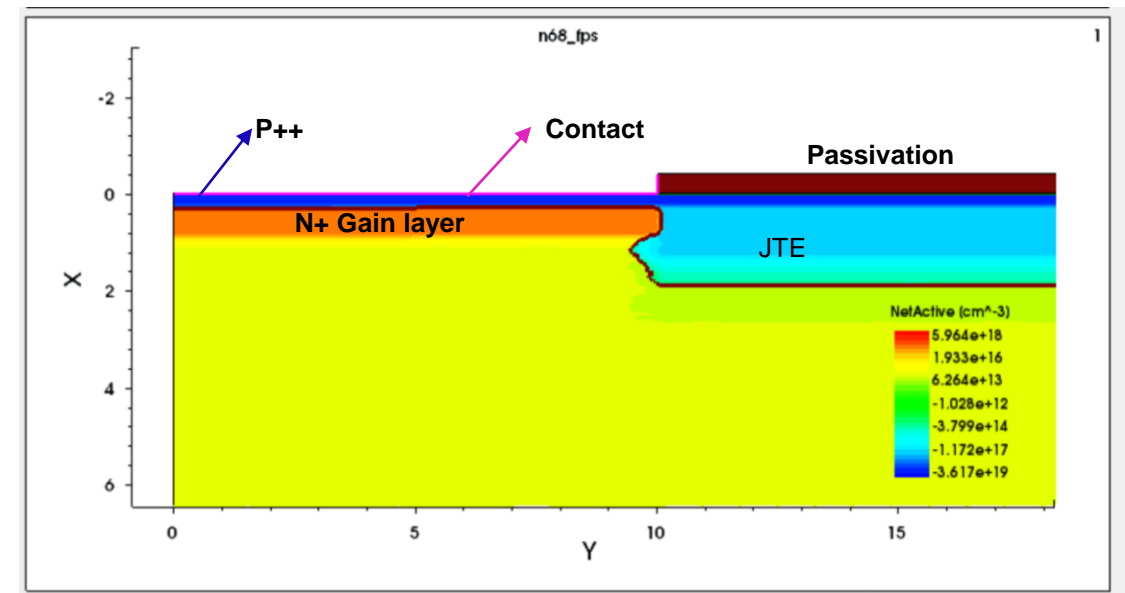
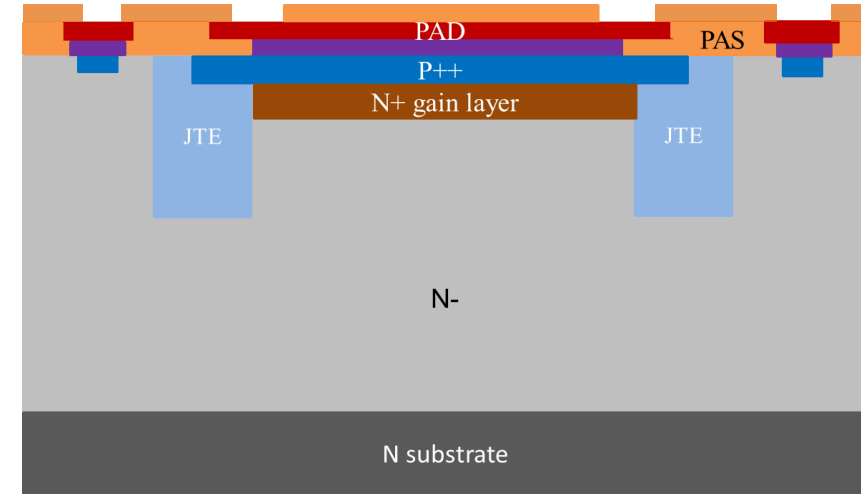
- **Ion Implantation Terminal**

- High-Temperature Ion Implantation & Annealing
  - ✓ JTE termination
  - ✓ Guard ring



## ● Prototype of SICAR3\_LGAD

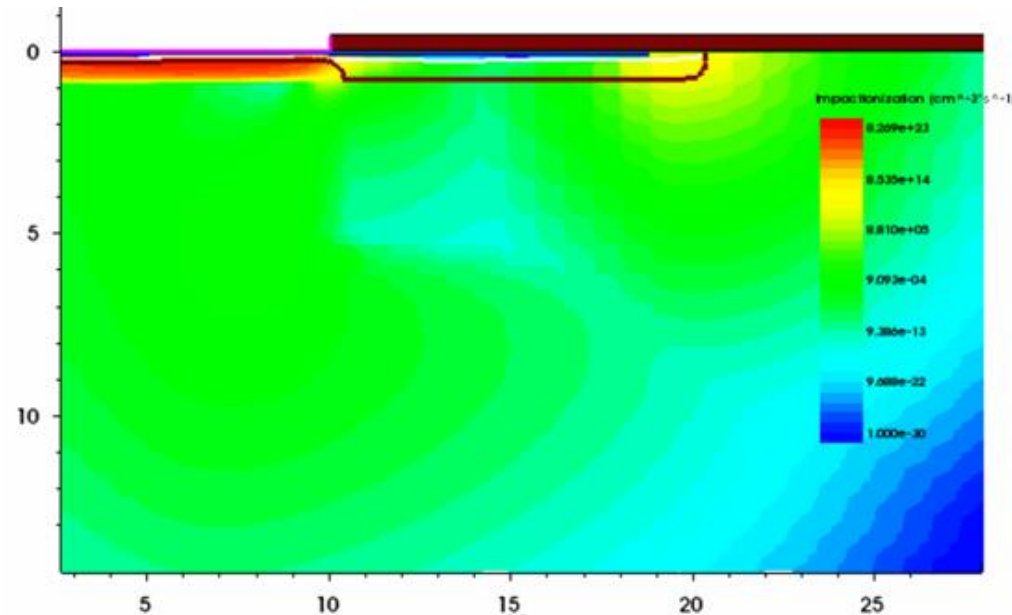
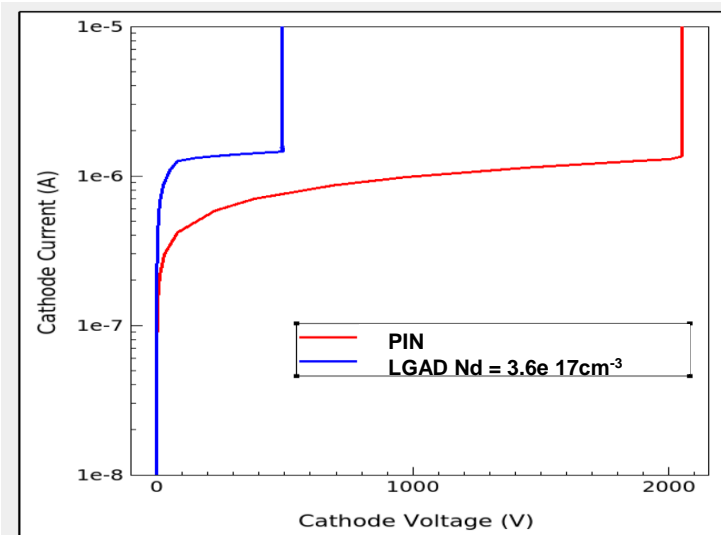
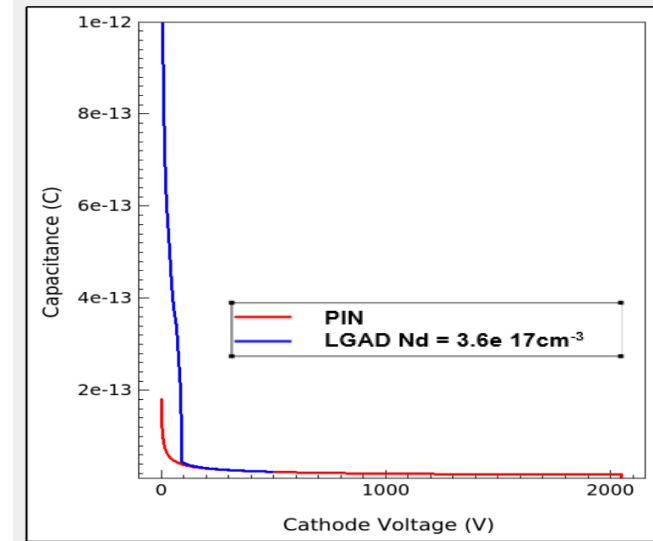
- N+ gain layer
  - ✓ Nitrogen implantation:  $N_d \sim 3.6e17 \text{ cm}^{-3}$
  - ✓ Implantation depth: 0.2-0.7  $\mu\text{m}$
- JTE termination
  - ✓ Aluminum implantation:  $N_a \sim 2.5e17 \text{ cm}^{-3}$
  - ✓ Implantation depth: 1.2  $\mu\text{m}$
- P++ Layer
  - ✓ Aluminum implantation:  $N_a \sim 1e19 \text{ cm}^{-3}$
  - ✓ Implantation depth: 0.2  $\mu\text{m}$



- **Simulation of CV and IV Characteristics**

- Depletion voltage of the gain layer  $\sim 100V$
- Breakdown voltage  $\sim 550V$
- Gain factor  $\sim 10$  @  $300V$
- The breakdown primarily occurs at the interface between the gain layer and the JTE

- Further optimize the terminal design



- **SICAR 1.2 PIN:**

- Low yield due to photoresist residue
- Promising X-ray radiation hardness
- Next Step: Beta-particle validation required

- **SICAR 2 LGAD:**

- Adjusting the epitaxial layer parameters to optimize the gain factor and consistency
- Optimizing the process work flow

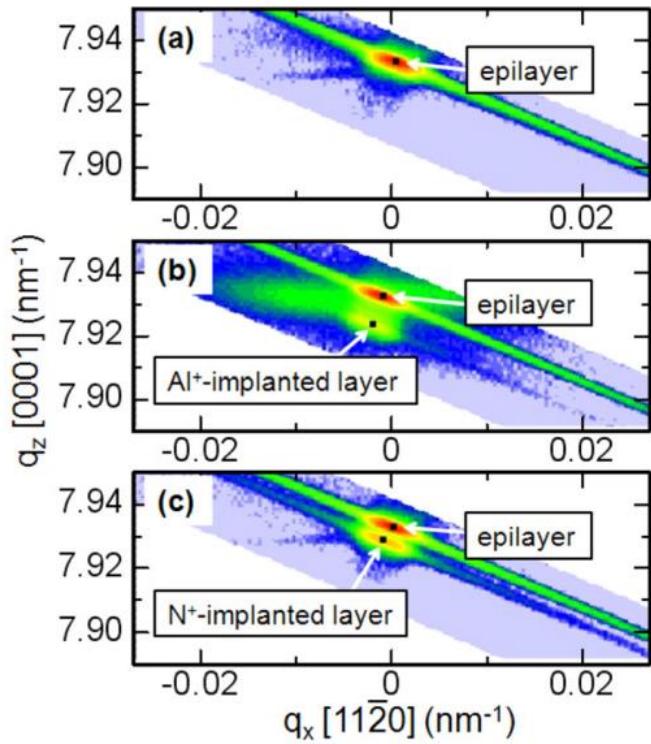
- **SICAR 3 LGAD:**

- Design phase; ion implantation simulation
- Optimizing the termination

Thanks for your attention!

Higher Implantation increases lattice mismatch and defects !

## Reciprocal space mapping



- N-type epitaxial layer
  - The epitaxial peak overlap with substrate
- After Al<sup>+</sup> implanted
  - P<sup>+</sup> peak deviates from the substrate peak
  - lattice mismatch
- After N<sup>+</sup> implanted
  - N<sup>+</sup> peak deviates from the substrate peak
  - lattice mismatch

