

Update on SICAR

Thursday, 13 November 2025 14:40 (20 minutes)

This talk outlines the fabrication progress of the second-generation 4H-SiC Low-Gain Avalanche Diode (SICAR2), designed for a nominal gain of 10–15. Fabricated using 350nm stepper lithography and substrate thinning for improved timing resolution, the 2mm × 2mm die includes devices with 1.4mm and 0.55mm active areas, along with AC-pixelated (2×2) and AC-strip (4-strip) test structures. All devices feature an etched termination with field plate to reduce leakage current, though this limits the active area. SICAR2 establishes a critical foundation for next-generation SiC LGAD development —SICAR3 which will introduce a high-temperature ion-implanted Junction Termination Extension (JTE) to enable larger active areas with low leakage.

Type of presentation (in-person/online)

in-person presentation

Type of presentation (I. scientific results or II. project proposal)

I. Presentation on scientific results

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