SiC LGAD Edge Termination via Controlled Ion-Implantation Damage

B. J. Sekely[1], T. Yang[2], Y. Satapathy[1], G. Allion[1], G. Atar[1], P. Barletta[1], C. Haber[2], S. E. Holland[2], S. Stucci[3], A. Tishelman-Charny[3], S. Pavlidis[1], J. F. Muth[1]

[1] North Carolina State University

[2] Lawrence Berkeley National Laboratory

[3] Brookhaven National Laboratory

NNF
NCSU NANOFABRICATION FACILITY

4th DRD3 week on Solid State Detectors R&D

Acknowledgement: DOE Grant #DE-SC0024252

PM: Helmut Marsiske

BERKELEY LAB
LAWRENCE BERKELEY NATIONAL LABORATORY

Brookhaven National Laboratory

NC STATE UNIVERSITY Electrical and Computer Engineering

Silicon vs 4H-SiC

- 4H-SiC has material advantages over silicon for an improved timing response and a higher operating temperature for particle detection

Parameter	Silicon	4H-SiC	Result
Bandgap [eV]	1.1	3.34	Lower leakage currents; higher temperature operation
Threshold Displacement Energy [eV]	12 – 20	22 – 35	Higher theoretical radiation resistance
Thermal Conductivity [W/m*K]	130	370	Easier to cool associated readout electronics
Impact Ionization Coefficient	$\alpha_e > \alpha_h$	$\alpha_e < \alpha_h$	Inverted doping polarity of LGAD
Drift Carrier Mobility [$cm^2/V*s$]	$\mu_p = 460$	$\mu_n = 800 – 1000$	Better time resolution
Breakdown Field [MV/cm]	0.3	3	Higher bias voltage to support gain mechanism
e-h pairs generated per micron of MIP traveled	80	57	Lower initial signal from MIPs

Design & Fabrication of 4H-SiC LGAD by LBNL and NCSU

- Design based on 6-inch 4H-SiC wafers with custom epitaxial stacks
  - 0.5 µm gain layer with doping concentration from 2e17 to 5e17 cm^{-3}, which results in an electric field between 2 and 5 MV/cm

Sekely, B.J., et. al. Fabrication of 4H-SiC Low Gain Avalanche Detectors (LGADs). 10.4028/p-0t5ifB

Yang, T., et. al, Characterization of 4H-SiC Low Gain Avalanche Detectors (LGADs). 10.1016/j.nima.2025.170873

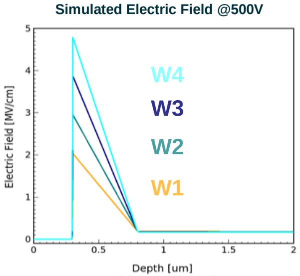
Custom Epitaxial Wafers

W1

P++ 0.3um 1e20
N+ 0.5um 2e17
N- 75um ~2e14
(doping level as low as possible)
N-buffer 2um 1e18
N++ Substrate

W2

P++ 0.3um 1e20
N+ 0.5um 3e17
N- 75um ~2e14
(doping level as low as possible)
N-buffer 2um 1e18
N++ Substrate


Simulated Electric Field @500V

W3

P++ 0.3um 1e20
N+ 0.5um 4e17
N- 75um ~2e14
(doping level as low as possible)
N-buffer 2um 1e18
N++ Substrate

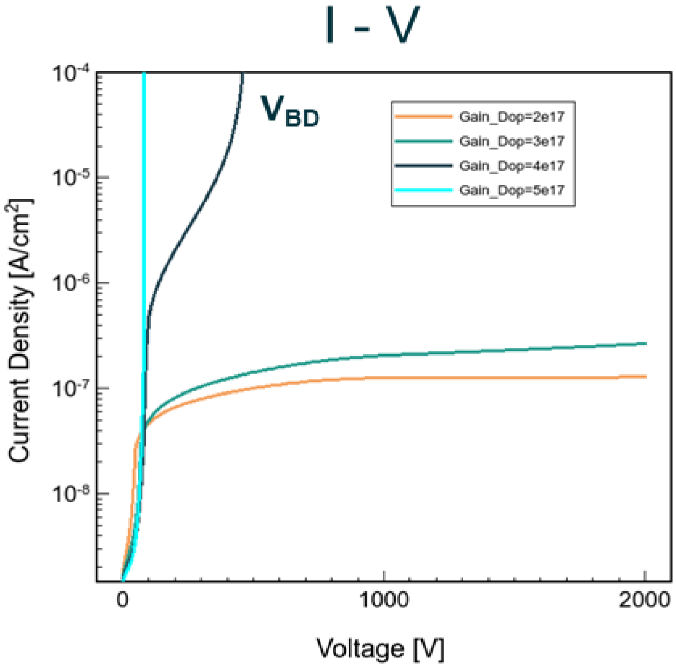
W4

P++ 0.3um 1e20
N+ 0.5um 5e17
N- 75um ~2e14
(doping level as low as possible)
N-buffer 2um 1e18
N++ Substrate

W5 (PIN)

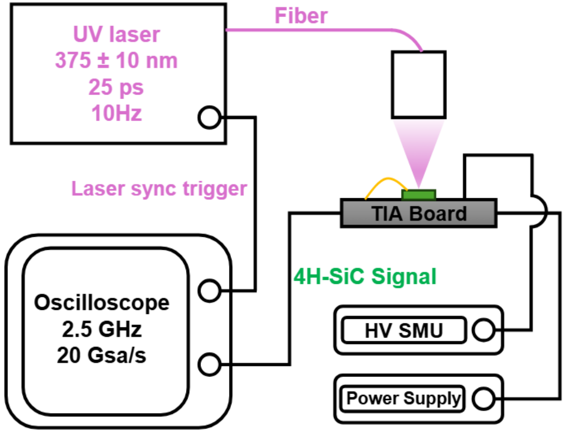
P++ 0.3um 1e20
N- 75um ~2e14
(doping level as low as possible)
N-buffer 2um 1e18
N++ Substrate

TCAD Simulation – Mesa Structures


I - V

4H-SiC LGAD Timing Resolution

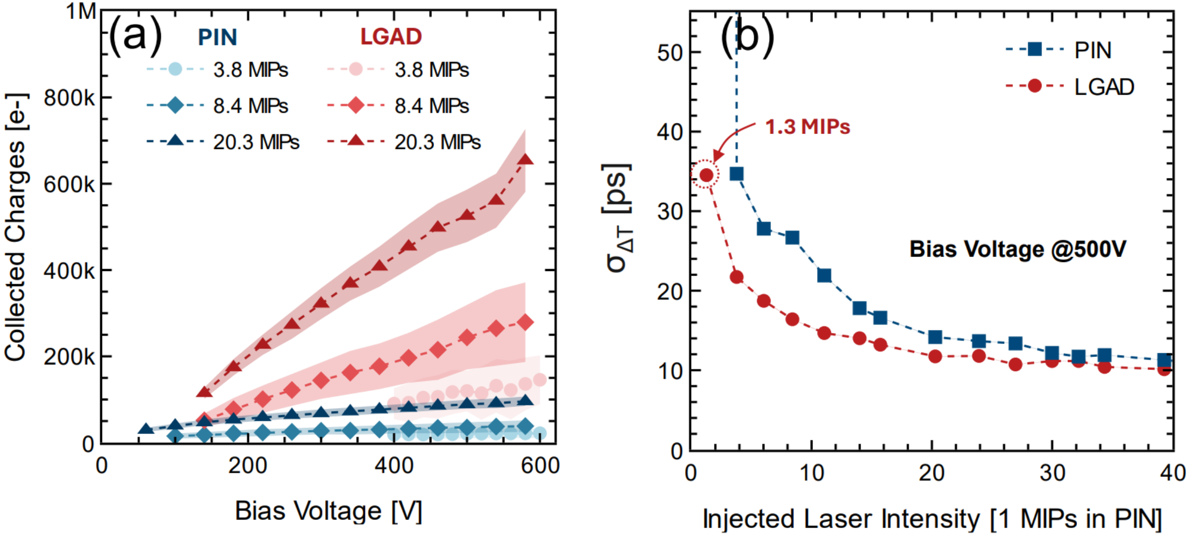
- Ultra-violet transient current technique (UV-TCT)
  - Laser-injected charge equivalent to number of MIPs
  - Current amplified in the LGAD via greater collected charge
- Room temp SiC LGAD timing resolution better than 35 ps with near single MIP equivalent detection – comparable with Si detectors!



UV-TCT Setup

W3 (4e17 cm^{-3})

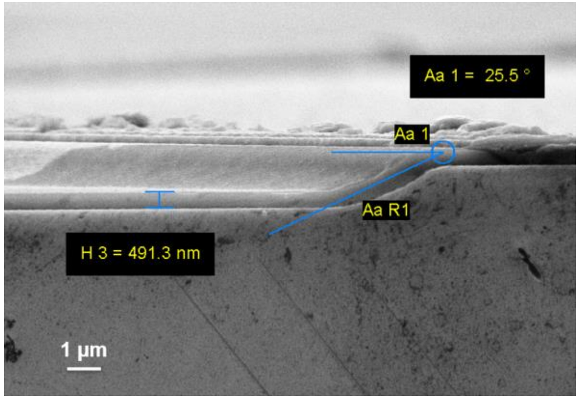
W3 (4e17 cm^{-3})



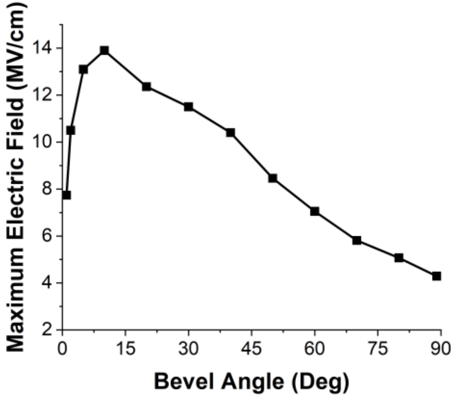
Tao Yang *et al.*, “Ultra-Fast 4H-SiC LGAD with Etched Termination and Field Plate”, *IEEE Electron Device Letters*, vol 46, no. 5, pp. 845-847, May 2025, doi: https://doi.org/10.1109/LED.2025.3548509.

A Source of Premature Breakdown

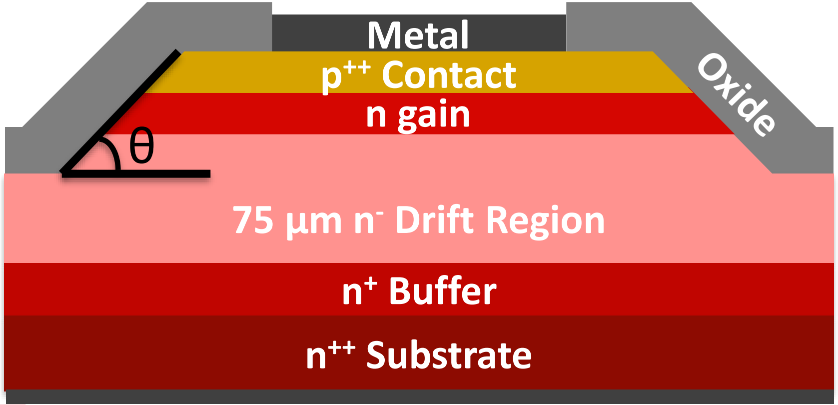
- Sloped mesa sidewall: "negative bevel"
  - Electric field crowding @ PN junction causing premature breakdown
- Vertical sidewalls reduce E-field crowding shown by Synopsys

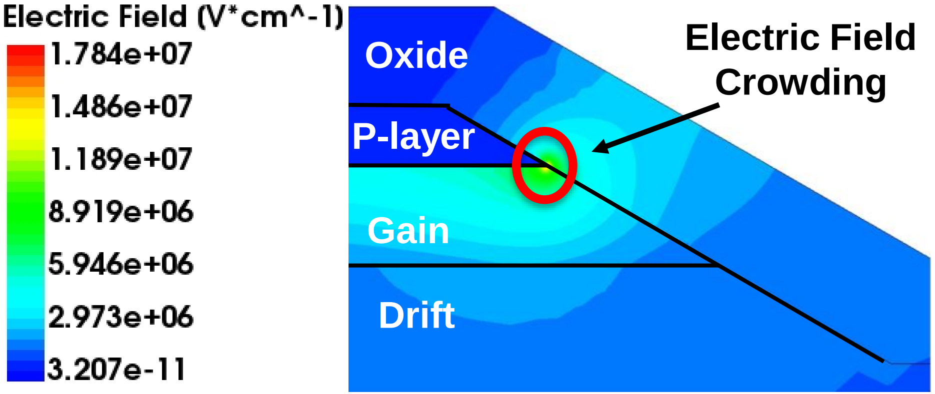


Synopsys TCAD



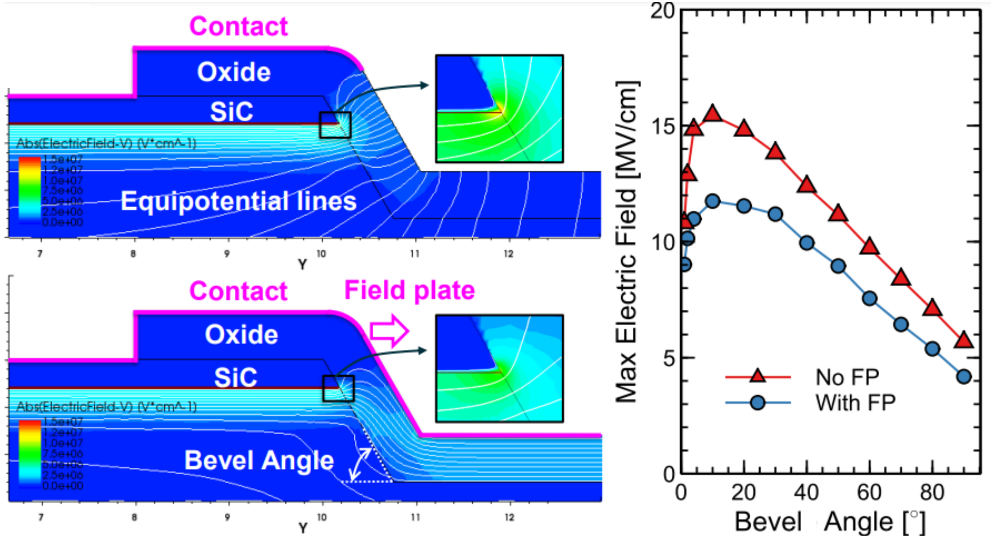
Mesa Device



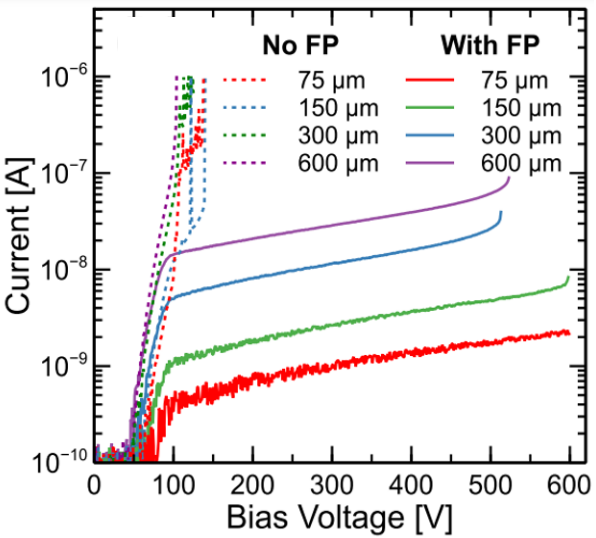


Electric Field Control – Field Plates (FPs)

Simulation



Experimental

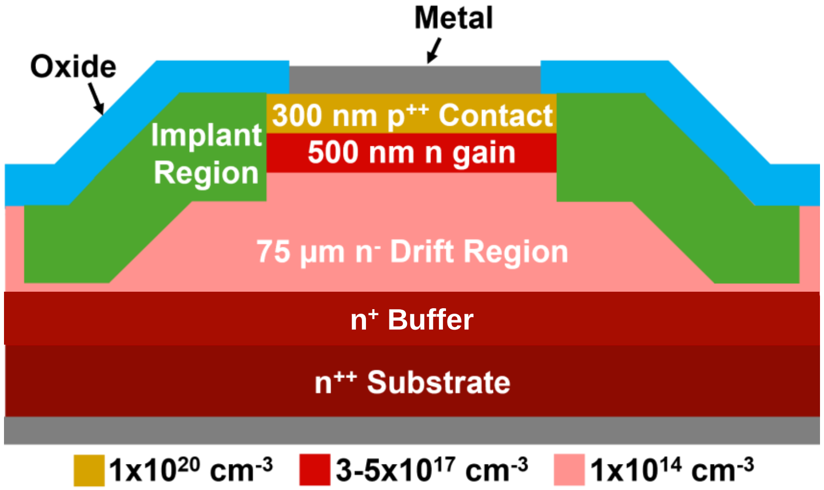


- E-field crowding due to negative bevel decreases V_{BD}
  - – Breaks down prior to full drift layer depletion
- FPs **<u>improves</u>** V_{BD} by spreading electric field in device but breaks down **<u>prior</u>** to full drift layer depletion

Tao Yang, Ben J. Sekely, Yashas Satapathy, Greg Allion, Gil Atar, Philip Barletta, Carl Haber, Steve Holland, John F. Muth, Spyridon Pavlidis, Stefania Stucci, Abraham Tishelman-Charny, “Ultra-Fast 4H-SiC LGAD with Etched Termination and Field Plate”, *IEEE Electron Device Letters* (accepted)

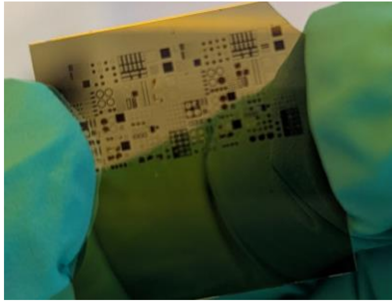
Ion Implantation Damage in 4H-SiC LGADs

- Si LGADs use ion implantation for JTEs
  - How to make JTE-like in 4H-SiC LGAD?
  - Implantation in SiC requires hard masking, high temperature (>1700 C) annealing, carbon capping
- Our innovative approach: **cold He ion implantation to create SiC defects**
  - No high-temp anneal – **<u>leave defects</u>**!
  - Defect compensation – control field by altering effective doping
  - Potential advantages of implantation:
    - Efficient termination enabling full depletion and high gain
    - Simple process/fab using std Si tools/processes

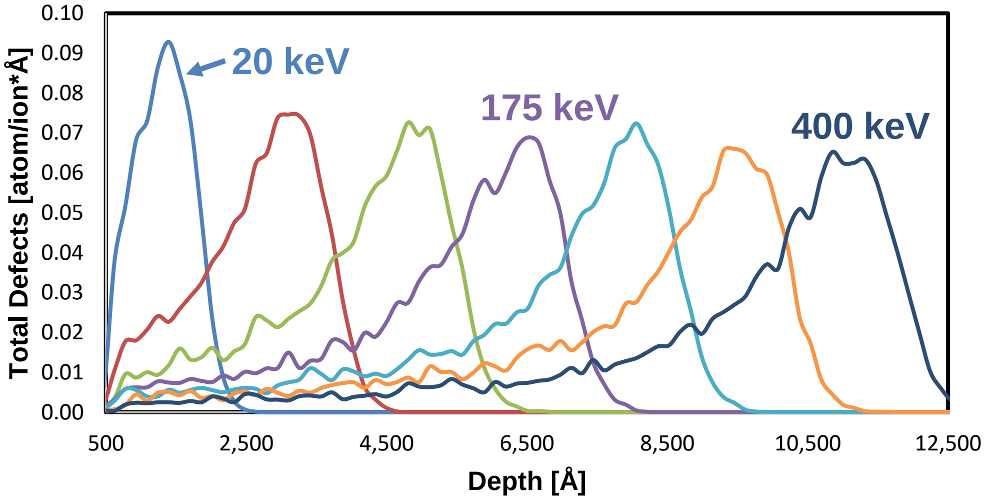


Modeling He Implantation Damage Profile

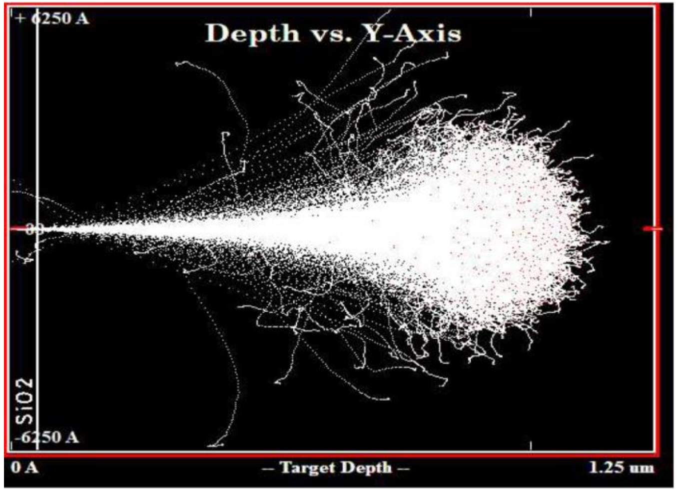
- Defect profile calculated using TRIM[1]
- Box profile for implantation – minimum diffusion in SiC
  - Requires multiple implant energies to form box profile
- Reference devices made without implantation on same chip



Total Damage - He Implantation



TRIM – He Implantation

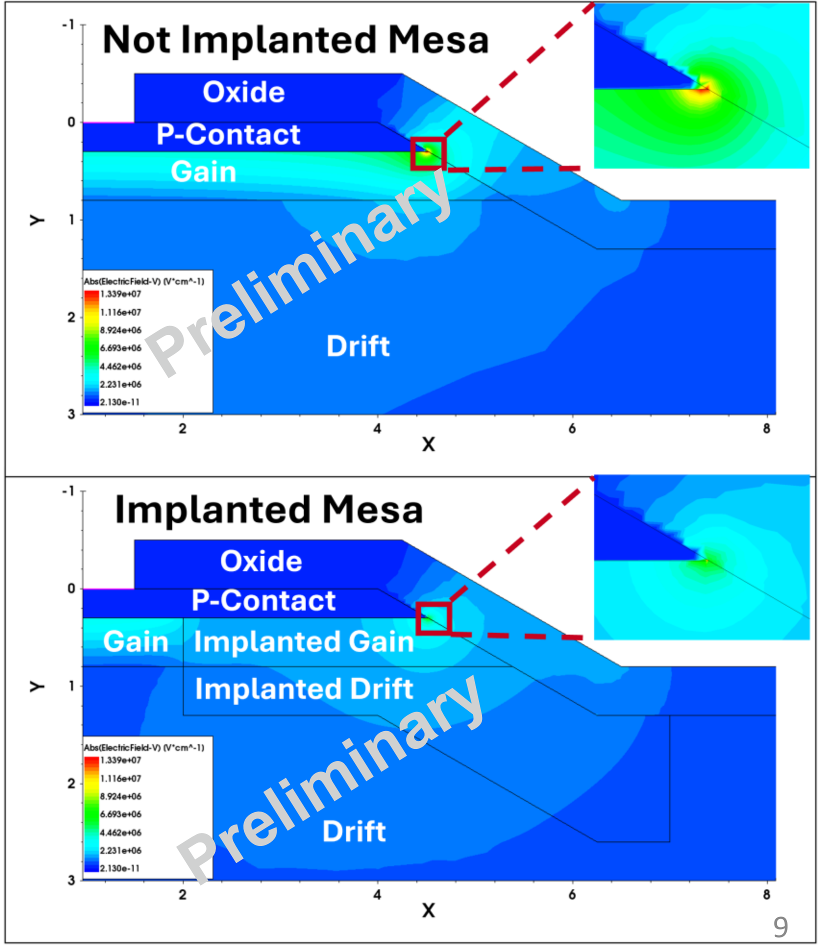


---

1. J. F. Ziegler, M. D. Ziegler, and J. P. Biersack, “SRIM – The Stopping Range of Ions in matter,” *Nucl. Instrum. Methods Phys. Res. Sect. B.*, vol. 268, pp. 1818 – 1823, 2010.

Ion Implantation – Defect Compensation Approach

- Implant below critical amorphization dose to prevent amorphization
  - Implant dose high enough to modulate doping through generated defects
  - Implant region: crystal defect states modeled as lower n-type doping
  - Primary defect: “acceptor-like”[1] carbon vacancy
    - Reduces effective doping in n-type implanted regions
  - p-contact highly conductive: “FP like”
  - Preliminary TCAD simulation here which assumes no crystal damage

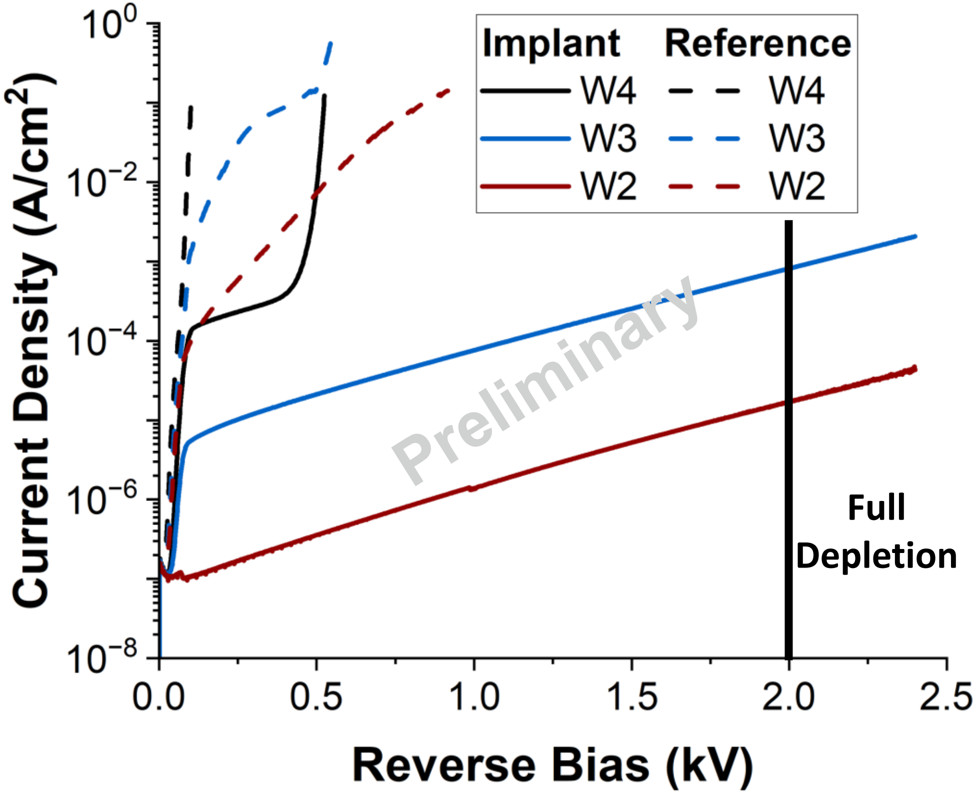


---

1. T. Kimoto, K. Kawahara, B. Zippelius, E. Saito, and J. Suda, “Control of carbon vacancy in SiC toward ultrahigh-voltage power devices,” *Superlattices and Microstructures*, vol. 99, pp. 151 – 157, 2016.

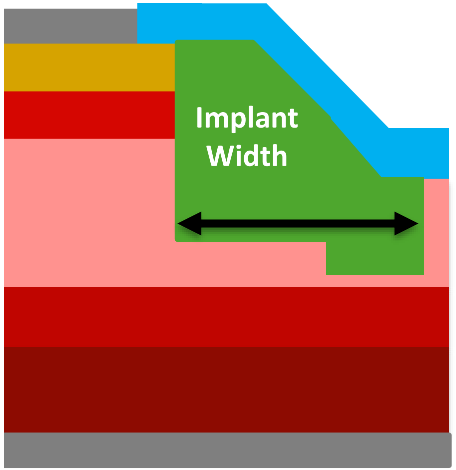
Preliminary I-V of Defect Compensated LGADs

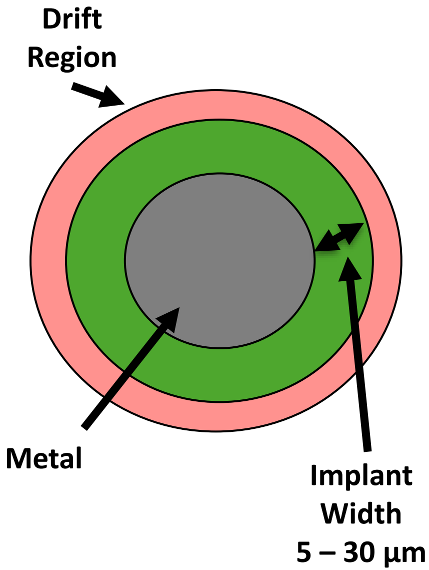
- Implanted mesa structures show improved breakdown voltages across all epistacks
  - Reference: unimplanted samples on same chip
  - Greater leakage in devices with higher gain
- Devices achieve full drift and gain layer depletion prior to breakdown

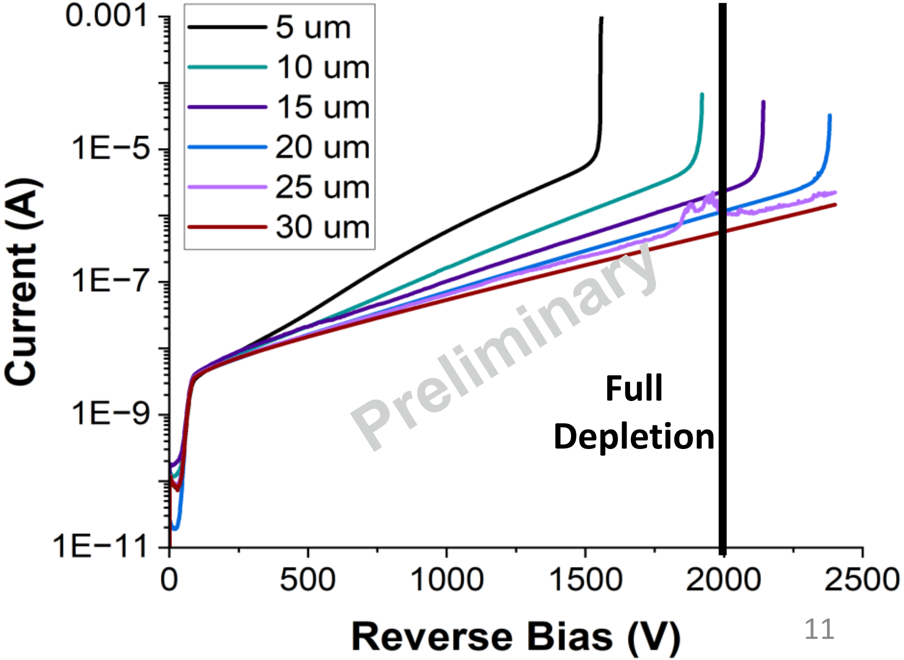


Ion Implant Width on I-V Characteristics

- Wider implants show greater breakdown voltage and decreased leakage current
  - Greater distance to “spread” electric field, reduces spatial resolution

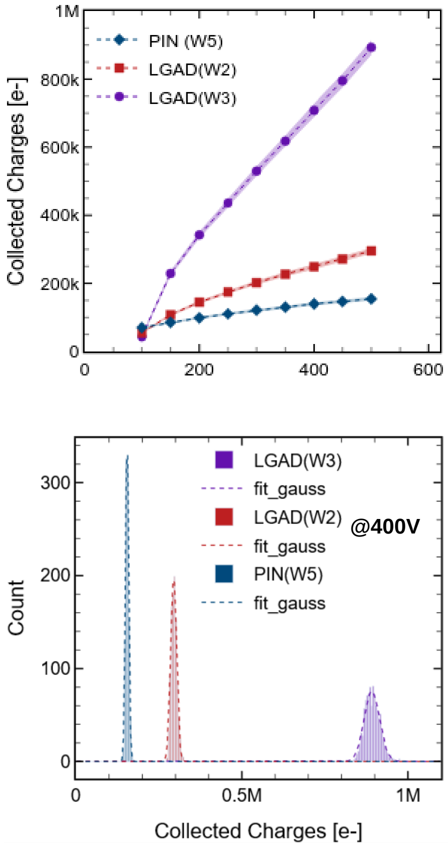

X-Section


Top-Down

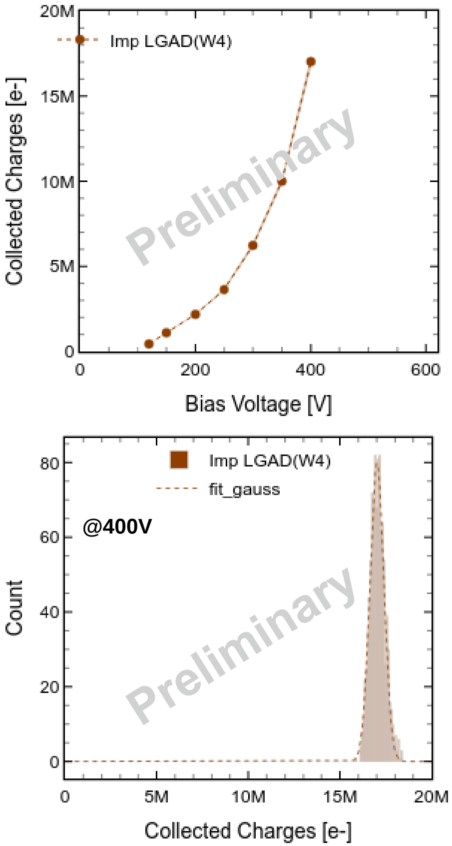

W3 (4e17 cm^{-3}) Mesa Structures

UV-TCT Test on Defect Compensated LGADs

PIN, LGAD(W2,W3) without implantation



LGAD(W4) with implantation



- Ion implantation achieves a larger breakdown voltage in the W4 LGAD
    - higher bias voltage operation during UV-TCT
- Preliminary results indicate a substantially increased gain in the W4 epi, attributed to the higher gain layer doping concentration
- Larger gain results in a broader charge collection distribution
    - The impact on the device’s timing performance is currently under evaluation

Summary

- Novel use of defect compensation via ion implantation to:
  - Efficient termination enabling full depletion and high gain by decreasing E-Field crowding
    - Intact p-contact layer acts as a built-in FP to spread E-field
  - Simple process/fab using standard Si tools/processes
  - Thicker implant widths reduce leakage and increase breakdown voltage
  - Greater reverse bias operation using UV-TCT to see high gain in W4 epi
- Issues remaining to be explored:
  - Sources of leakage currents
  - Characterization of trap states generated during implantation
  - Timing performance of defect compensated LGADs
  - Irradiation testing

Thank you for your attention

Supplemental Slides

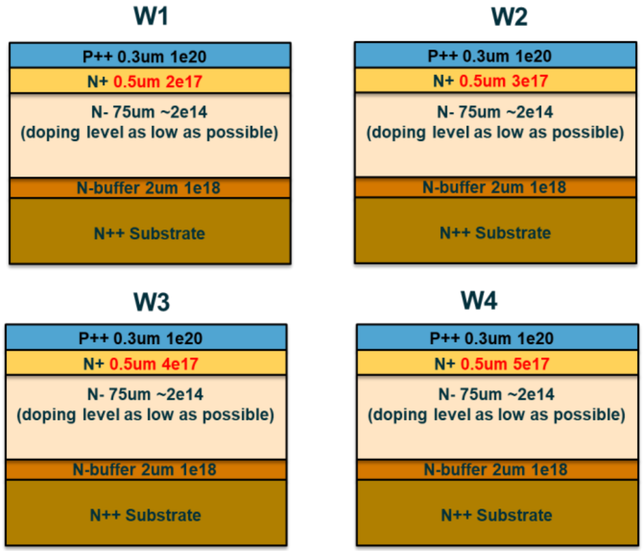
Design & Fabrication of 4H-SiC LGAD by LBNL and NCSU

- Design based on 6-inch 4H-SiC wafers with custom epitaxial stacks
  - 0.5 µm gain layer with doping concentration from 2e17 to 5e17 cm^{-3}, which results in an electric field between 2 and 5 MV/cm

Sekely, B.J., et. al. Fabrication of 4H-SiC Low Gain Avalanche Detectors (LGADs). 10.4028/p-0t5ifB

Yang, T., et. al, Characterization of 4H-SiC Low Gain Avalanche Detectors (LGADs). 10.1016/j.nima.2025.170873

Custom Epitaxial Wafers



W1

P++ 0.3um 1e20
N+ 0.5um 2e17
N- 75um ~2e14
(doping level as low as possible)
N-buffer 2um 1e18
N++ Substrate

W2

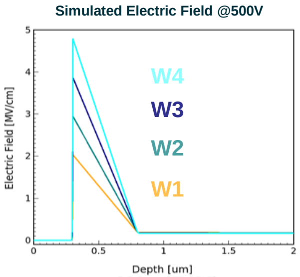
P++ 0.3um 1e20
N+ 0.5um 3e17
N- 75um ~2e14
(doping level as low as possible)
N-buffer 2um 1e18
N++ Substrate

W3

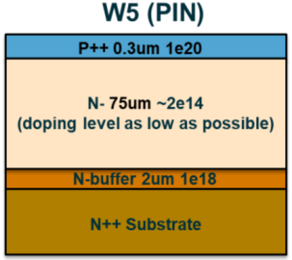
P++ 0.3um 1e20
N+ 0.5um 4e17
N- 75um ~2e14
(doping level as low as possible)
N-buffer 2um 1e18
N++ Substrate

W4

P++ 0.3um 1e20
N+ 0.5um 5e17
N- 75um ~2e14
(doping level as low as possible)
N-buffer 2um 1e18
N++ Substrate



Simulated Electric Field @500V



W5 (PIN)

P++ 0.3um 1e20
N- 75um ~2e14
(doping level as low as possible)
N-buffer 2um 1e18
N++ Substrate

TCAD Simulation – Mesa Structures