TPC DAQ developments

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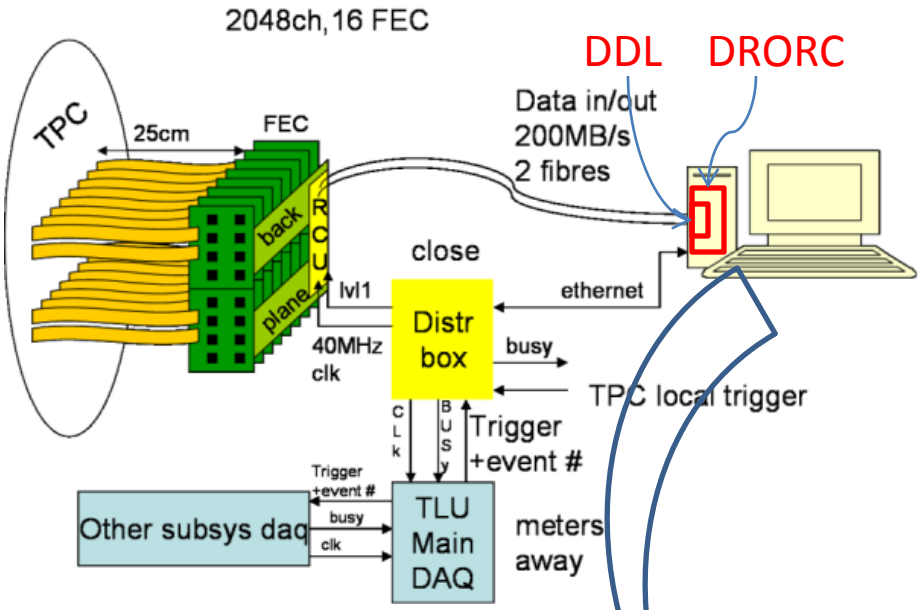
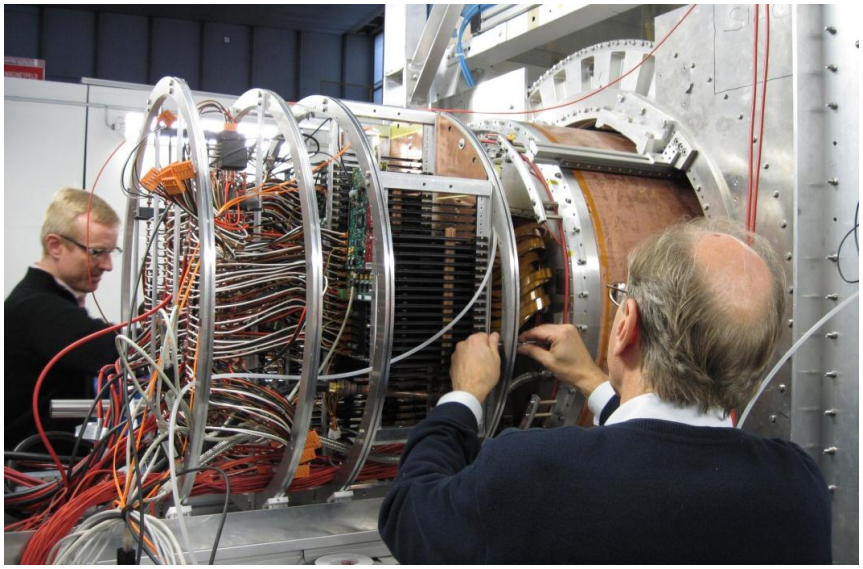
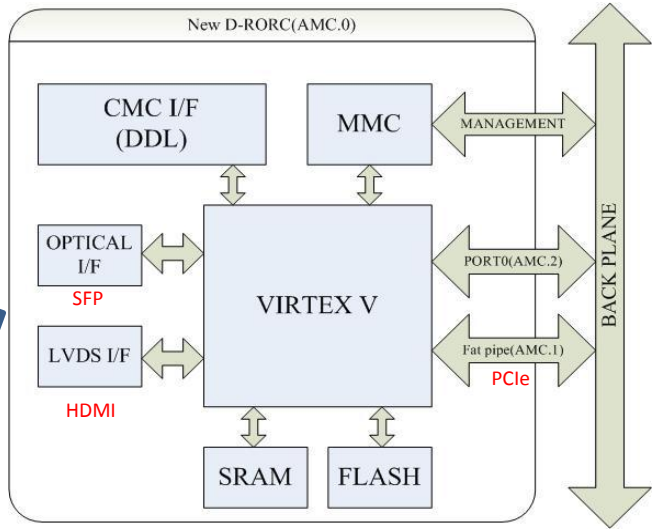
ILC TPC: New D-RORC design

Based on ALICE Hardware: FEC, RCU, DDL, DRORC (PCI)





From PC to µTCA

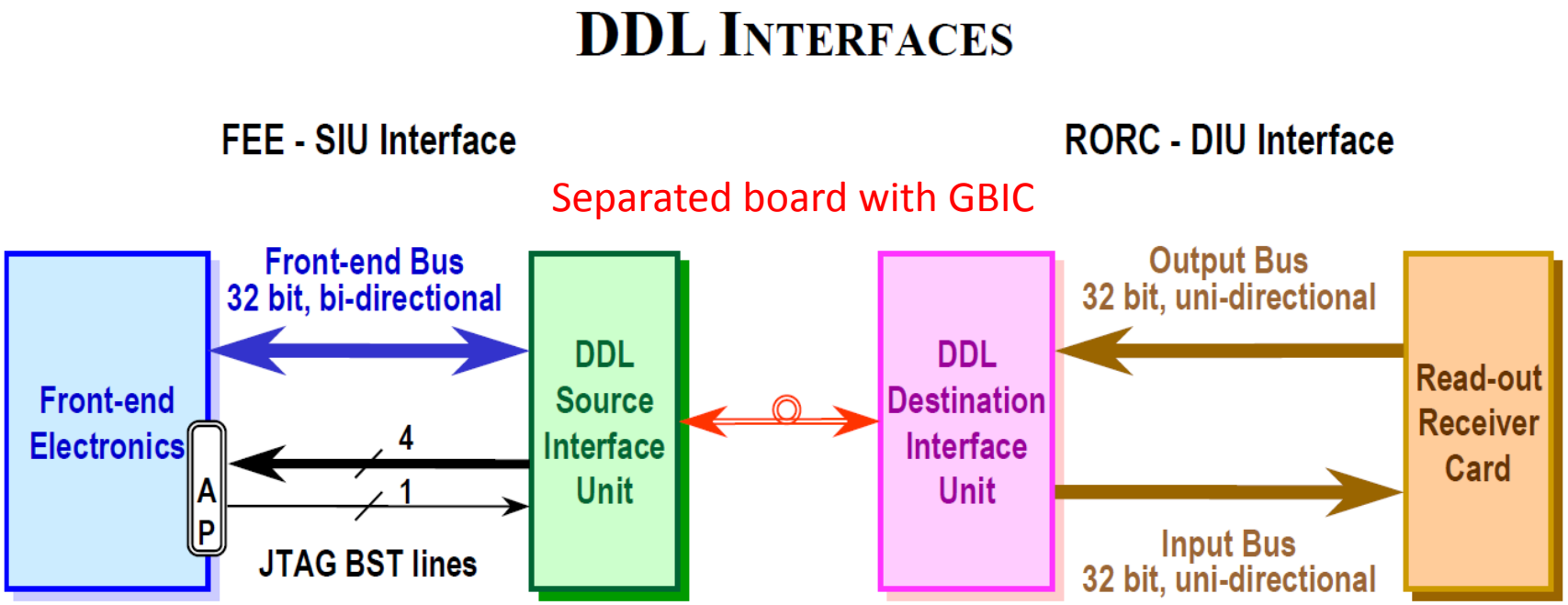


Collaboration with DESY, Lund

Specifications

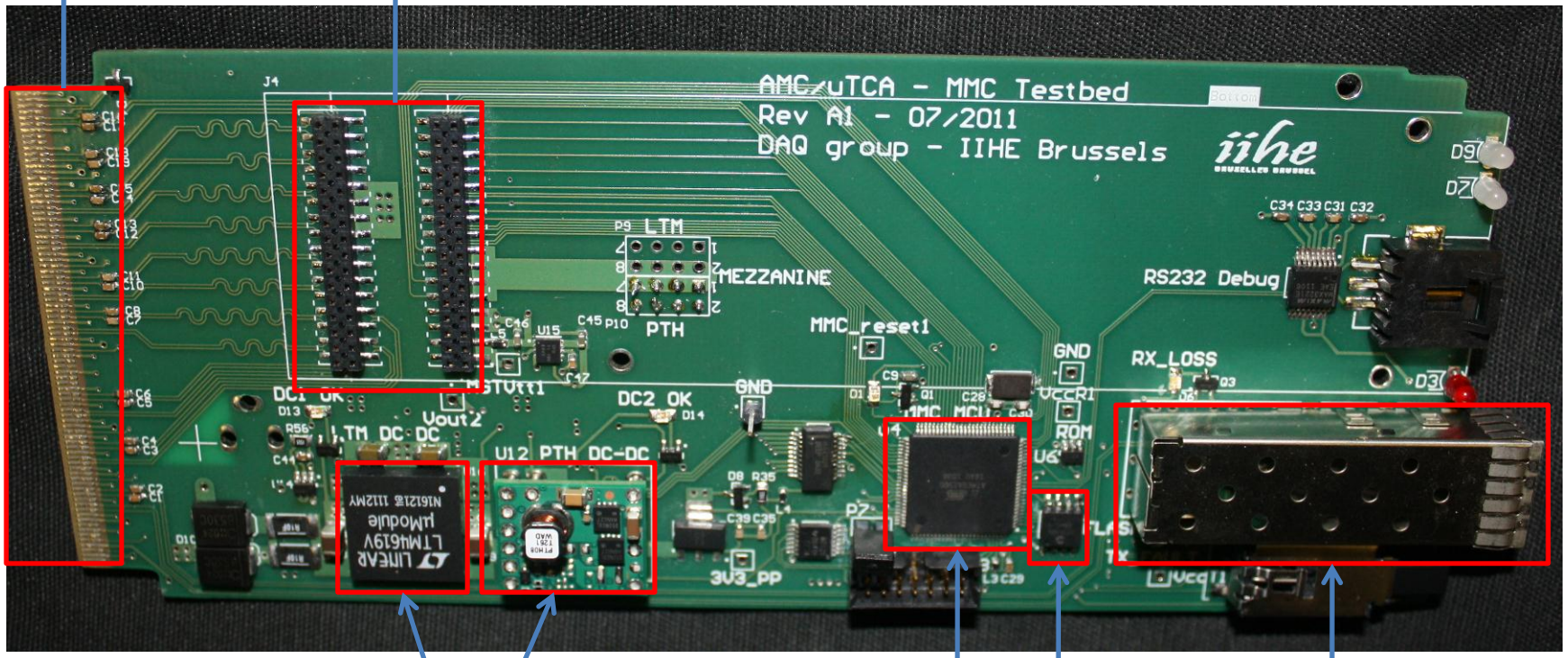
- From detector:
- DDL : 200MBps
- GBT : 400MBps
- To DAQ:
- PCI (64bit@100MHz) :800MBps
- PCIe (serial link) : 250 or 500 MBps/lane (up to 8 lanes)
- Plateform :
- PC
- MicroTCA (Micro Telecommunication Computing Architecture)

Interface

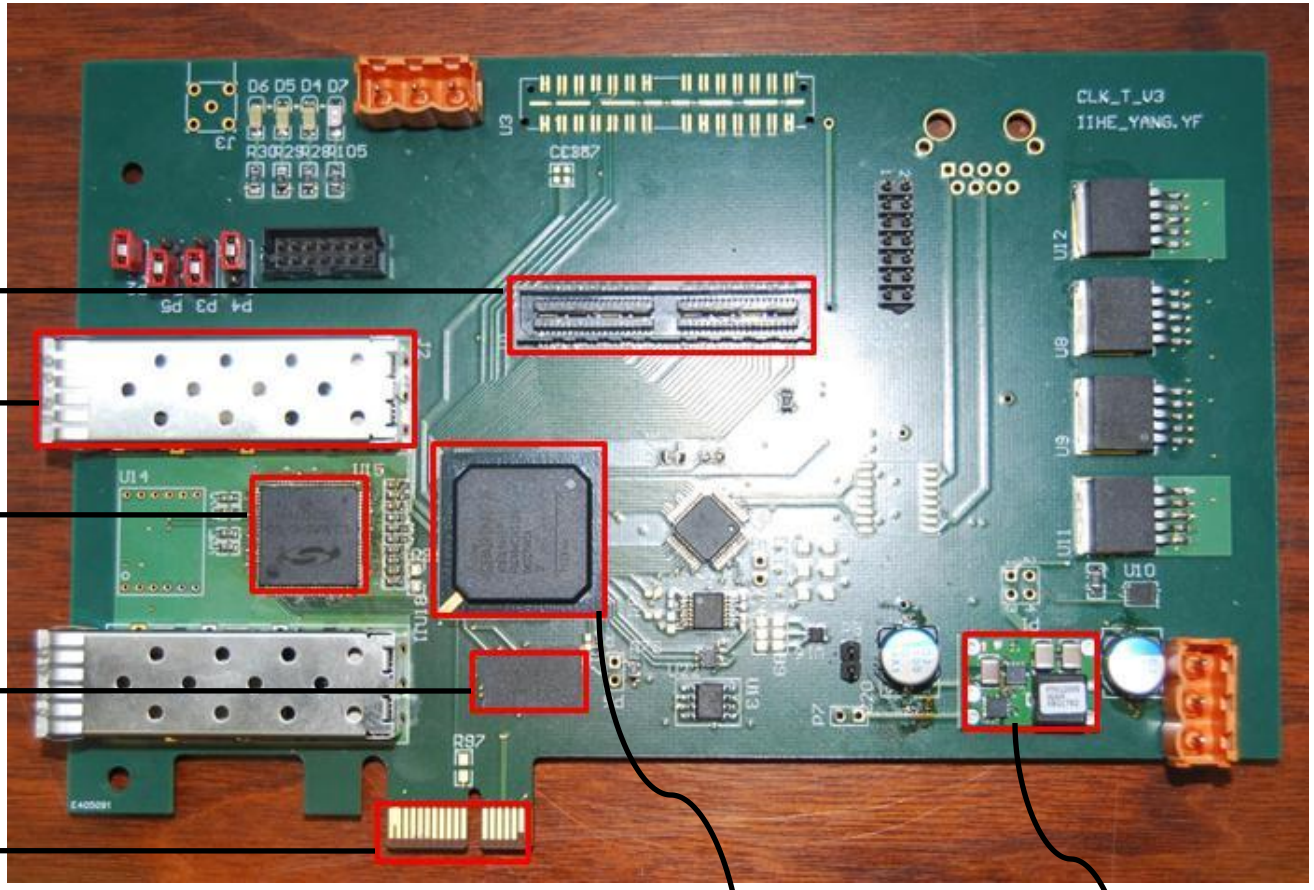


JTAG BST - *Joint Test Action Group Boundary-Scan Testing Architecture (IEEE Std 1149.1-1990)*
TAP - *Test Access Port*

MMC study

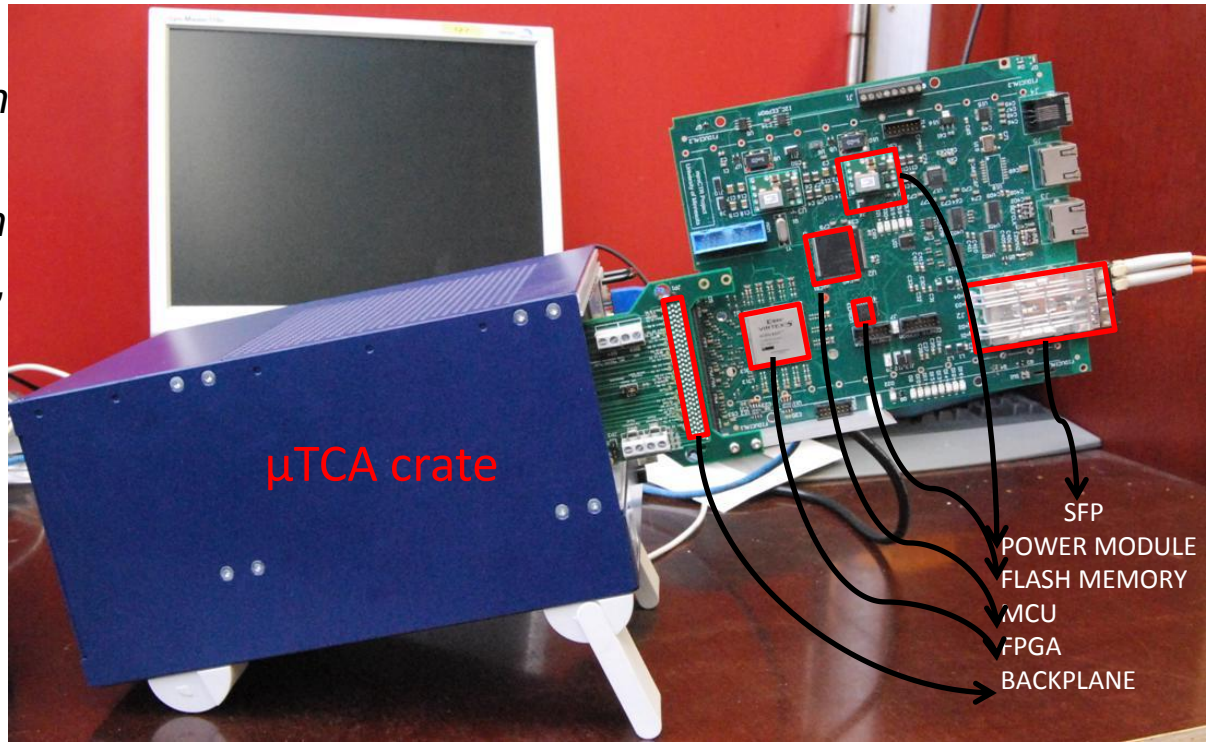

AMC connector
CMC connector
AMC/uTCA - MMC Testbed
Rev A1 - 07/2011
DAQ group - IIHE Brussels
iihe
LTM
MEZZANINE
PTH
MMC_reset1
RS232 Debug
RX_LOSS
GND
DC1 OK
DC2 OK
LTM DC-DC
U12 PTH DC-DC
3V3_PP
ROM
Power module
MCU
Sensor
SFP module

PCIe study


QSE connector
Optical module
Jitter cleaner
DDR2 memory
PCIe×1 connector
FPGA
Power module

Future plan

A large interconnection network with high bandwidth (10G ethernet , PCIe, etc)



Large processing power with some flexibility

Thank You!