AIDA Annual Meeting: WP3

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Valerio Re
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AIDA meeting
30.3.2012
DESY, Hamburg

- Objectives of WP3
- Definition of the program
- Agenda of first annual meeting
  - Status of milestones and deliverables
  - Progress report by established sub-projects
  - Discussion: projects not yet established and Groups not yet associated to a project
- Conclusions

WP3 Objectives

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Task 3.1: Coordination and communication

- To coordinate and schedule the execution of the WP tasks
- To monitor the work progress and inform the project management and the participants within the WP
- To follow-up the WP resource utilization
- To prepare the internal and Deliverable Reports

Task 3.2: 3D Interconnection

- Creation and coordination of a framework to make 3D interconnection technology available for HEP detectors
- Organisation of a network of contacts with industry to enable fabrication of sensors and electronics optimized for 3D interconnection
- Assess 3D vertical integration techniques enabling the HEP community to advance the state of the art of particle detectors

Task 3.3. Shareable IP Blocks for HEP

- Creation and coordination of a framework for the design of low and medium complexity microelectronics libraries and blocks in advanced submicron technologies to be made available to the community of users in HEP
- Organization of the design and qualification of a set of blocks using selected and qualified technologies
- Distribution and documentation of the library of functional blocks
- Organisation of regular Microelectronics Users Group meetings to exchange information, plan and coordinate actions related to the creation of a shared library of macro blocks.

Participants: CERN, CEA, CNRS, MPG-MPP, UBONN, INFN, AGH-UST, CISC, UB, UU, STFC
Associates: IPASCR, NTUA, UNIGLA, UNILIV, FOM

3D Interconnection

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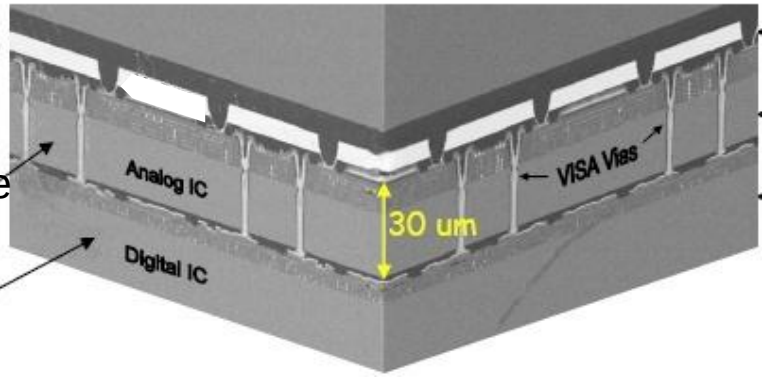
How to integrate good sensors and good electronic circuits?

3D Interconnection:

Si pixel sensor

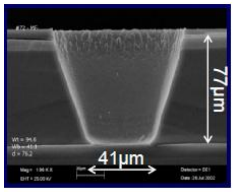
BiCMOS analogue

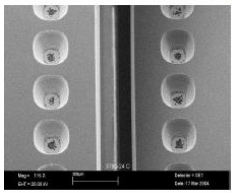
CMOS digital

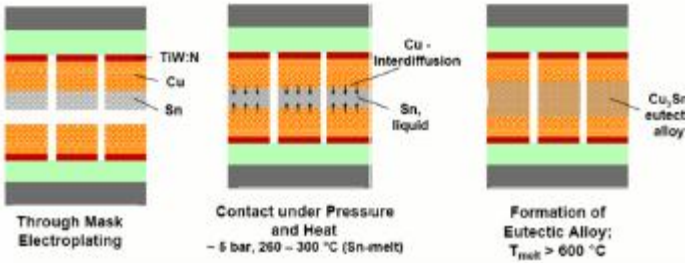


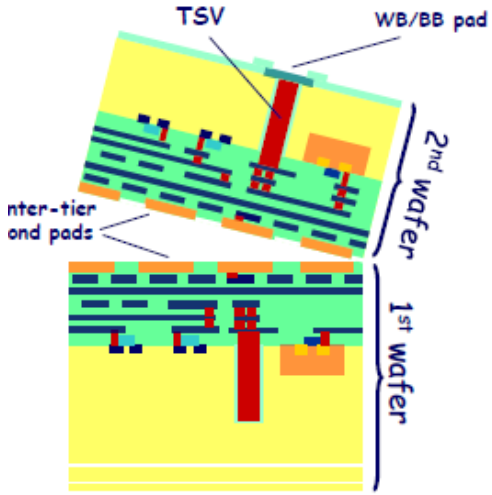
Two or more layers (="tiers") of thinned semiconductor devices interconnected to form a "monolithic" circuit.

Many ways to do it









Workshop with Industry

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Workshop with industry held in Bergamo, May 23.

- CEA-Leti (Mark Scannell)
- CMP (Kholdoun Torki)
- Fraunhofer EMFT (Armin Klumpp)
- Fraunhofer IZM (Thomas Fritsch)
- IMEC (Piet De Moor)
- T-Micro (Makoto Motoyoshi)
- VTT (Sami Vaehaenen)

In general technologies rated as 'mature' (by the company!) offer rather large TSV (small aspect ratio) and TSV/interconnection pitch (>50 μm). Few companies/institutes offer more advanced technologies with allowing smaller pitch, but they are still more on an R&D level.

WP3 strategy

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We agreed upon a “via last ” approach to 3D integration to build a 2-layer device **in heterogeneous technologies**, where the two layers are fabricated independently, and TSVs and interconnections are made as the last steps of the process. The “via last” approach could be applied to different device structures

A more c**onservative approach** can be based on “mature” technologies, with ~50 µm pitch for bonding and (peripheral) TSVs. This seems to be already commercially available, as confirmed by several R&D activities in our community

A more **aggressive approach** could go for real fine pitch and small TSV. This will target very future sensors (ILC, CLIC) and interconnections of individual pixels (like in 3D CMOS or SOI sensors). This has certainly higher profile and potential, higher costs and need of special ASICs.

We may agree to follow both approaches, closely monitoring the evolution and the availability of 3D technology in industry. Of course, this cannot be done with AIDA resources only; WP3 could support other R&D projects and contribute to the dissemination of results and know-how

We asked the participating institutes to propose projects

In a series of meetings we discussed and evaluated the proposals (including their funding)
One aspect was to merge similar proposals or ask participants to partner, in order to focus the resources

Approved Sub-Projects: WP3.2

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1) Bonn/CPPM:

Interconnection of the ATLAS FEI4 chips to sensors using bump bonding and TSVs from IZM (large diameter TSV, large interconnection pitch).

2) CERN:

Interconnection of MEDIPIX3 chips using the CEA-LETI process

3) INFN/IPHC-IRFU:

Interconnection of chips from Tezzaron/Chartered to edgeless sensors and/or CMOS sensors using an advanced interconnection process (T-MICRO or others)

4) LAL/LAPP/LPNHE/MPP:

Readout ASICs in 65nm technology interconnected using the CEA-LETI or EMFT process.

5) MPP/GLA/LAL/LIV/LPNHE:

Interconnection of ATLAS FEI4 chips to sensors using SLID interconnection and ICV (high density TSVs) from EMFT.

6) Barcelona

use a 2-tier approach to increase the fill factor of APD-sensors (based on Tezzaron/Chartered)

Bonn/CPPM

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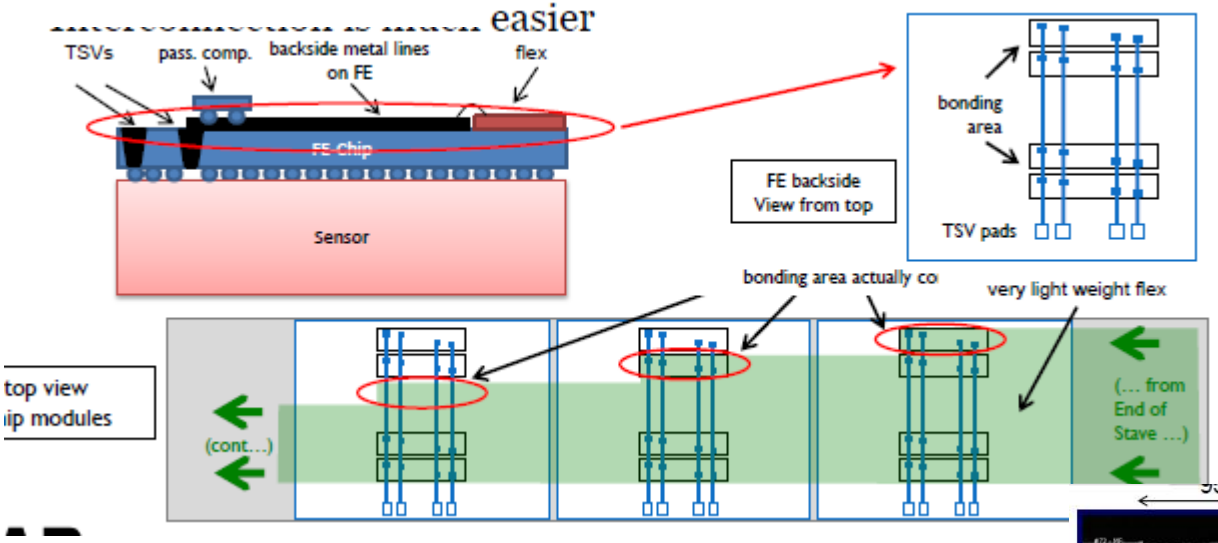
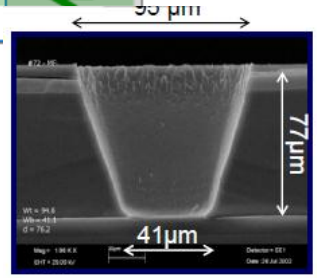
TSVs in ATLAS FEI4 chips and bump bonding to sensor

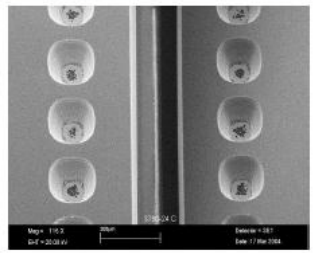


Large tapered vias by IZM. Successfully tested with FEI3



‘mature’ technology

FEI4 ASICs exists on wafers (3 reserved for project)



Run with IZM will start soon => results end of 2012
Run with LETI is planned
=> on schedule

CERN

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TSVs by LETI in Medipix3 ASIC

Phase I: TSV processing on Medipix3

Phase II; Hybridisation

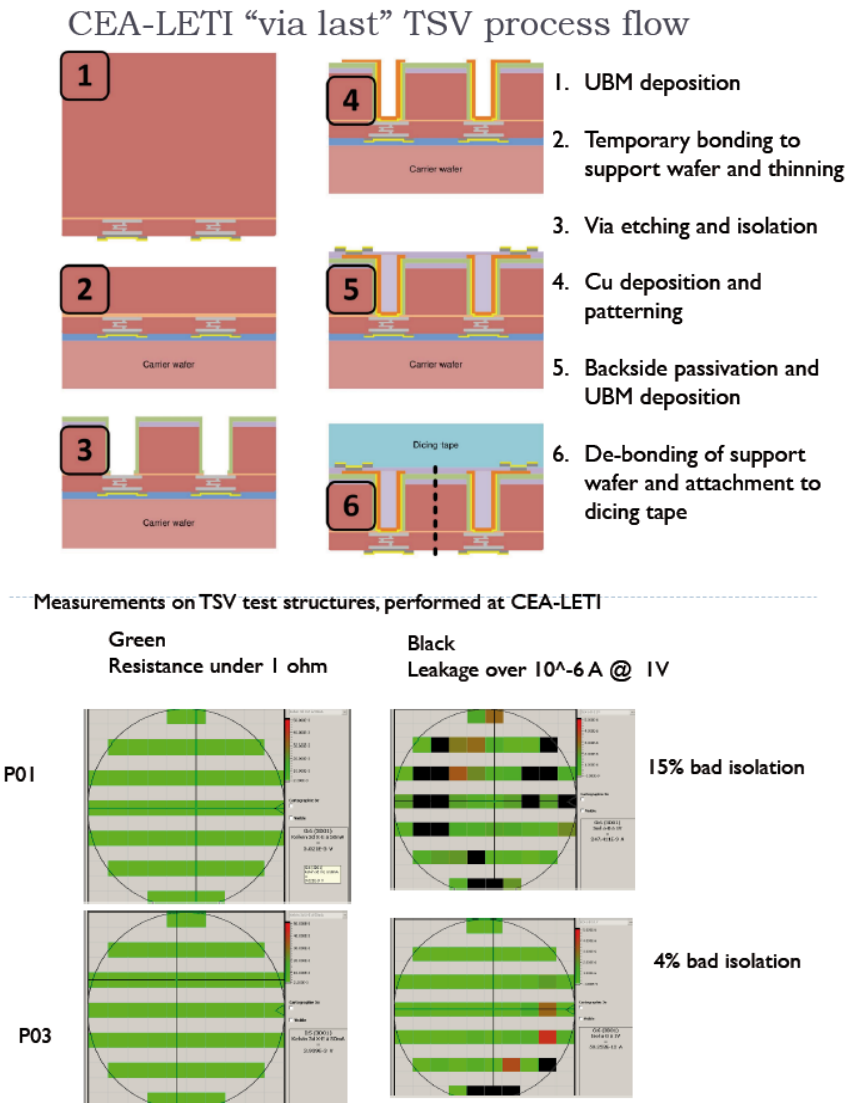
Phase III: Demonstrator Module

Rather large vias of 60µm diameter
1:2 aspect ratio

=> 'mature technology

Phase I done, good yield after some initial problems

Phase II started: bonding at VTT
(need for sensor wafers)



INFN/IPHC-IRFU

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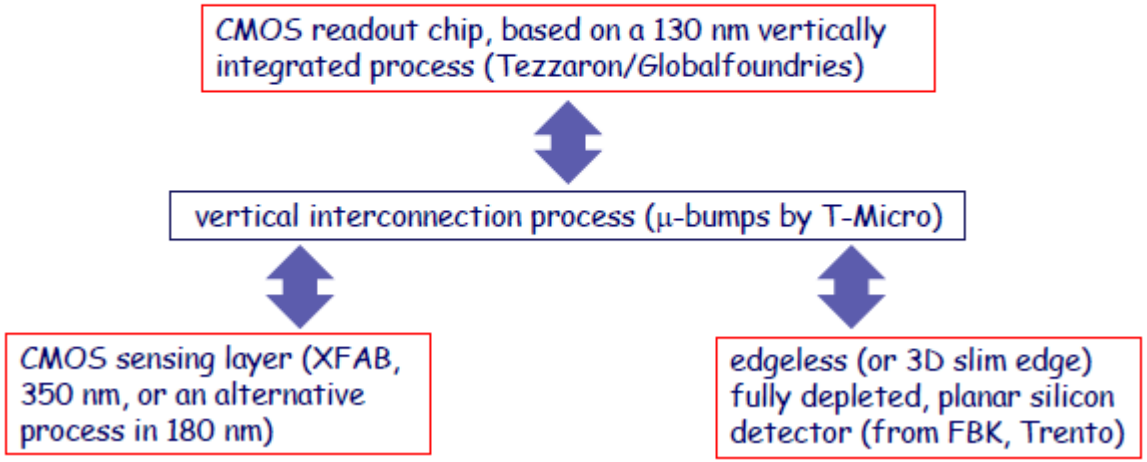
Design and fabrication of a multi-tier pixel sensor resulting from the vertical interconnection of a readout chip and of a sensing layer



Task	Delivery time
Edgeless sensor design (FBK)	Month 14
Edgeless sensor production (FBK)	Month 23
CMOS sensor design (IPHC-IRFU)	Month 26
CMOS sensor production (IPHC-IRFU)	Month 29
Readout chip design (INFN)	Month 17
Readout chip production (INFN)	Month 26
Readout chip-to-sensor vertical integration (T-Micro)	Month 41

Challenging project, ‘aggressive’ technology

Sensor order soon

On schedule

LAL/LAPP/LPNHE/MPP

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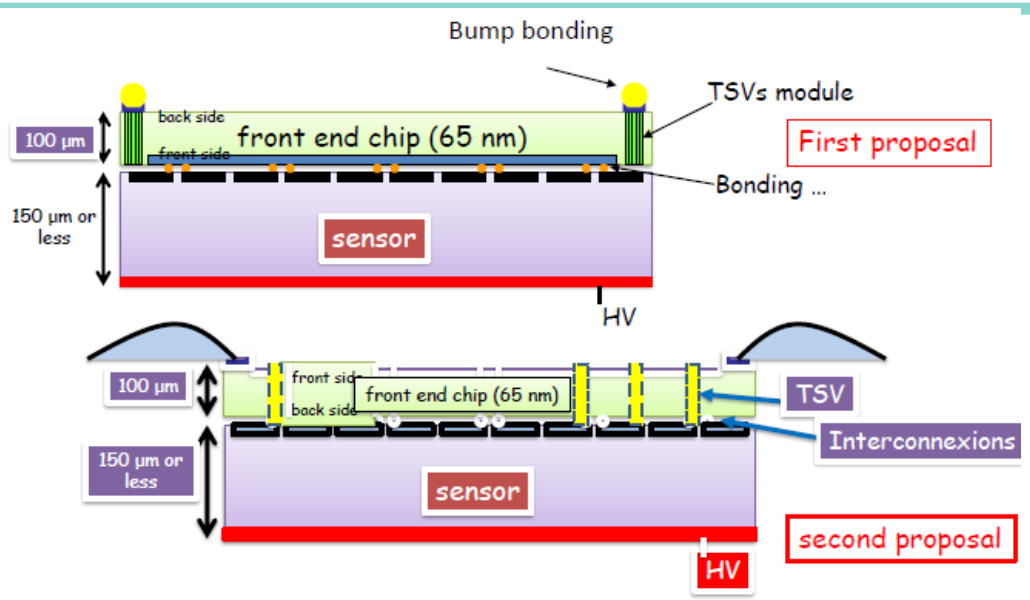
OMAEGAPIX2 pixel chip & sensor (35x200µm² pixels)

130nm Tezzaron version submitted in 2012

65nm planned (perhaps via AIDA WP3.3



A-operation: is to get slim edge Pixel sensors (IZM) with Omegapix2 chip- 05/2012

B-operation is to get edgeless pixel sensors (VTT) with Omegapix2 chip- 05/ 2012

Third step is to have an Omegapix ASIC readout 130nm (end 2013)and later-on 65nm

Deliver a 4 side abuttable monolithic edgeless device where I/O signals are routed vertically through the readout chip (~2015)

MPP/GLA/LAL/LIV/LPNHE

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Demonstrator module for SLID and TSV technologies based on ATLAS FE-I4

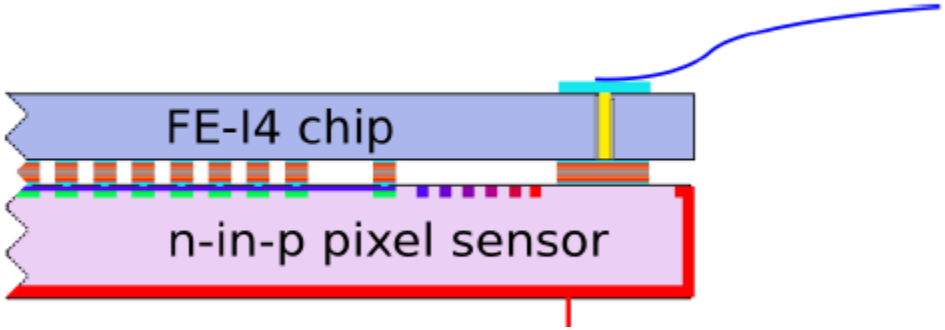
chip and n-in-p pixel sensors with a thickness of (150-200) *mm:*

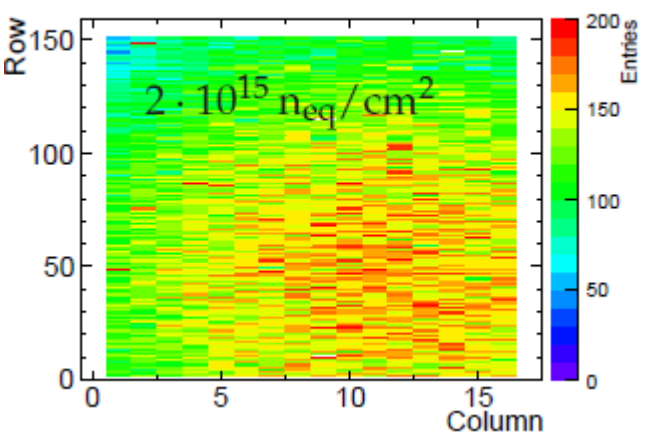
SLID as possible alternative to bump-bonding.

TSV with Via Last approach below the wire bonding pads for backside readout

Similar to Bonn project, but more 'aggressive technology
⇒SLID ok for smaller pitch
⇒3µm 1:10 vias

3 FEI4 wafer already available
Sensors in production (VTT, Micron)





Successful test of SLID with FEI3:
100% connected pixels, radiation tested
Challenge: adapt TSV technology to FEI4 (etching from backside instead of frontside)

Barcelona

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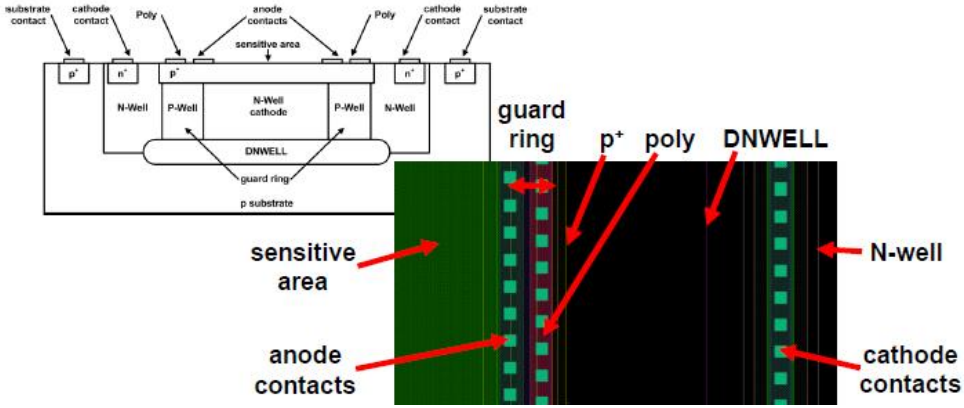
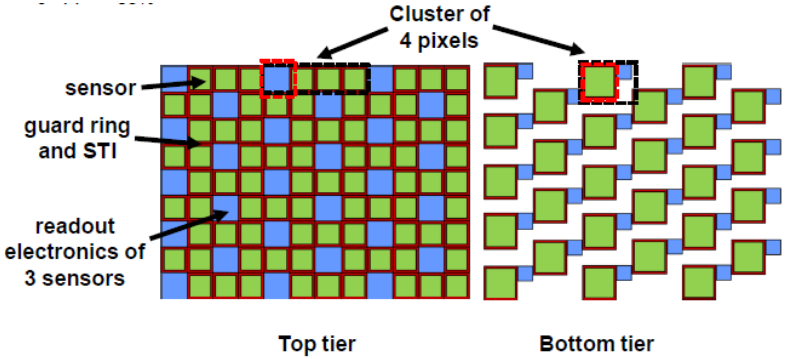
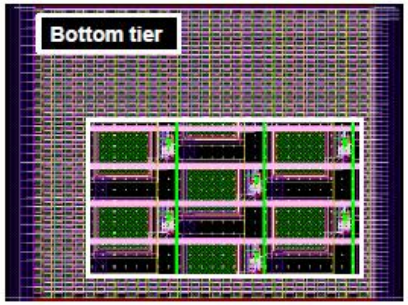
Basic idea: tracking sensor based on Geiger APD realized in CMOS (incl. readout)

Use 2 tier 3D to increase fill factor







Option 1: Tezzaron/Chartered MPW in Sept. 2012
alternatively (e.g. design rule mismatch)
Option 2: AMS 0.35µm HV + AIDA interconnection

Because of late schedule not yet in D3.1 => addendum

Other projects

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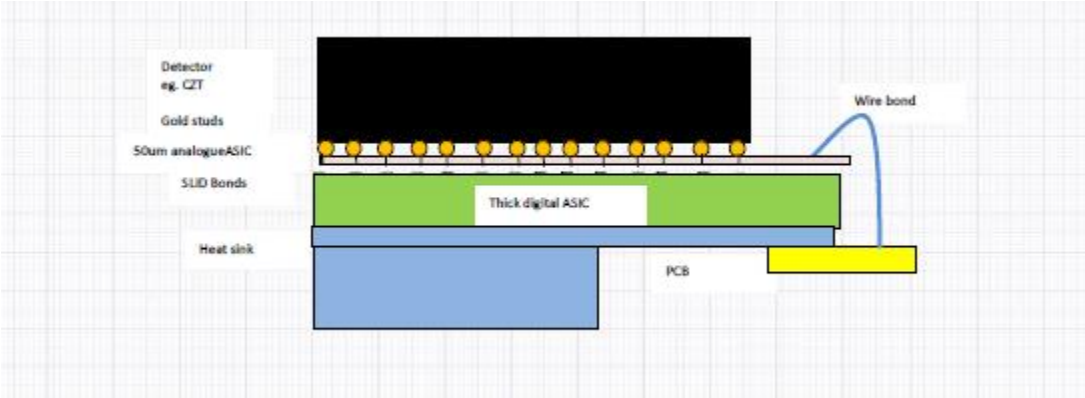
RAL:

2 tier readout chip for GZT X-ray detector using EMFT SLID interconnection & TSVs
ASICs exist & tested

Not yet approved by AIDA since not fully funded

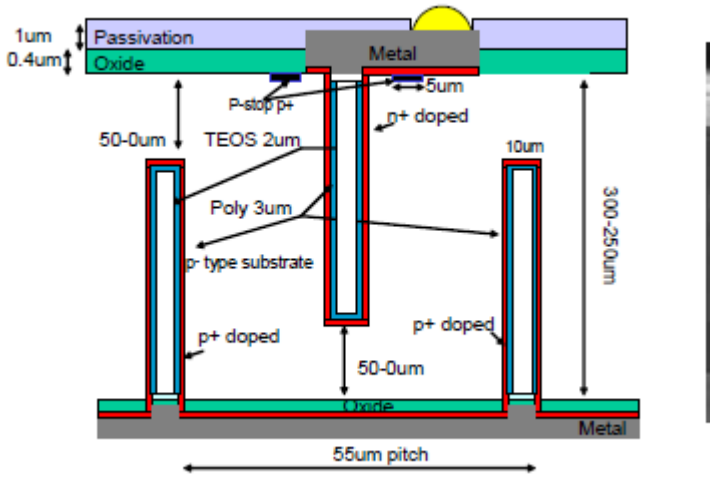
Uppsala will join
⇒Could get 'critical mass'
Decision April/May



CNM:

Offer sensors (slim edge, 3D)
Masks available for Medipix, & FEI4

Interest by CERN and LAPP



Milestones

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Schedule of relevant Milestones

Milestone number [88]	Milestone name	Lead beneficiary number	Delivery date from Annex I [89]	Comments
MS18	Availability of wafers with ASIC	18	17	Layout of ASICs in MPW (Task 3.2)
MS19	Submission of dedicated sensors for 3D interconnection	11	17	Layout of sensors (Task 3.2)
MS20	Qualification of ASIC and sensors for 3D interconnection	18	25	Laboratory tests (Task 3.2)
MS21	Validation of first set of IP blocks	1	26	Laboratory tests and full documentation of functional blocks (Task 3.3)
MS22	3D interconnection processing accomplished	18	36	3D integrated devices available for technology assessment (Task 3.2)
MS23	Enable access to 3D interconnection technology	12	48	Laboratory tests for validation of 3D integration processes (Task 3.2)
MS24	Validation of second set of IP blocks	8	48	Laboratory tests and full documentation of

Deliverables

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List of deliverables

Delive-rable Number [61]	Deliverable Title	Lead benefi-ciary number	Estimated indicative person-months	Nature [62]	Dissemi-nation level [63]	Delivery date [64]
D3.1	Organisation of the 3D production	18	20.00	R	PU	12
D3.2	Availability of wafers of ASIC electronics	18	30.00	R	PP	17
D3.3	Production of dedicated sensors	11	25.00	R	PP	17
D3.4	1st set of macro blocks	1	22.00	R	PU	22
D3.5	Wafer post processing (thinning, TSV)	12	24.00	D	PP	25
D3.6	Component processing	18	12.00	R	PU	29
D3.7	Test interconnection and evaluation	12	24.00	R	PP	36
D3.8	Detectors in 3D available for assessment	18	24.00	D	PP	40
D3.9	2nd set of macro blocks	8	22.00	R	PU	44
D3.10	Assessment of 3D integrated sensors	11	20.00	R	PU	48

Milestones and Deliverables in 2012

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Milestones:

1) MS18 Availability of ASIC wafers, M17 (July 2012)
already met (FEI4, Medipix)

2) MS19 Submission of dedicated sensors, M17 (July 2012)
INFN: production of edgeless sensors (April 2012)
MPP: sensor procurement (CSEM/VTT) (July 2012)

Deliverables:

1) D3.1 Organisation of the 3D production M12 (Feb 2012) **- done**

2) D3.2 Availability of ASIC wafers M17 (July 2012)
already delivered (FEI4, Medipix)

3) D3.3 Production of dedicated sensors M17 (July 2012)
INFN: production of edgeless sensors (April 2012)
MPP: sensor procurement (CSEM/VTT) (July 2012)

IP Blocks: WP 3.3

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Provide sharable IP blocks for HEP
Lead institutions: CERN & LAL
large interest: Bonn, INFN, CNRS (LAL; LAPP; LPNHE, CPPM), AG

A) First set of blocks for 65nm CMOS
depends on CERN (frame contract expected end 2012)
Deliverable date D3.4 (M22, Dec, 2012) might be a problem

B) Second set of blocks for SiGe
First: technology choice: 350nm (AMS) or 130nm (IBM, ST, IHP)
depends on the cost
(130nm is rather expensive and needs a additional contribution)
decide within one year
Deliverable date D3.9 (M44 should be ok.

Conclusions

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WP3.2 (3D integration) fragmented into many sub-projects (6 + 1)
Thanks to the institutes willingness to contribute own resources and to the availability of ASICs (FEI4, Timepix) we can afford this large program

This allows exploring different technologies (of different maturity, potential, and risk) and different sensor readout ASIC concepts (Planar/3D/CMOS-sensors) and 1 or 2 tier ASICs in different technologies (130nm, 65nm)

Depending on the technological challenges the projects have different schedule. However, the ones using 'mature' will certainly meet the AIDA milestones and delivery dates.

WP3.3 has also defined its program, providing IP blocks for 65nm CMOS and SiGe.
65 nm CMOS depends on CERN to provide a frame contract with a manufacturer. The target date may force us to delay D3.4

SiGe is on a longer timescale. Next step is to choose the best (or affordable) technology.