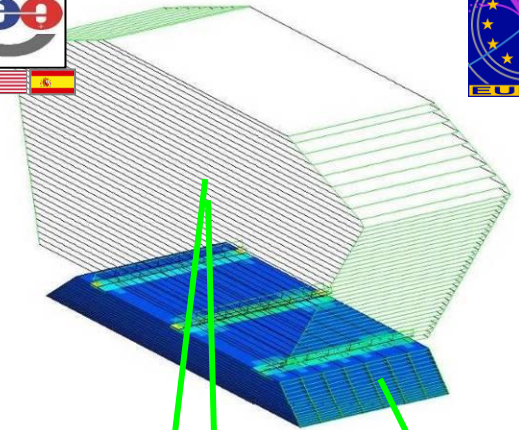
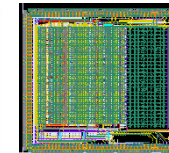
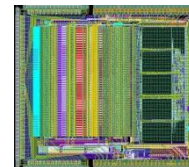


ANNUAL MEETING WP9.5 FEE status

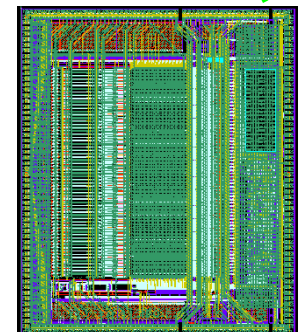
- **Schedule presented at the AIDA Kick Off meeting**
 - **2011: Characterization of the 2nd generation ROC Chips**
 - Dedicated run produced in **March 2010**
 - 25 wafers received in June
 - 20 000 chips packaged in the US
 - **2012: Submission and test of one of the 3rd generation chips**
 - **2013: Submission of a second 3rd generation chip**
 - **August 2013: Report**
- **Budget for 3rd generation of electronics:**
 - 31k€ (ECAL) + 50 k€ (Hadronic Calorimeter) => 2 chip submissions
 - 30 ppm
- **Cost:**
 - Multi Project runs (MPW): 1k€/mm²
 - Packaging: \$3500
 - Testboard: 1500 €



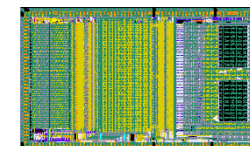
HARDROC2/MICROROC
SDHCAL RPC/μMEGAS
64 ch 20 mm²



SKIROC2
ECAL Si
64 ch. 65 mm²



SPIROC2
AHCAL SiPM
36 ch 32 mm²



0.35μm SiGe AMS technology

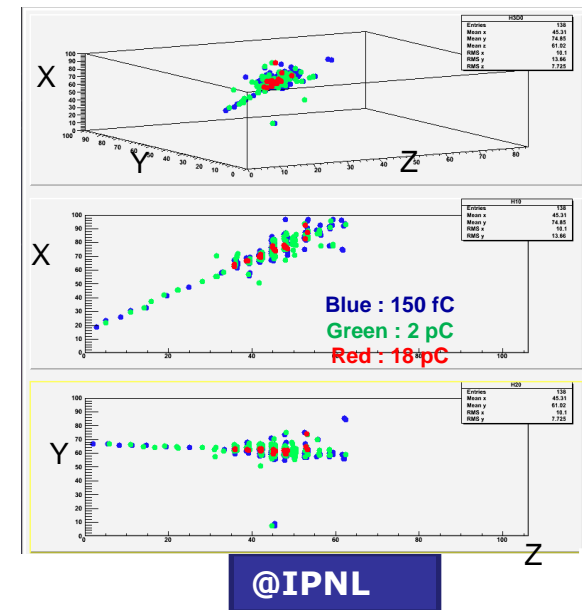
HARDROC2 Characterisation

• HARDROC2: 64 channels (RPC DHCAL)

- preamp + shaper+ 3 discris (semi digital readout)
- Auto trigger on 10fC up to 20 pC
- 5 0.5 Kbytes memories to store 127 events
- Full power pulsing => 7.5 $\mu\text{W}/\text{ch}$
- 2010 TB : 1 m2 (144 HR2b)
 - power pulsing in magnetic field successfully tested
- SDHCAL technological proto with 40 layers (5760 HR2 chips) built in 2010-2011.
 - Testbeam summer 2011: pb with the DAQ2 (HDMI) + pb of cooling
 - TB November 2011: 6 detectors and USB DAQ: good performance of the electronics and detector
- Next TB (April 2012) with 40 detectors and intermediate DAQ (HDMI & DCC cards for synchronization and USB for config & readout)
- HARDROC3 FE: No major modifications needed



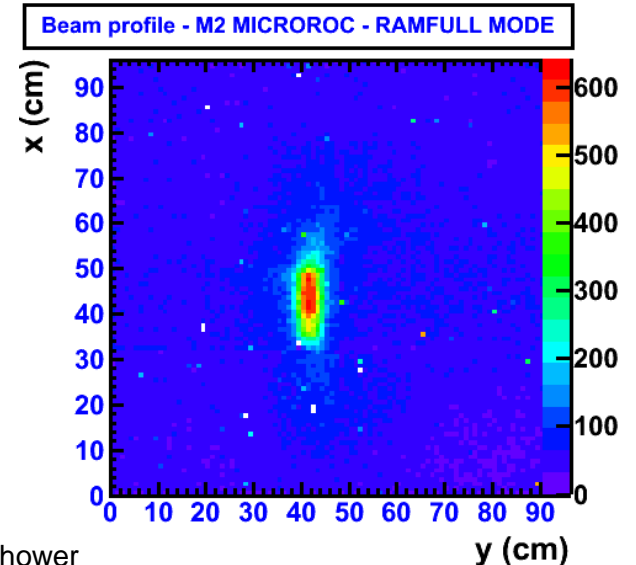
Cosmic hadronic shower



- **MICROROC: 64 channels μ Megas DHCAL**

- ❑ Very similar to HARDROC except for the input preamp and shapers (100-150 ns)
- ❑ Noise: 0.2fC (Cd=80 pF). Auto trigger on 1fC up to 500fC
- ❑ Pulsed power: **10 μ W/ch** (0.5 % duty cycle)
- ❑ 1 m² in TB in August and October 2011. Very good performance of the electronics and detector (Threshold set to 1fC).
- ❑ 2012: 4 m² in TB

@LAPP



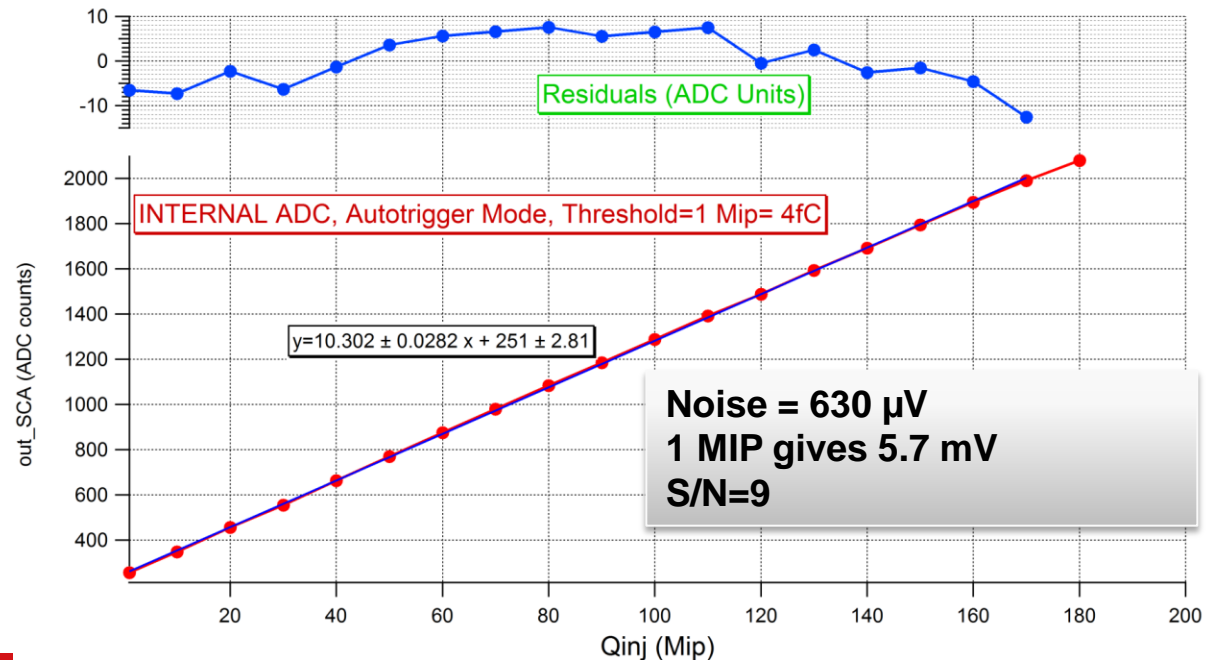
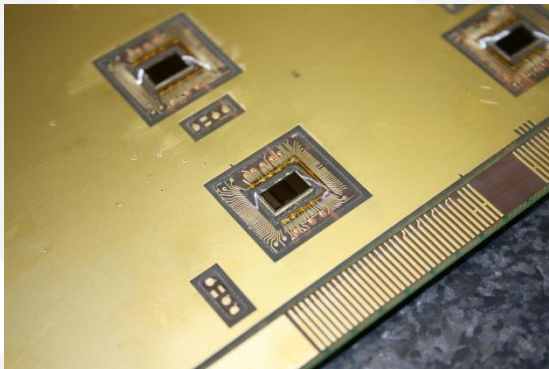
Cosmic hadronic shower



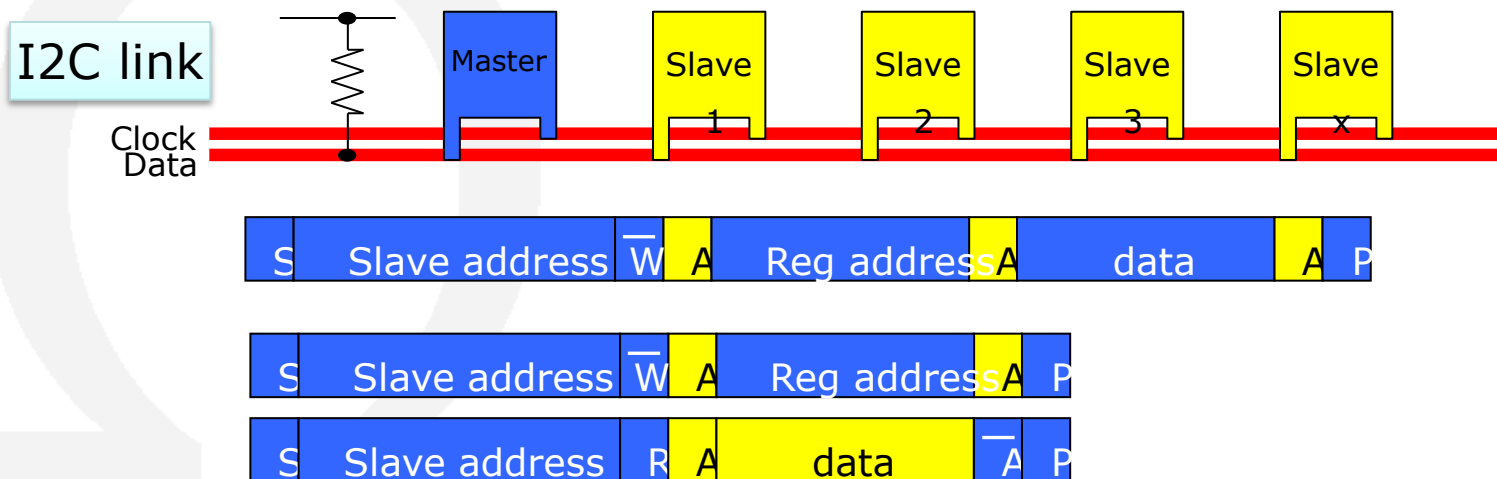
- **SPIROC2: 36 channels for AHCAL (SiPM)**
 - ❑ Autotrigger on 1 spe (150 fC), 16 depth SCA for Charge measurement (up to 300 pC) and Time measurement (< 1 ns)
 - ❑ 2 memories of 2K bytes to store Charge and Time measurements from the internal 12 bits ADC
 - ❑ Pulsed power: **25 μ W/ch** (1 % duty cycle)
 - ❑ Testbench measurements at ORSAY and at system level at DESY show some defects
 - ✓ Design of a new input preamp to solve rate dependency pb + coherent noise + Crosstalk (HG/LG)
 - ✓ Building block with this new FE tested in December 2011: Very good performance
 - » HG Preamplifier + Slow shaper: $V_{max} = 46$ mV/pe, Noise RMS = 2,3mV \Rightarrow **SNR ~ 20**
- \Rightarrow Submission of SPIROC2C (Feb 2012) with this new FE**
- ✓ **Klaus2 chip** (Heidelberg University): also a good candidate for the FE of Spiroc \Rightarrow "KlausROC"
- ❑ TDC: First tests of TDC ramps in SPIROC2b show promising results. Resolution < 1 ns (dominated by linearity) \Rightarrow New tdc in SPIROC2c to minimize dead time
- ❑ HBU2 tested successfully in DESY test beam (March 2012)

- **SKIROC2**: 64 channels for ECAL (Si pin diodes)
 - ❑ Autotrigger on 0.5 MIP (2 fC), 15 depth SCA for Charge measurement (0-2500 MIPs) and Time measurement (< 1 ns)
 - ❑ 1 memory of 4K bytes to store the digitized measurements of Charge and Time by the internal 12 bits ADC
 - ❑ Pulsed power: **25 μ W/ch** (1 % duty cycle)
 - ❑ Similar to SPIROC2 except for the input PA \Rightarrow SKIROC2 benefits from SPIROC measurements
 - ❑ Testbench measurements: very good performance
 - ❑ Test beam @ DESY starting 26th March (FEV boards with sensor and 4 packaged SKIROC2)

FEV board



- 2nd generation ROC chip
 - Auto-trigger, analog storage, digitization and token-ring readout, common DAQ
 - Power pulsing : <1 % duty cycle
- 3rd generation ROC chip
 - **Independent channels (= Zero suppress)**
 - 64/36 address pointers
 - ReadOut, BCID, SCA (Spiroc and Skiroc) management
 - => Digital part much more complicated**
 - SCA depth: 8 instead of 16
 - Possibility to use "Roll mode" by Slow Control: circular memory very useful for Testbeam
 - New TDC with no dead time
 - **New Slow Control (Triple voting) using I2C link** (while keeping the « old SC » system)



- **1st submission (Feb 2012): SPIROC2C** (*2nd generation chip*)
 - new input preamp: less sensitive to coherent noise, better Signal-to-Noise ratio, no pedestal shift and no rate dependency
 - SC: old one (No I2C)
 - Input 8-bit DAC slope uniformity improved
 - TDC : dead time decreased
 - Pin to pin compatible with spiroc2b so noise measurements can be performed at the system level using the existing HBUs
 - Die size: 32 mm² => MPW run 32 k€ (**CALICE/EUDET funding**), 27th Feb 2012

- **2nd submission (June 2012 or September 2012): HARDROC3**
 - « Simple » chip compared to Spiroc3: I2C, independent channels, circular memory, one register/channel, temperature sensor
 - No major modifications in the analog part
 - HR3 won't be pin to pin compatible with HR2 and probably in a different package: TQFP208 instead of TQFP 160 (same size and thickness)

⇒ New 1 m² RPC chamber to be built to test HR3 at the system level

 - Die size should be ~30 mm² => 30 k€ + 5K test setup (AIDA funding)

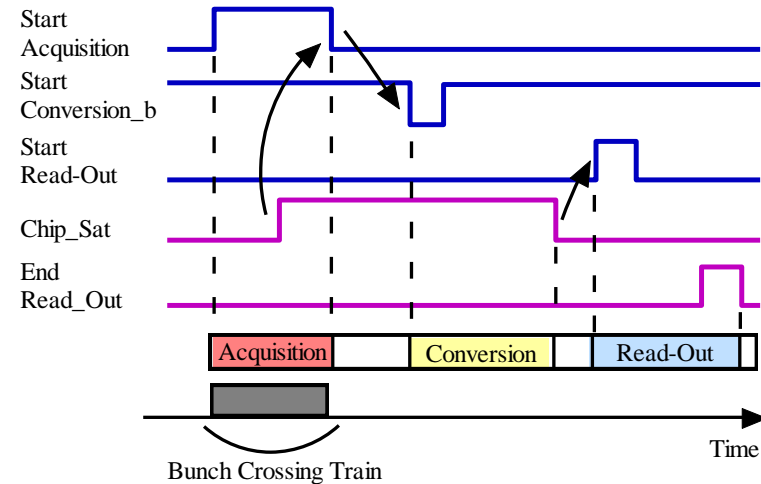
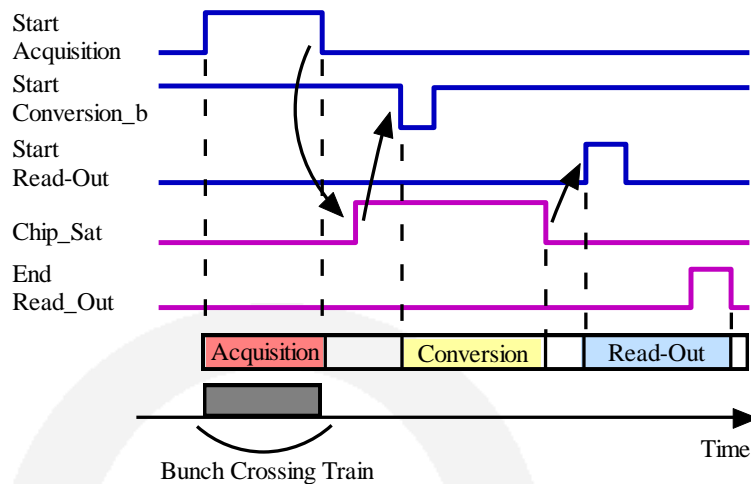
- **3rd submission (March 2013) SPIROC3: Complex chip**, many parts still to be tested on test bench and at the system level
 - I2C, independent channels but also new PA, TDC , SCA
 - Hardroc3 and Spiroc2c test feedback necessary before submitting Spiroc3
 - Size should be ~40 mm² => 40 k€ + 5 K test setup (AIDA funding)

- 2011:
 - 2nd generation ROC chip characterisation
 - no money spent, 4 ppm (0.3 FTE) for the design of the digital part of the 3rd generation of ROC chip
- 2012:
 - HR3 design and submission (June or September)
 - Test of HR3 and SPIROC2C before submitting SPIROC3
 - 35k€ for HR3, 16 ppm (1.3 FTE)

BACK UP Slides



- DIF sequencing (Acq, Conv and Readout):
 - Backward compatibility with 2Gen ROC chips sequencing
 - Use of ChipSat signal
 - Daisy chained chips for readout

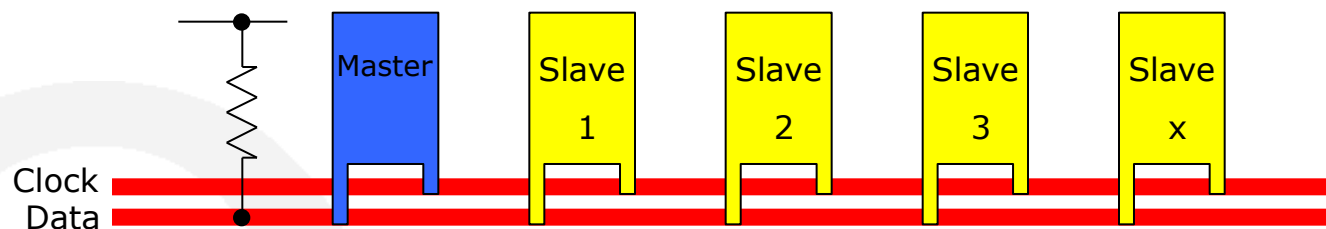


- Possibility to use Roll mode by Slow Control:
 - If RollMode = "0" → Backward compatibility with 2Gen ROC chips behavior
 - Only the N first events are stored
 - If RollMode = "1" → 3Gen ROC chips behaviour
 - Use the circular memory mode
 - Only the N last events are stored

3Gen ROC chips: common features



- Slow control parameters:
 - Backward compatibility with 2Gen ROC chips slow control
 - Use of classical shift register slow control
 - Embedded I2C
 - 7-bit address + 1 general call address (127 chips can be addressed)
 - Access port doubled
 - Bidirectional data line with open collector (Driver will be the same as Dout)
 - Read back capability of SC bits (non destructive)



- Write frame:



- Read frame:



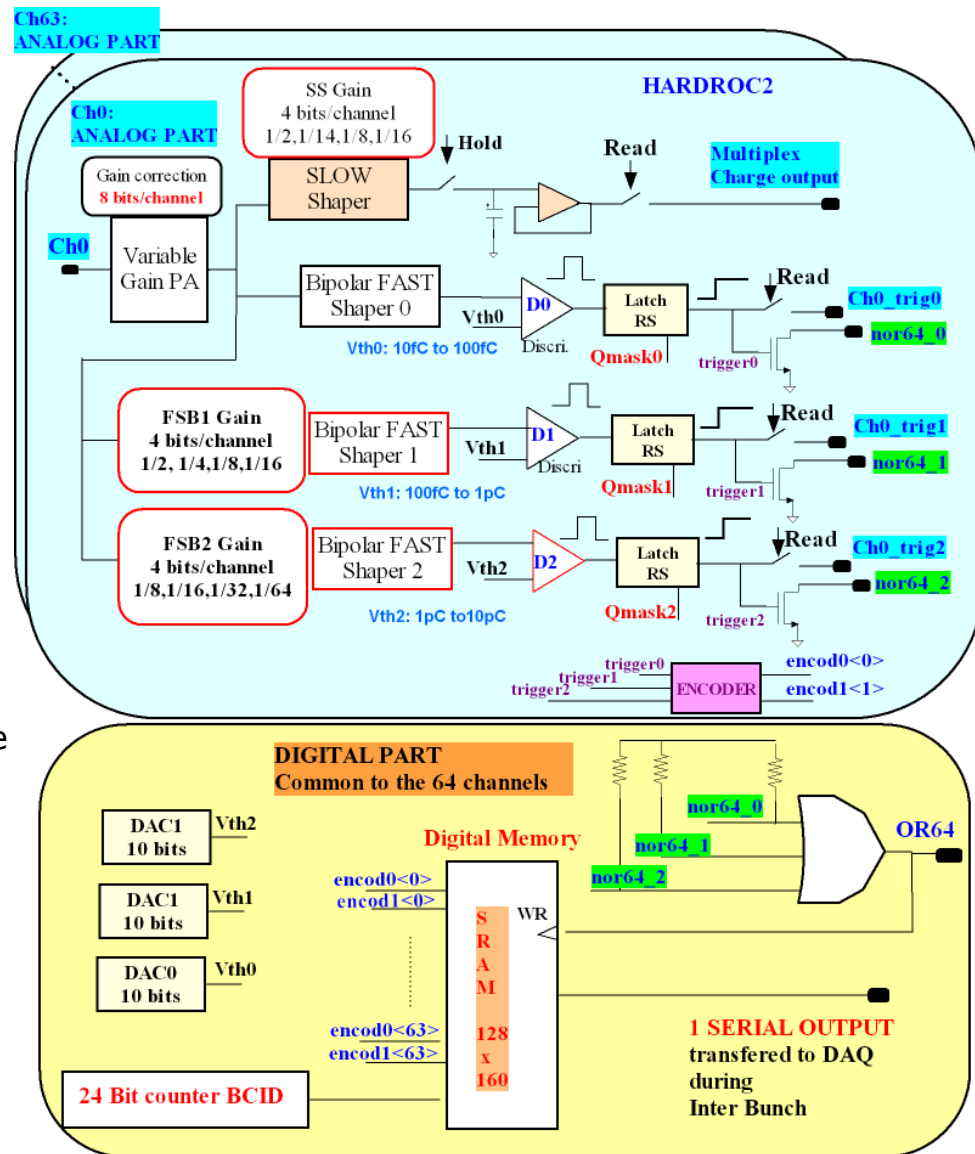
3Gen ROC chips: common features



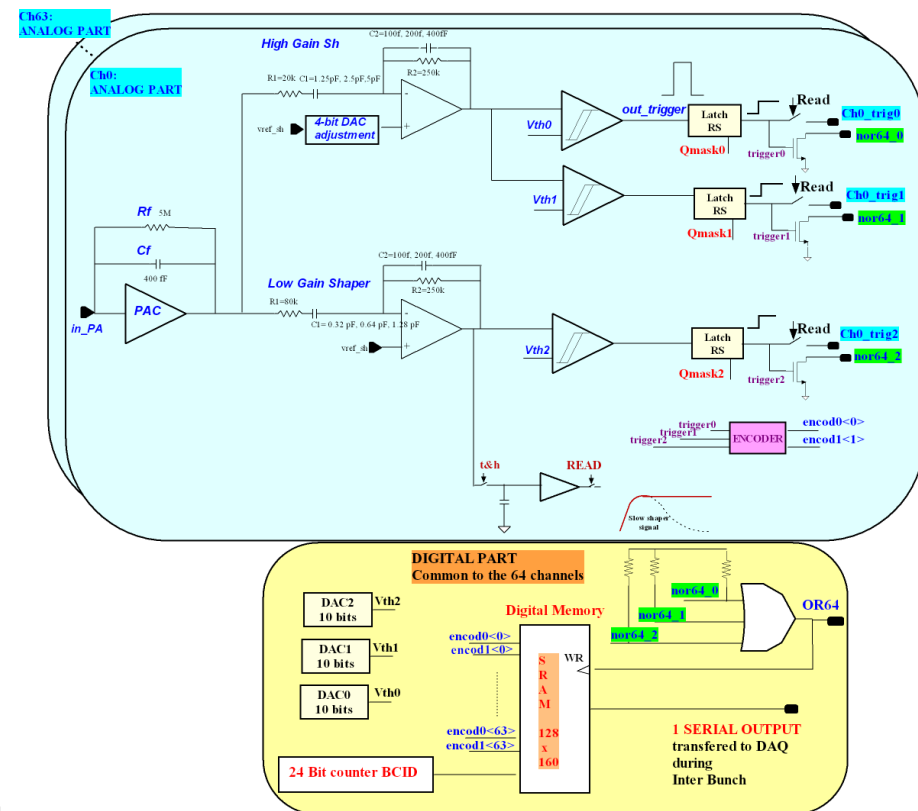
- Extra pin needed for I2C / SC:

HARDROC 2		HARDROC 3		
ShiftReg_In	1	ShiftReg_In	1	Standard SC
ShiftReg_Out	1	ShiftReg_Out	1	
ShiftReg_Clk	1	ShiftReg_Clk	1	
ShiftReg_Rst	1	ShiftReg_Rst	1	
		ShiftReg_Loadb	1	SC with triple voting
		ShiftReg_ReadBack	1	
		Error_Triple_Voting	1	
				I2C
		7-bit I2C @	7	
		2 x (SCL / SDA)	4	
		Select_I2C_Port	1	
		Clk_I2C_SR	1	
		Rstb_I2C	1	Selection I2C or std SC
		Select_I2C_SR	1	
Total	4	Total	4+18	

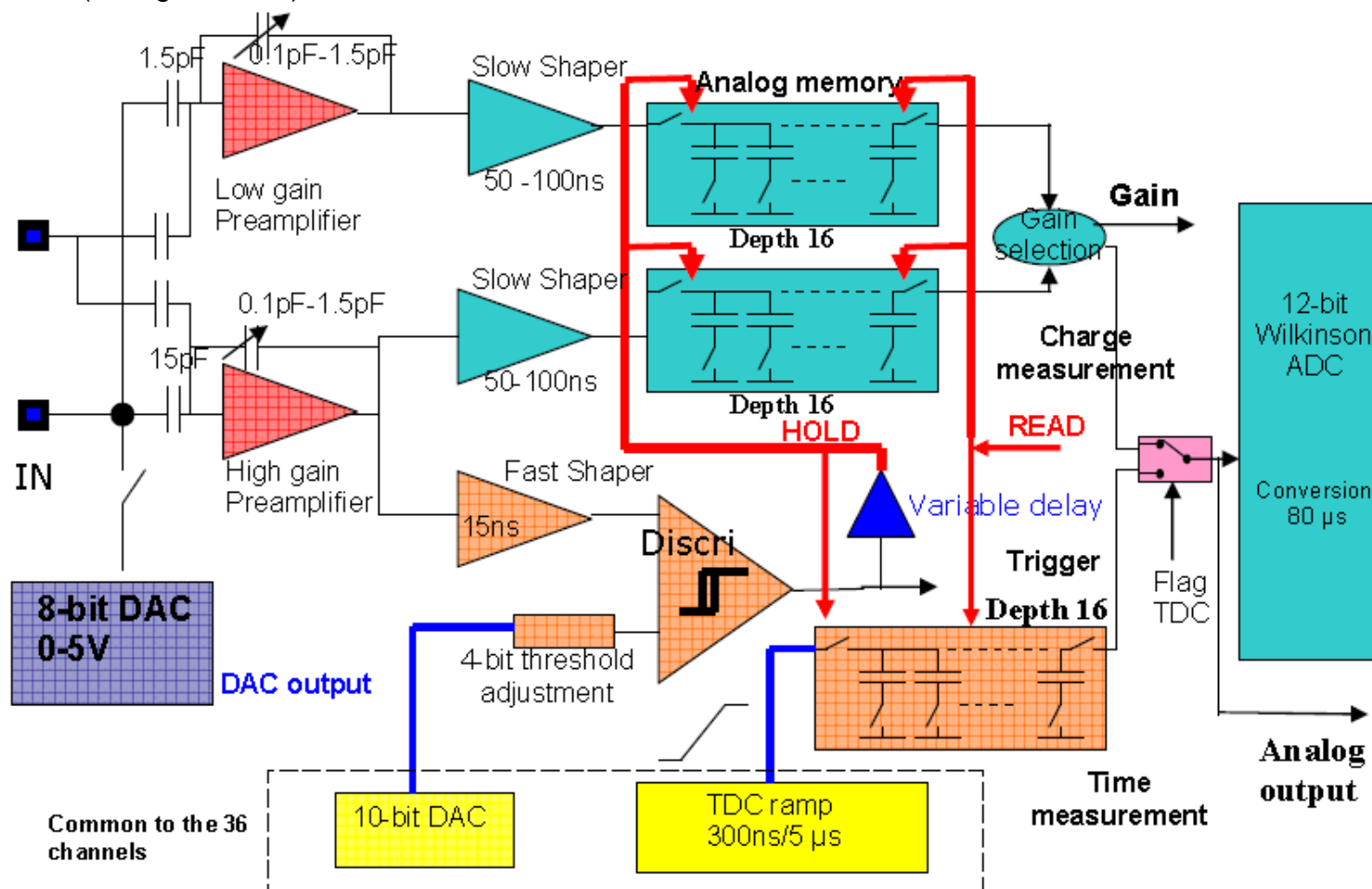
- ❑ **64 channels, 20 mm2**
- ❑ **Variable gain (8bits) current preamps (50 ohm input)**
- ❑ One multiplexed analog output (12bit)
- ❑ **3 shapers, variable R_f , C_f and gains**
- ❑ **3 thresholds** (\Rightarrow 3 DACs):
 - ❑ 10 fC, 100fC, 1pC (megas)
 - ❑ 100fC, 1pC, 10pC (GRPC)
- ❑ **Auto-trigger on 10fC**
- ❑ Store all channels and BCID for every hit. Depth = 128 bits
- ❑ Data format :
 $128(\text{depth}) \times [2\text{bit} \times 64\text{ch} + 24\text{bit}(\text{BCID}) + 8\text{bit}(\text{Header})] = 20\text{kbits}$
- ❑ **872 SC registers, default config**
- ❑ **Power pulsing**



- ❑ Collaboration with LAPP Annecy
- ❑ 64 channels, 20 mm²
- ❑ Same as HARDROC but with charge preamp input stage + **HV protection** and slower shaping + 4bit DAC/channel
- ❑ Preamp optimized for $C_d=80$ pF, noise = 0.2 fC. $C_f=0.4$ pF $R_f=5$ M
- ❑ Maximum input charge : 500 fC
- ❑ Bi-gain shaper (G1-G4), peaking tunable 50-200 ns (2 bits)
- ❑ 3 thresholds: Lowest threshold ~2 fC
- ❑ Pin to pin compatible with HR2
- ❑ Store all channels and BCID for every hit. Depth = 128 bits
- ❑ Data format :
 $128(\text{depth}) \times [2\text{bit} \times 64\text{ch} + 24\text{bit}(\text{BCID}) + 8\text{bit}(\text{Header})]$
 = 20kbits
- ❑ **872 SC registers**, default config
- ❑ **Power pulsing**



- 36 channels , 32 mm²
- Bi-gain (autogain)
- Analogue Memory depth : up to 16 events can be stored (columns)
- 2 × 36 channels (Charges/Times)



64 channels, 70 mm2

