AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

AIDA WP9 Forward Calorimetry Status of Readout Electronics and Future Plans

Marek Idzik AGH-UST

Faculty of Physics and Applied Computer Science
AGH University of Science and Technology

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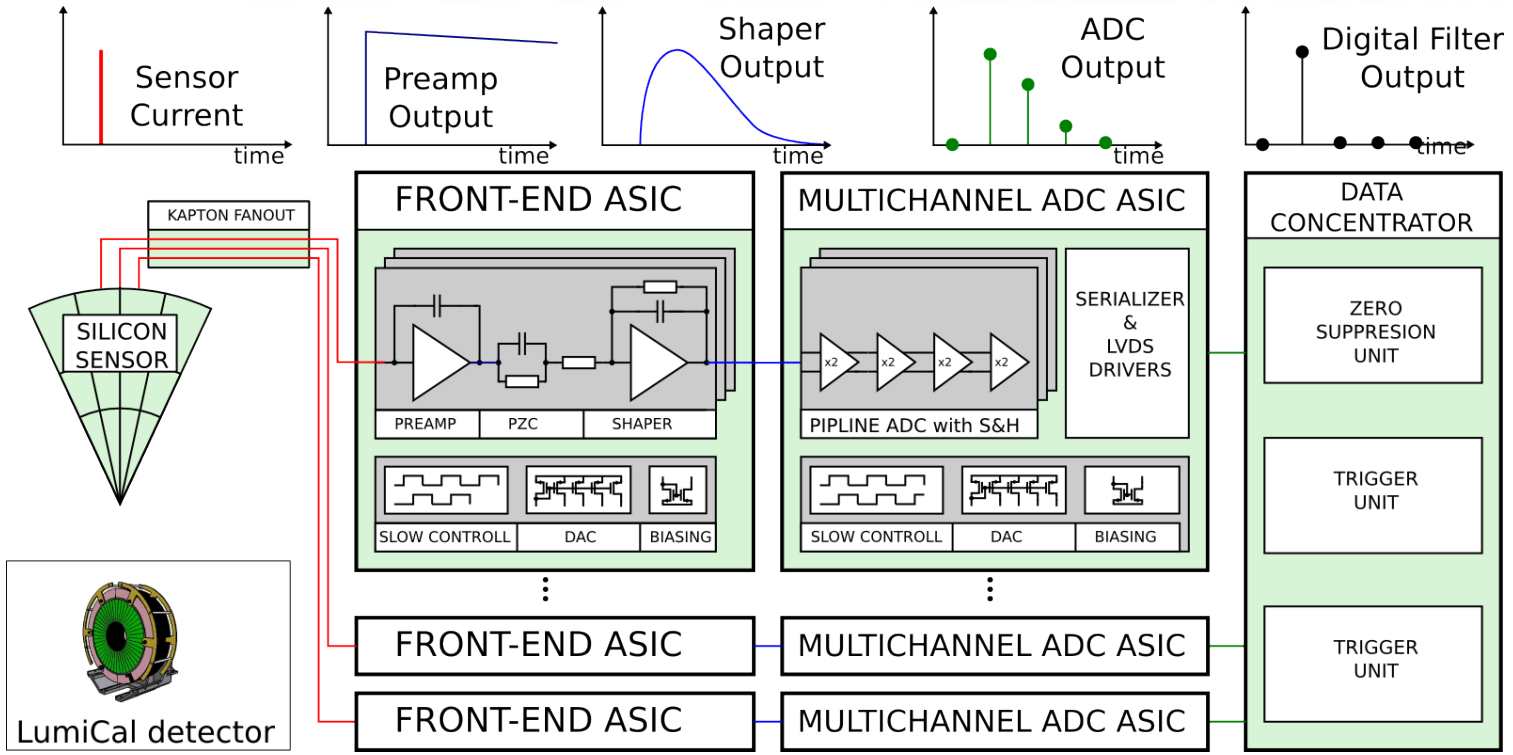
Outline

- Status and ongoing works with readout electronics developed in the past in AMS 0.35um
- Development of new readout for LumiCal detector in IBM130nm

All works done by now have been supported with non-AIDA resources. To use more efficiently the limited AIDA funds we will start to spend it in 2012 !

Present Readout of LumiCal detector

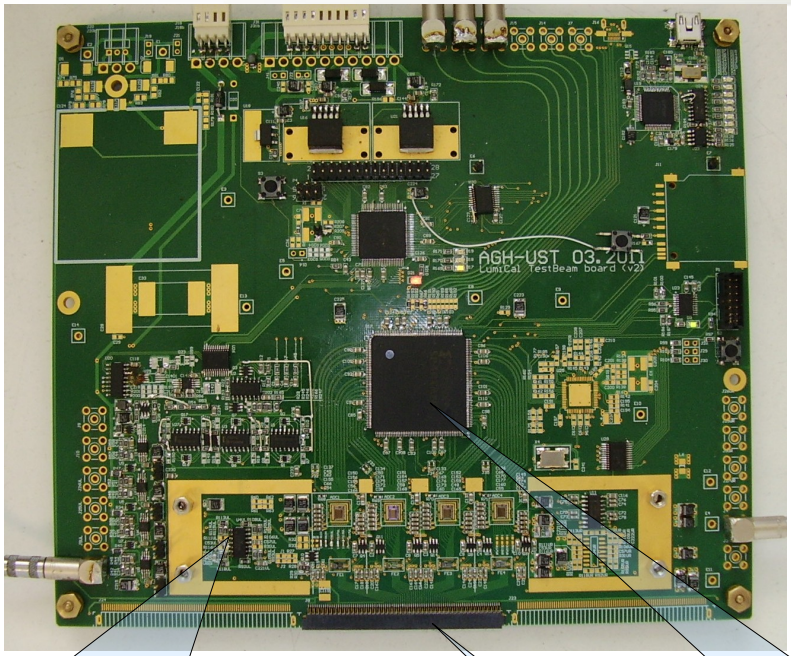


Multichannel readout comprising 8 channel front-end and ADC ASICs, plus FPGA data concentrator was developed in AMS 0.35um, and integrated in the 32 channels system.

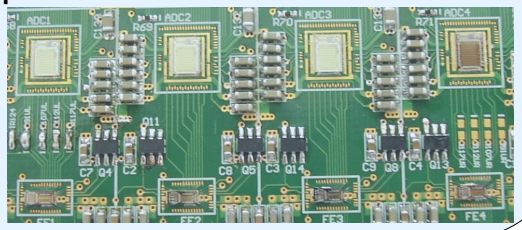
FE - M. Idzik, Sz. Kulis, D. Przyborowski, "Development of front-end electronics for the luminosity detector at ILC", NIM A 608. 32 p.169-174, 2009

ADC - M. Idzik, K. Swientek, T. Fiutowski, Sz. Kulis, D. Przyborowski "A 10-bit multichannel digitizer ASIC for detectors in particle physics experiments", IEEE Trans. Nucl. Sci. 2012, in print

32 channels readout module



4 pairs of front-end+ADC ASICs



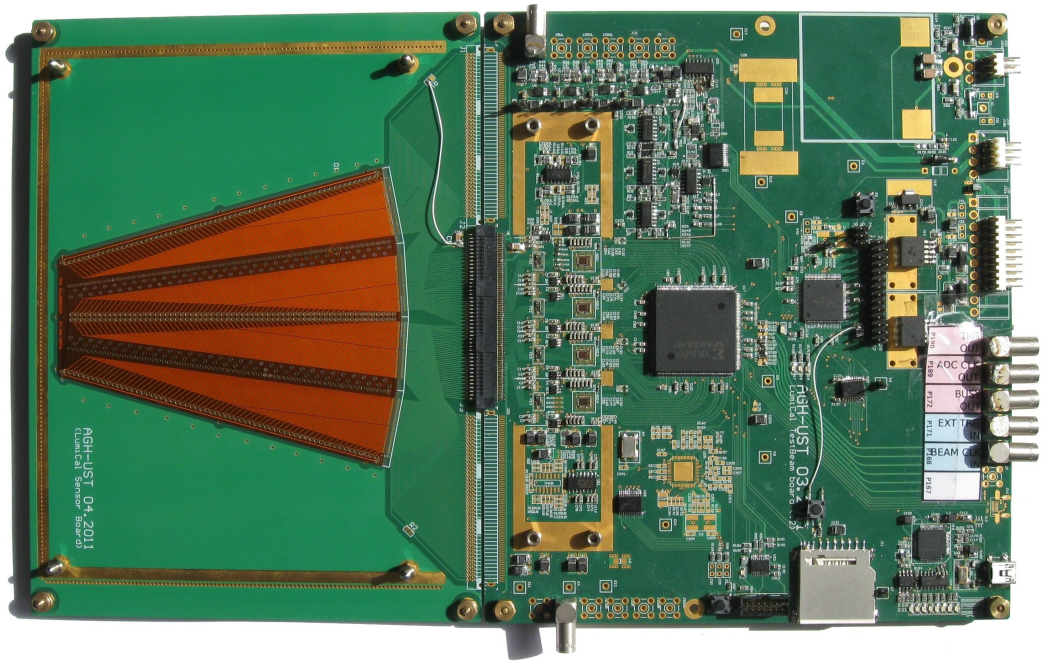
Data concentrator
Xilinx Spartan 3E

sensor
connector

- 32 channels fully equipped channels (Front-end +ADC)
- ADC sampling rate is up to 20 MS/s (6.4 Gbps)
- Extended trigger mechanism
  - External CMOS / LVDS
  - Self triggering on ADC values
  - Software
- Data can be transferred using USB
- Signal handshaking with Trigger Logic Unit (TLU)
- ADC Clock source
  - Internal (asynchronous with beam operation)
  - External (beam clock usec for synchronization) ILC mode

Sz. Kulis, A. Matoga, M. Idzik, K. Swientek, T. Fiutowski, D. Przyborowski "A general purpose multichannel readout system for radiation detectors", Journal of Instrumentation JINST 7 T01004 2012

LumiCal detector module



Good performance of detector module verified on 2 testbeams in 2011

Power pulsing (1ms_ON/199ms_OFF, ASICs Power_ON/OFF ~40)

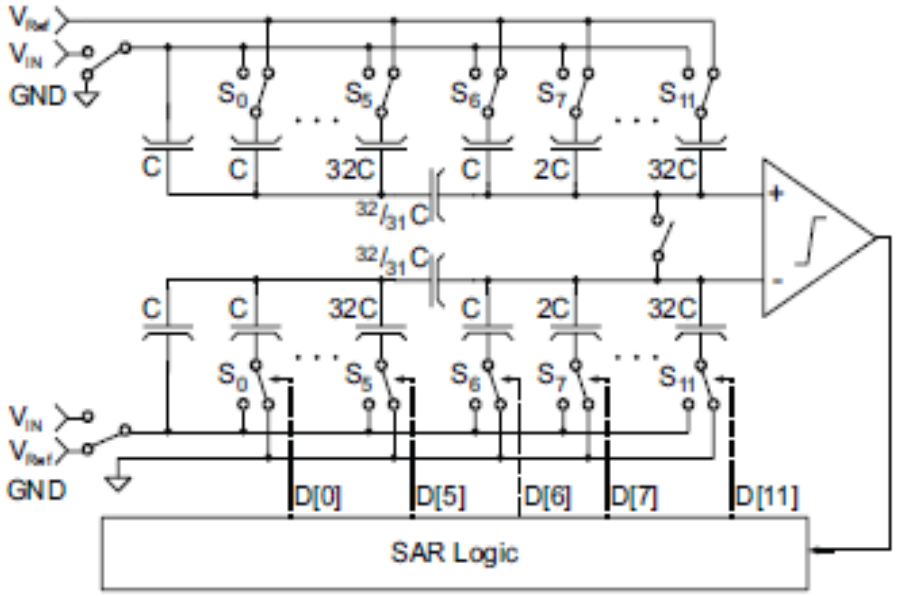
Two modules available (Cracow, Zeuthen), with two sensor boards (BeamCal, LumiCal)

Using deconvolution, tests for CLIC are performed with asynchronous readout

New developments in IBM 130nm

- Readout system developed in AMS 0.35um works very well, but in view of final readout of LumiCal at ILC/CLIC some parameters (power consumption, speed, radiation hardness) would need to be improved...
- The design of readout with the same architecture (FE+ADC in each channel) has been started in IBM 130nm
  - Submitted prototypes
    - 10-bit SAR ADC, PLL, SLVS I/O
  - Design in progress... to be submitted in 2012
    - Front-end, updated 10-bit SAR ADC

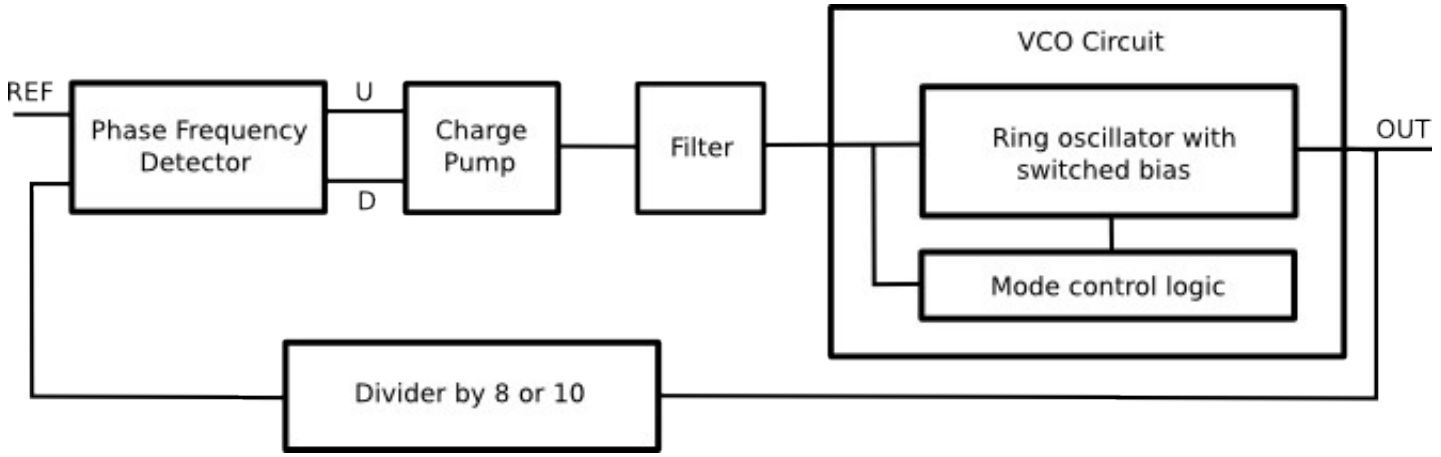
Segmented/Split capacitor SAR ADC



First prototype in IBM 130nm submitted in February 2012

- Architecture: 10-bit SAR ADC with segmented DAC
- Scalable frequency (up to ~50 MS/s) and power consumption
- 1-2mW at 40MS/s
- ~150um pitch

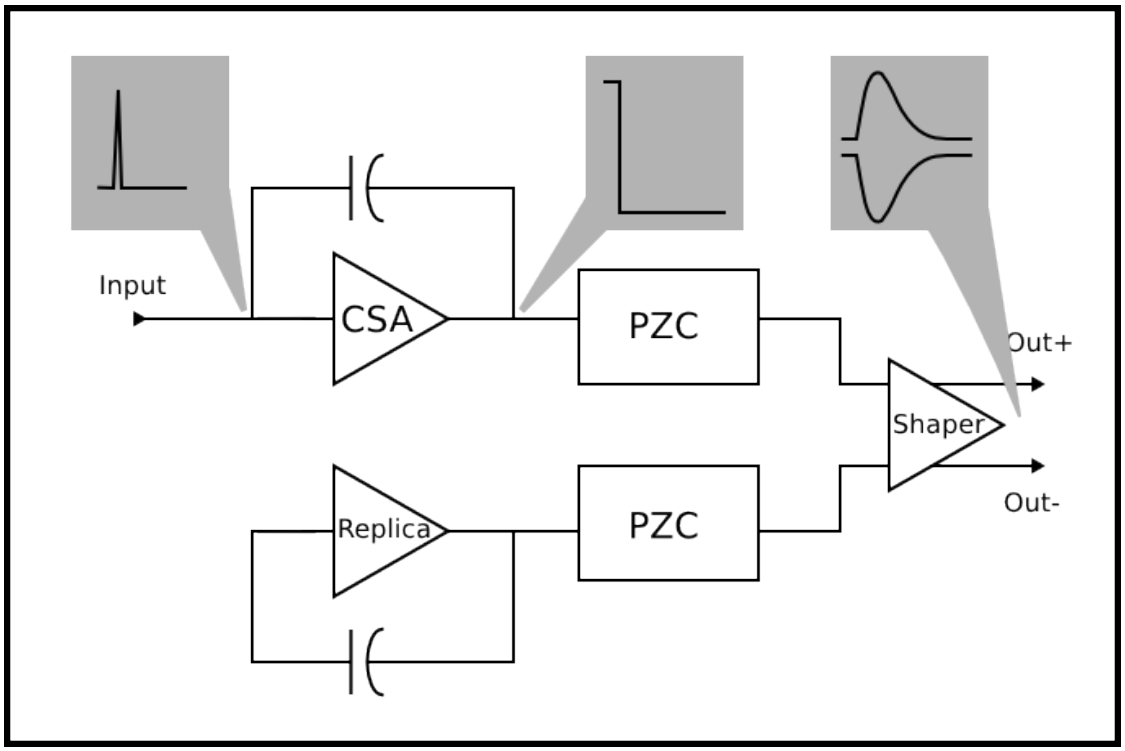
PLL for data serialization



First prototype in IBM 130nm submitted in February 2012

- Architecture: type II PLL with 2nd order filter
- Scalable frequency and power consumption
- Automatically switched VCO frequency range
- VCO frequency range 60MHz – 520MHz, divided by 8 or 10
- Power consumption <0.5mW at 500MHz
- Area 200um x 160um
- Jitter RMS<5ps

Front-end design in IBM 130nm, in progress...



Specifications, still under discussions:

- Charge Sensitive Preamplifier with PZC
- Fully differential CR-RC Shaper
- Variable gain: 0.15 $^{mV}/_{fC}$ – 15 $^{mV}/_{fC}$

(Two modes: calibration – high gain and physics – low gain**)**

- Variable peaking time: 25 – 100 ns
- Cdet ~ 5 - 30 pF
- Noise < 0.4 fC (SNR ~ 10 for MIP)
- Power cons. ~2mW/channel

Summary and future plans

- First prototypes of main LumiCal readout blocks, designed in IBM 130nm, should be available by the end of 2012
- In optimistic scenario the projects of multichannel versions may designed and submitted in 2013. Since there are very limited AIDA resources at AGH-UST, for this aim more resources will need to be found.

Thank you for your attention