Motivation for 65nm CMOS technology

- Benefits

  - Higher density, less material
  - Power
  - Enhanced radiation hardness (@ regular layout)
  - Extensive existing standard cells libraries

- Drawbacks

  - Learning curve (not a real issue)
  - Cost (but one transistor is cheaper)

Example: TSMC CMOS 65nm process and libraries

Analog: Mixed-signal + RF

- Voltage supply: core 1.0, 1.2V
  1.8, 2.5, 3.3V I/O transistors
- MiM and MoM (metal-oxide) caps
-Thick copper for inductors
- Diodes
- Poly diff, N-well resistors
- Deep N-well (noise immunity)

Digital:

- General purpose std cells 850kGate/mm2
- Very low power
  0.8, 1V
- 10-12LM

TSMC: 35 standard cells libraries:
http://www.magma-da.com/partners/standardcelllibs_65nm.aspx

Radiation Hardness

Below 130nm, CMOS is more and more intrinsically radiation-hard, but not enough…
e.g. 65nm SRAM @ <100kRad TID (TNS Vol.57 n4 Aug 2010 pp2079-2088)

65nm CMOS

- A. Marchioro (CERN) is evaluating 65nm CMOS providers (UMC, ST, TSMC, IBM)

- CERN will make a decision and provide in November a design-kit + rad-hard libraries to the community

- LAL, LAPP, and LPNHE have requested access to the regular 65nm CMOS TSMC process and libraries through IMEC/Europractice

Costs:

TSMC:

130nm: 2.3kEuros/mm2

65nm: 4 - 5kEuros/mm2

Prototyping through Europractice

Two runs/year

TSMC and UMC 65nm CMOS

TSMC:

– 2 MPW runs/year at Europractice
– 4-9 (10) metal (one thick), 1 poly
– Power core: (1.0) 1.2V
– I/O cells 1.2V 2.5V (3.3V)
– Digital cells, SRAM
– Cost: 5.2k€/mm2 (min. 2.25mm2)
– Cadence PDK

UMC:

– 3 MPW runs/year at Europractice
– 10 metal (two thick), 1 poly 1kΩ/sq
– Power core : 1.0 1.2V
– I/O cells 1.8V 2.5V 3.3V
– SRAM (Faraday),
– 15-600MHz PLL under development
– Cost: 4.2k€/mm2 (min. 3.6mm2)
– Cadence PDK

Potential for 65nm CMOS building blocks development at LAL, LAPP, LPNHE

Analog:

- Bandgap
- OTA
- Preamp (pixels LAPP)
- DAC (LAL)
- ADC (LAL, LAPP)

Digital:

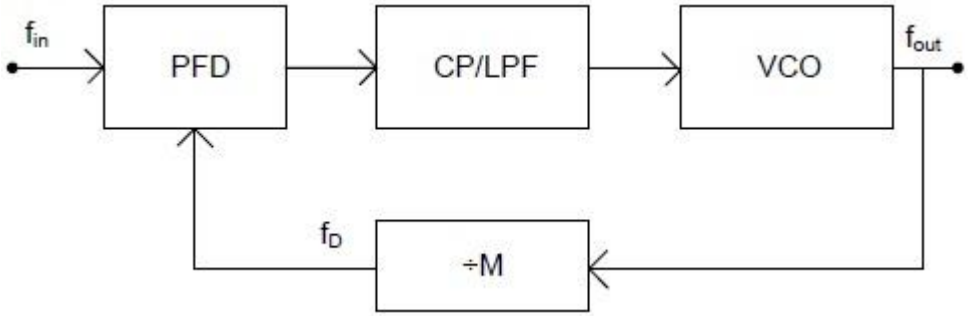
- Service serial link (LPNHE)
  - SPI (Serial Peripheral Interface)
  - I2C (Inter Integrated Circuit) (LAPP)
- JTAG controller (Testability) (LAPP)
- I/O cells
- PLLs (Time Over Threshold, pixels, (LAL, LAPP)

Very strong radiation hardness needed (sLHC requires > 100 Mrads)

Phase Locked Loops

Used as frequency synthesizers

Charge pump PLL (CP-PLL)



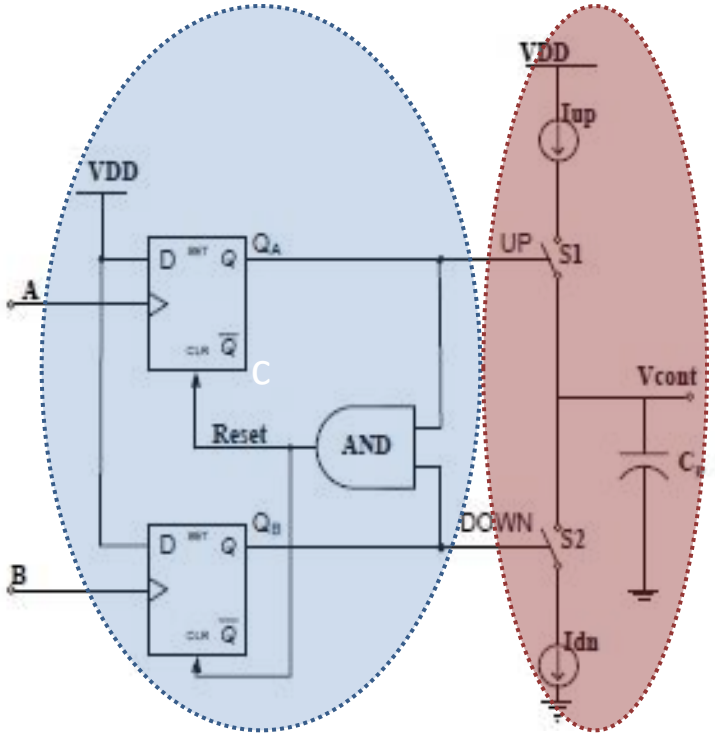
CP –PLL for frequency multiplication

Low power , low jitter , fully integrated

Typical Input frequency : 40 MHz
Output frequency range: 80 MHz-320 MHz

Jeanne Tongbong (LAL)

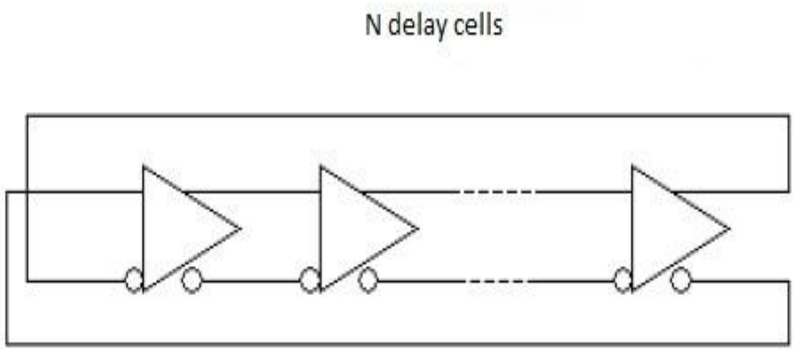
Phase Locked Loops



Phase Frequency Detector (PFD)

Chage Pump(CP) / Loop Filter (LP)

PFD-CP-LP basic implementation

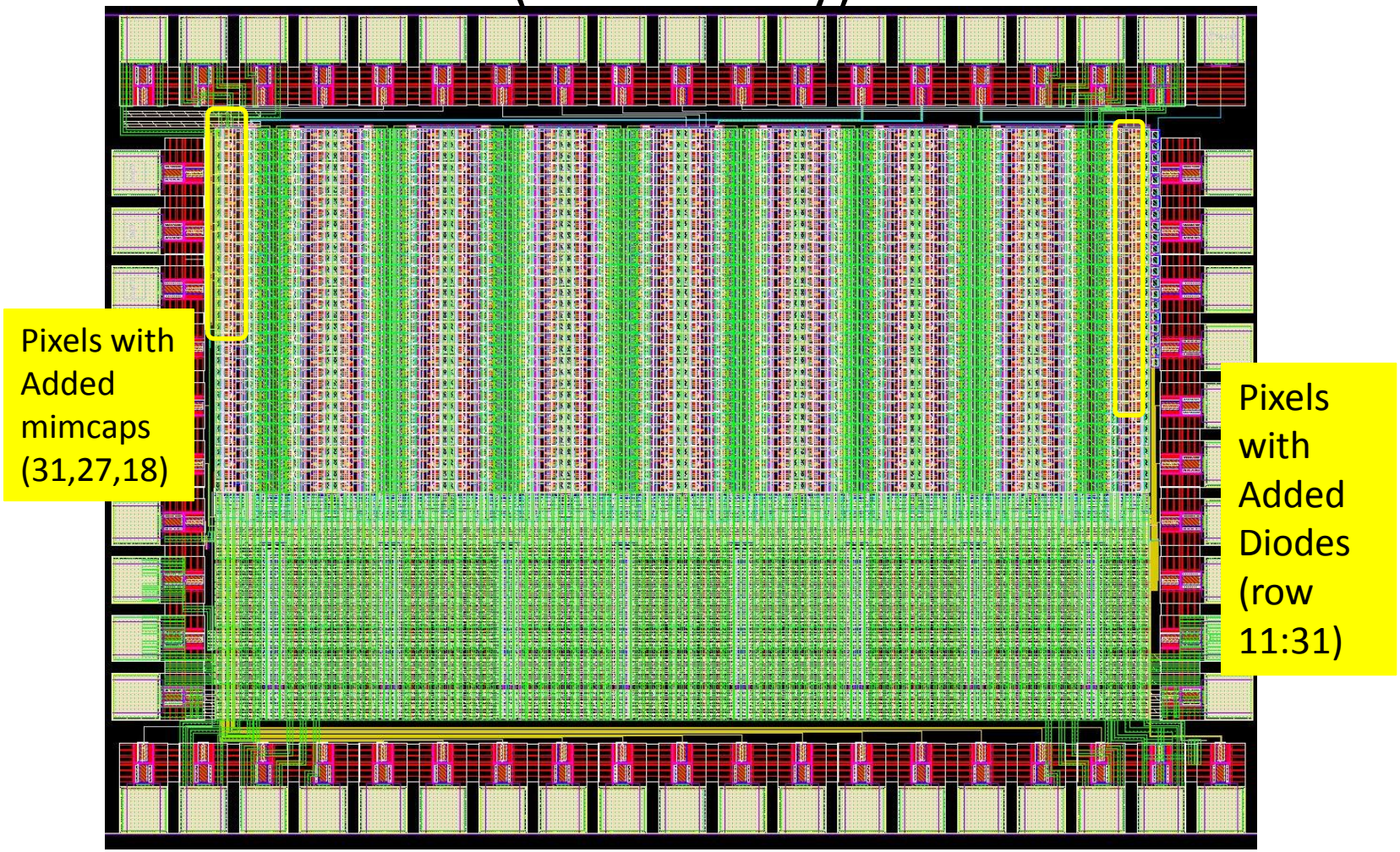


Ring oscillator

Jeanne Tongbong (LAL)

Example: 65nm CMOS FEI4 pixel ASIC

LBNL/CPPM/Bonn/NIKHEF/INFN: ATPIX65A chip (16X32 array)



A. Mekkaoui et al.