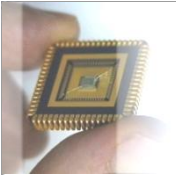


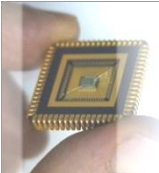
AIDA-WP9

Status and Plans @PM12

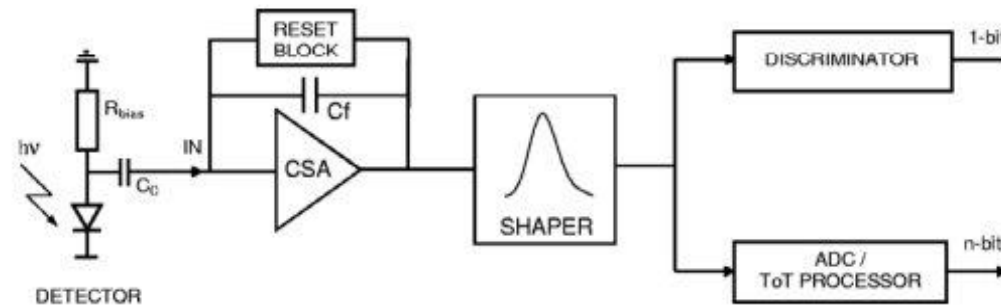
Angel Diéguez
adiiguez@el.ub.edu



- 1) Design flow
- 2) Technology selection
- 3) Functional model of a channel
- 4) Noise analysis
- 5) Amplifier design
- 6) Basic biasing current source
- 7) Future work



Low energy detectors (X-ray)



* Pawel Grybos, "Fast binary readout front-end electronics for silicon strip detectors for low energy x-ray imaging applications."

High energy detectors (particle physics)

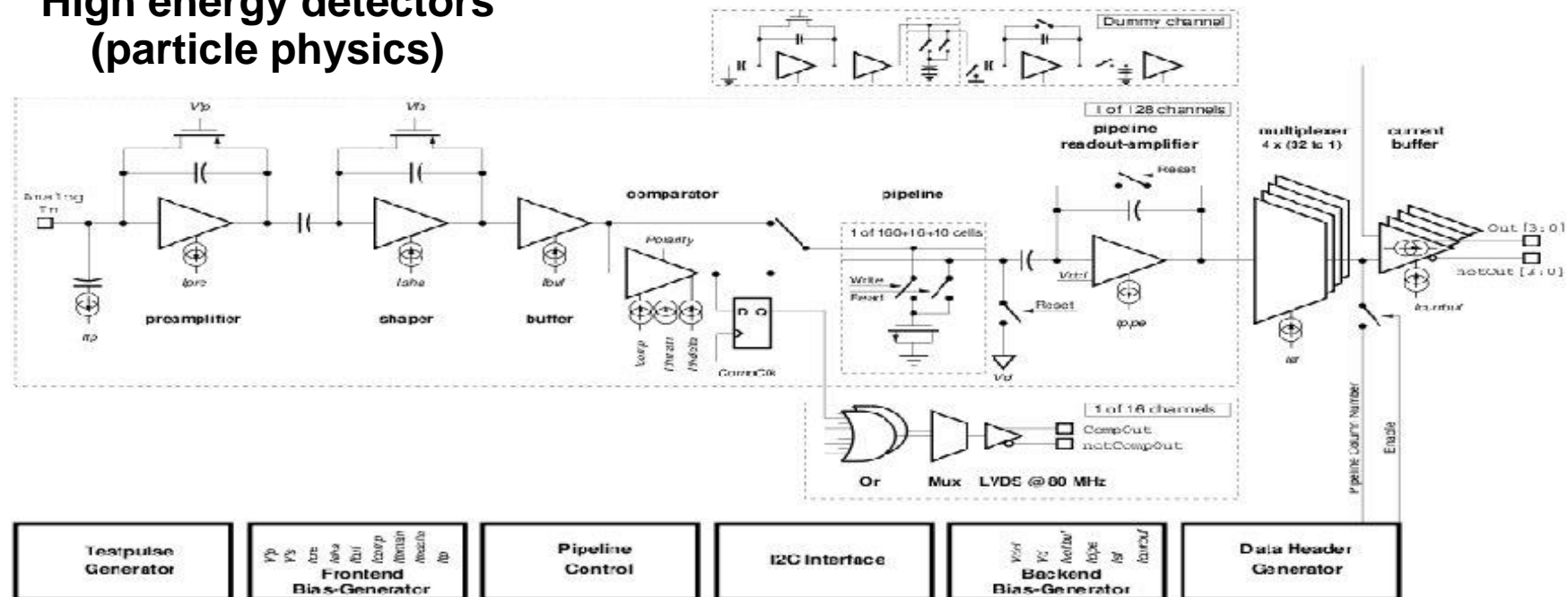
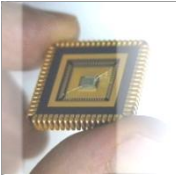


Figure 1: Schematic block diagram of the *Beetle* readout chip.



1- Technology analysis and selection (130nm IBM, 65nm TSMC)

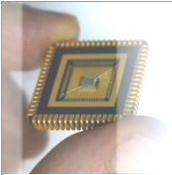
- Intrinsic transistor gain
- Noise spectral density

Chosen technology: TSMC 65nm

2- Functional models of an entire channel

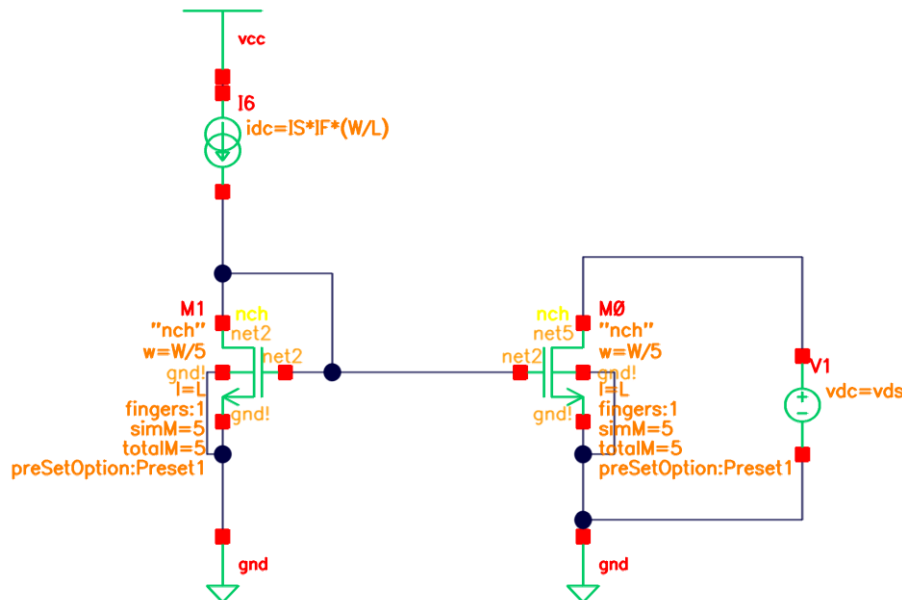
3- Design of the LNA / preamplifier

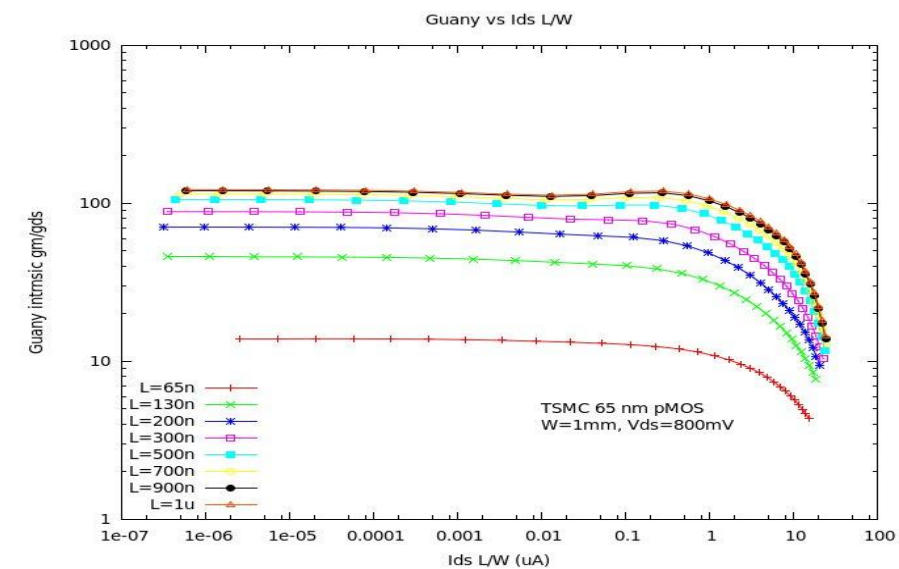
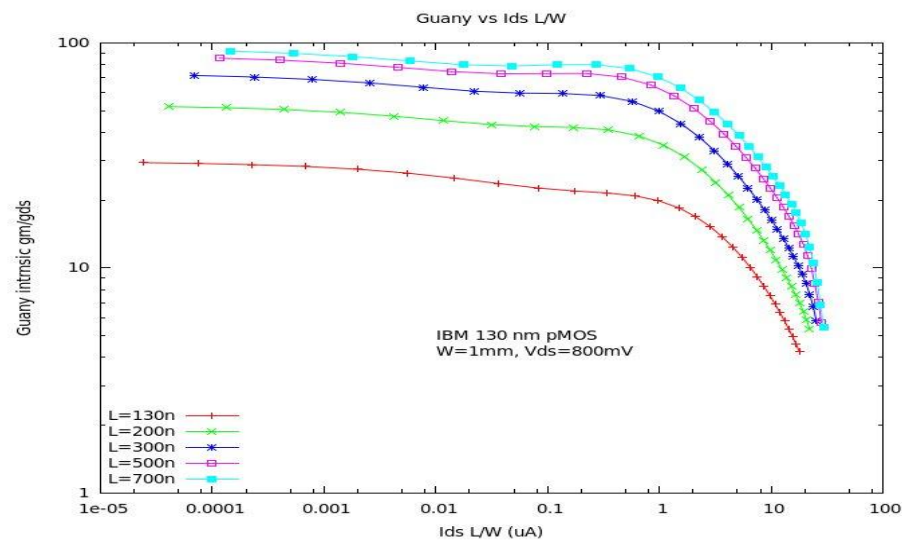
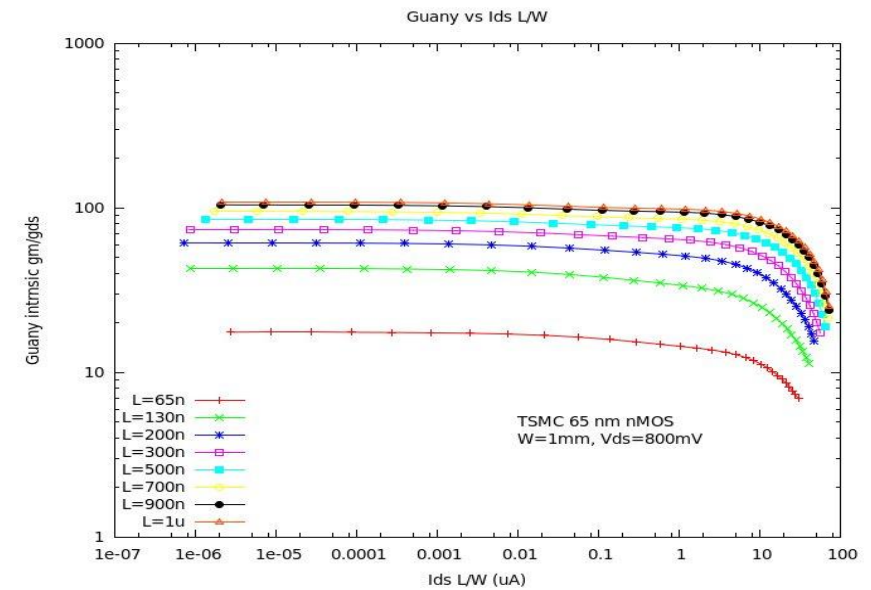
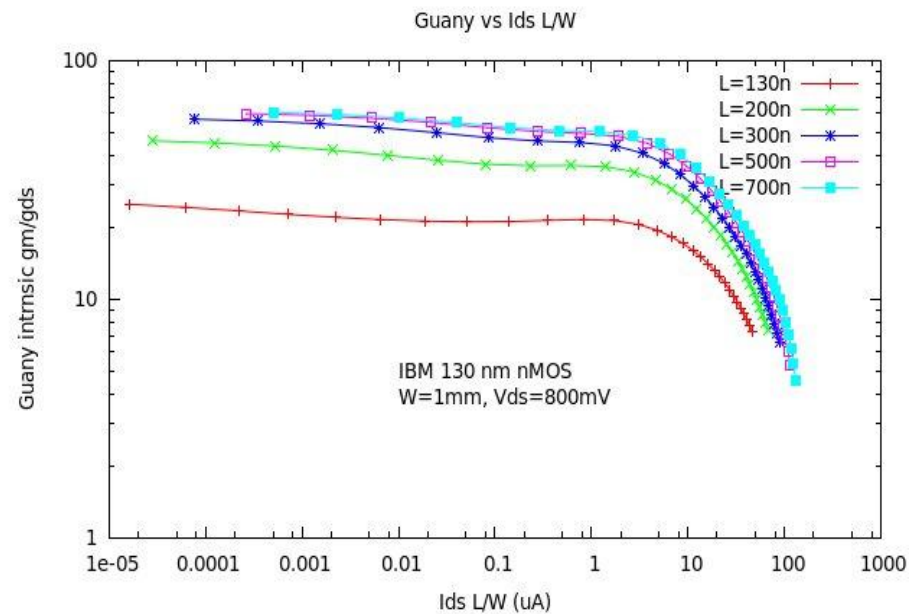
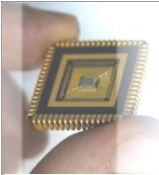
- Ideal amplifier with a pole and limited output
 - Amplifier specifications
- Chosen amplifier: Folded cascode
- Noise analysis
 - Input transistor size and bias

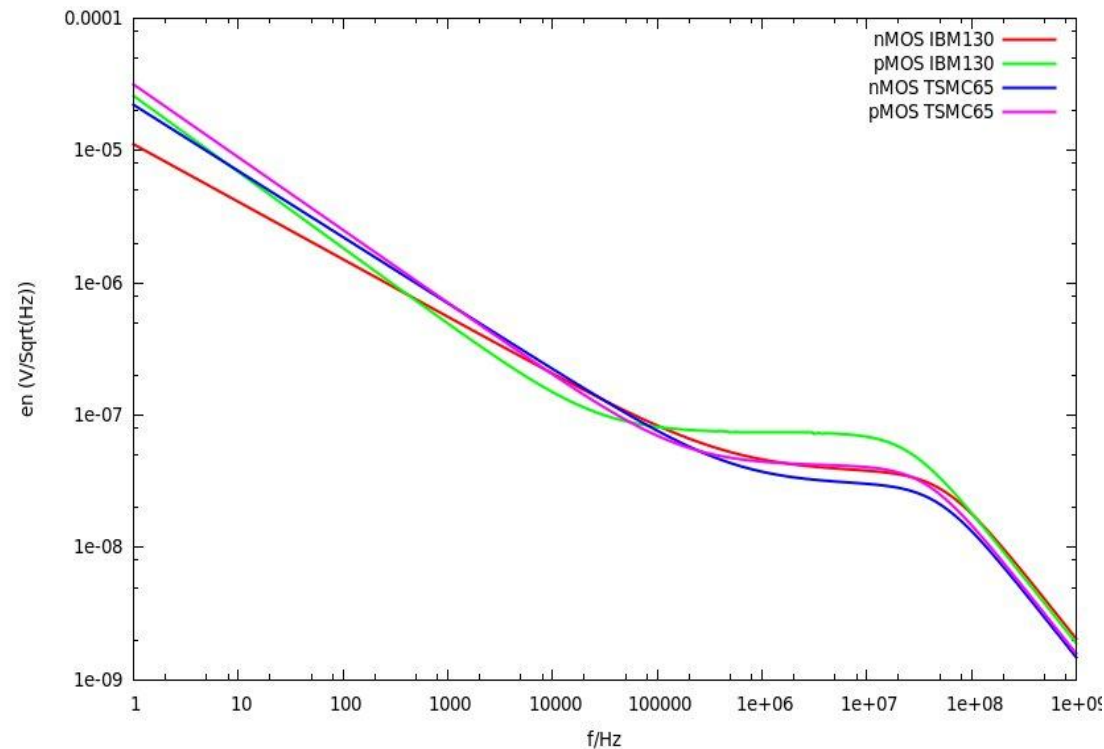
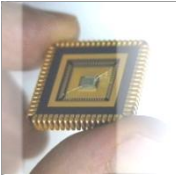


Intrinsic gain analysis:

- The DUT is biased (current mirror configuration) with an inversion factor IF and a fixed V_{ds} .
- A parametric sweep is done for the inversion factor, from w.i. ($10e-7$) to s.i. ($10e2$)
- The intrinsic gain, taken as g_m/g_{ds} is plotted against $I_{ds} \cdot L/W$.
- The procedure is repeated for different L .

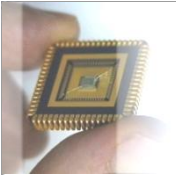






* Graphic obtained with Cadence simulations (BSIM4 model).

TSMC: Higher flicker noise
IBM: Higher thermal noise



TSMC 65nm

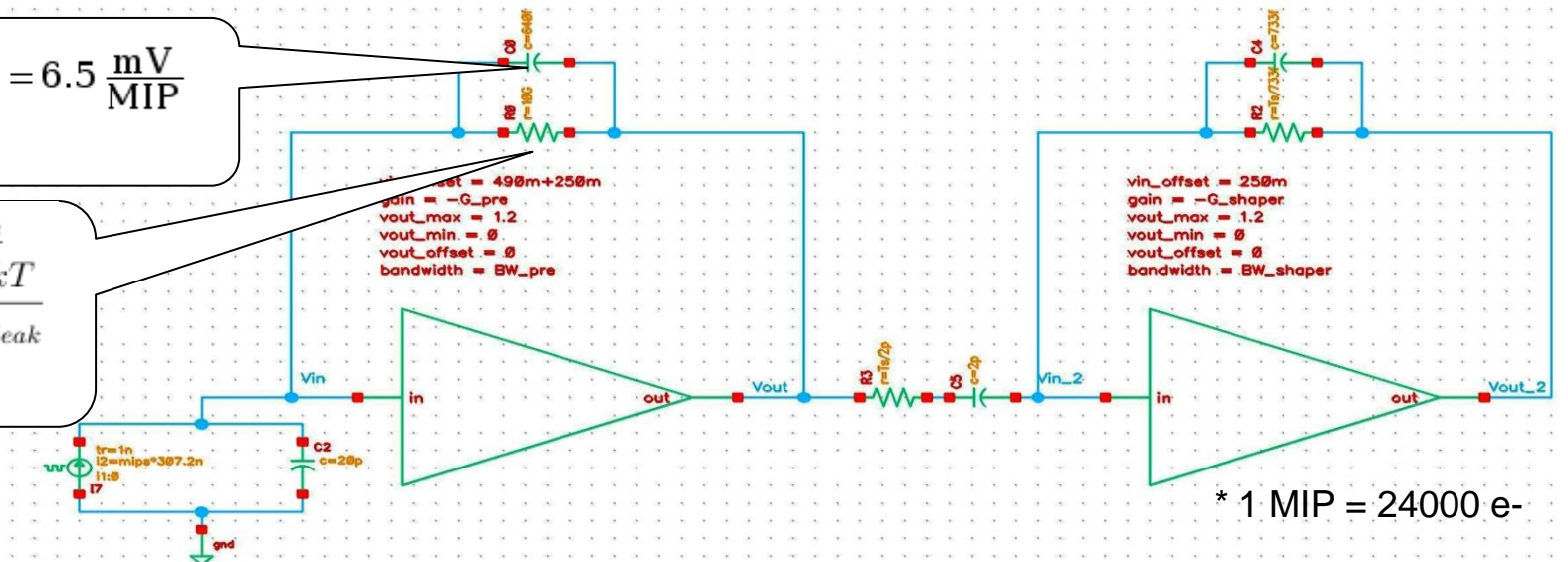
- Higher intrinsic gain
- Similar noise compared to IBM
- Fits more electronics



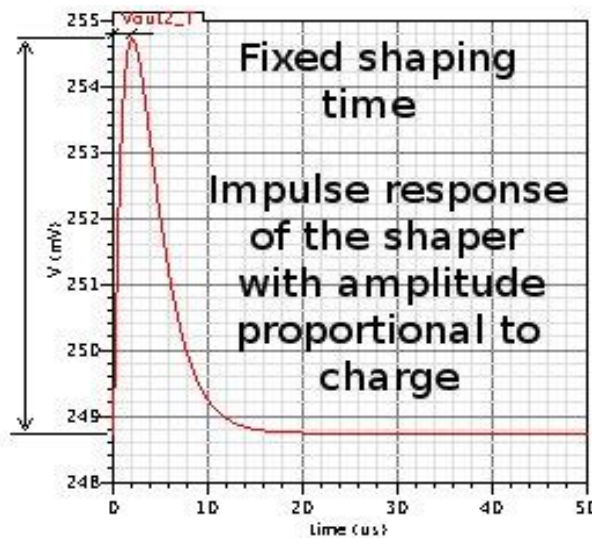
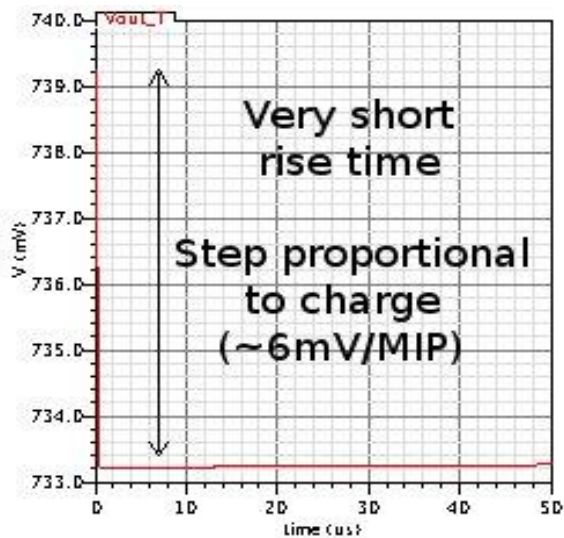
Functional model: Preamplifier + Shaper

$$G = \frac{1}{C_f} = 6.5 \frac{\text{mV}}{\text{MIP}}$$

$$R > \frac{\text{noise}}{2kT}$$



* 1 MIP = 24000 e-

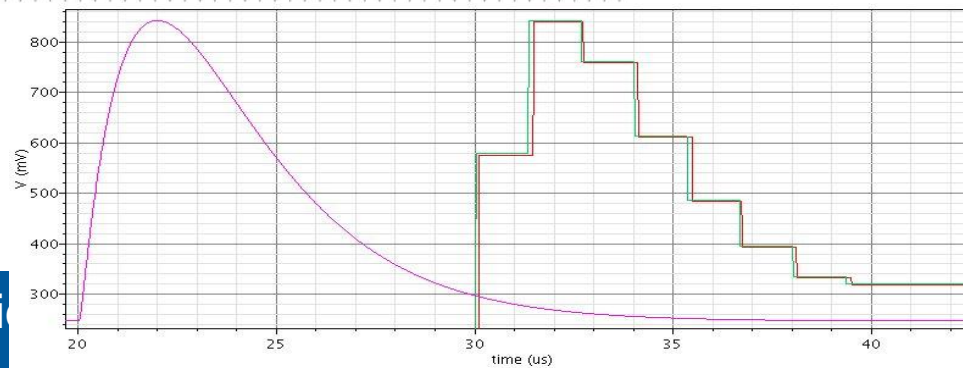
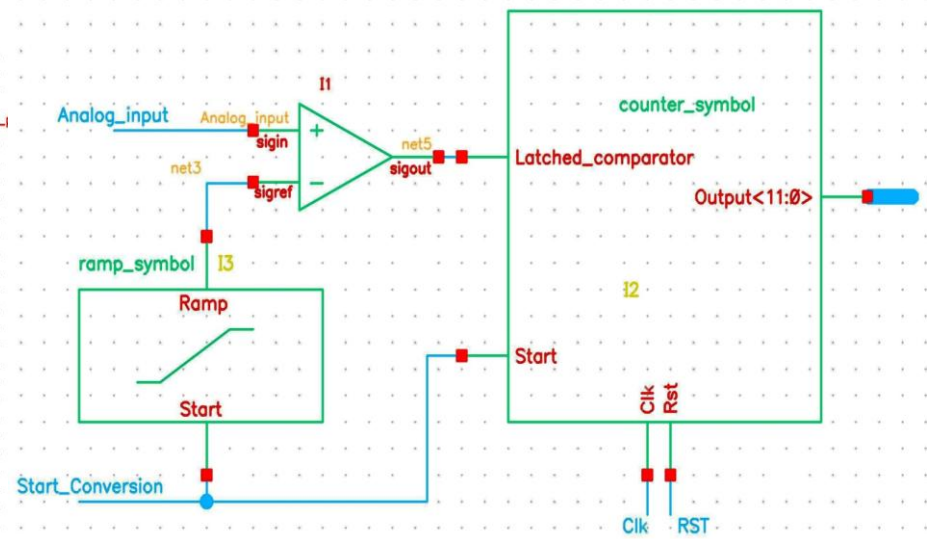
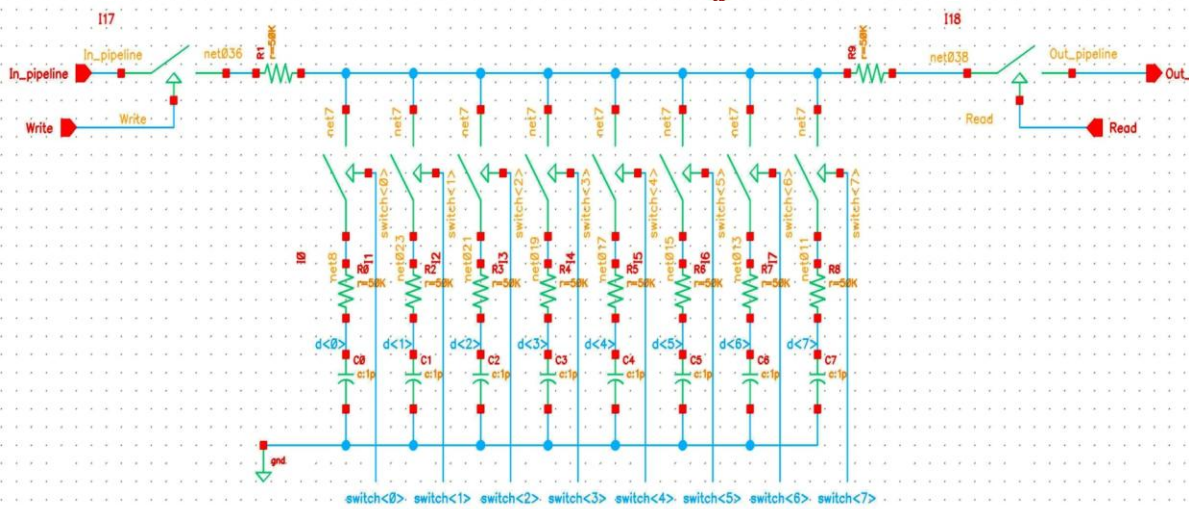
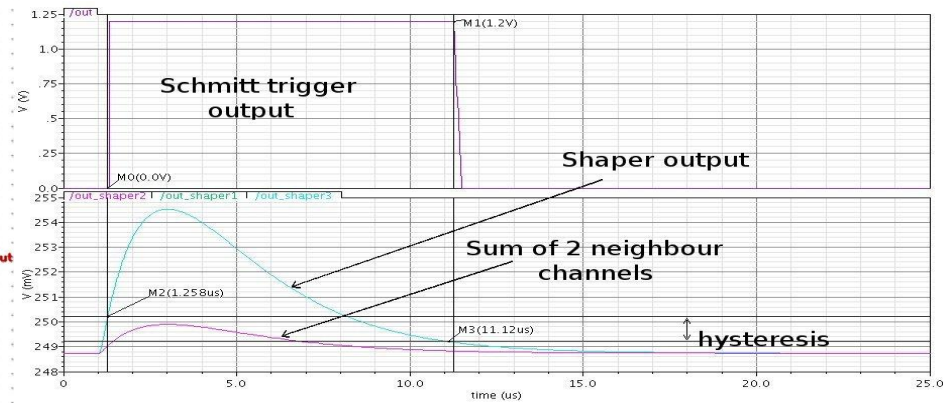
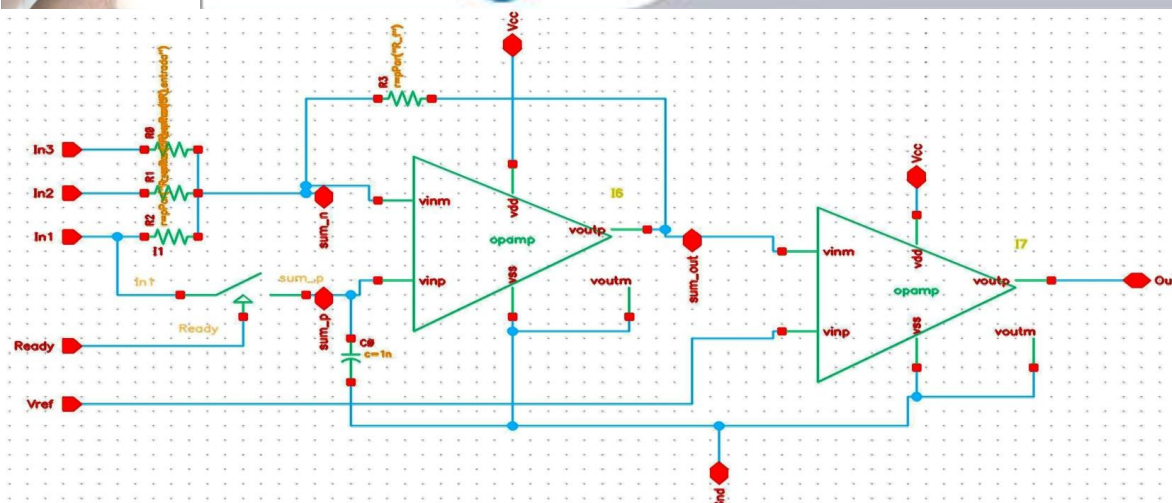


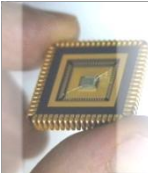
This functional model provides the minimum requirements.
Front-end amplifier:

Minimum gain:
60dB
Minimum BW @ 60dB
~ 100kHz



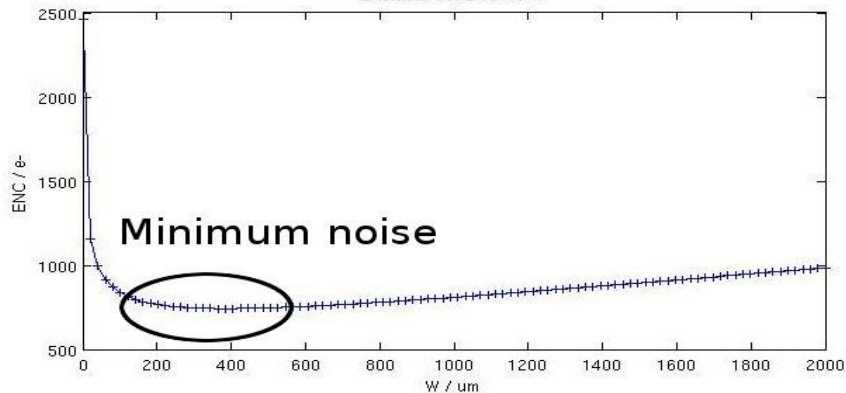
Functional model: Sparsifier + Comparator, analog sampler,
Wilkinson ADC (single ramp)





Optimum width for a given L and I_{ds}

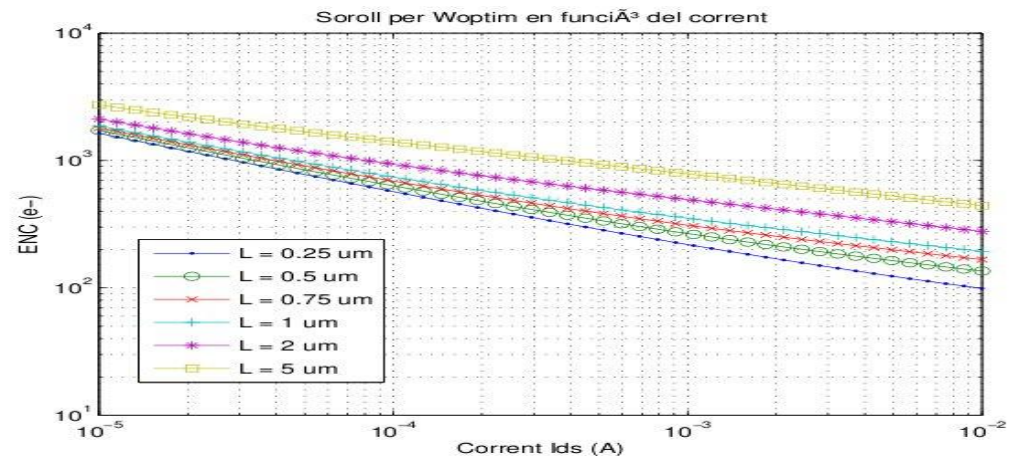
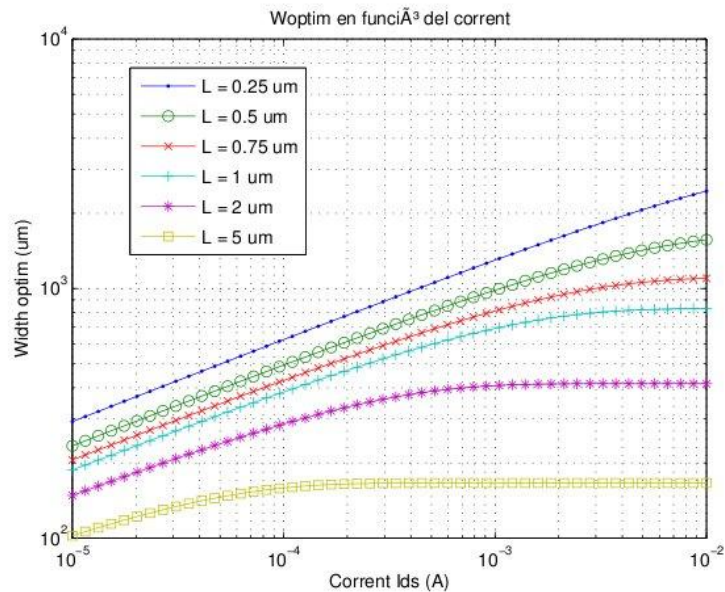
Evolució del ENC vs W



Característiques de soroll per diferents L i I_{ds}

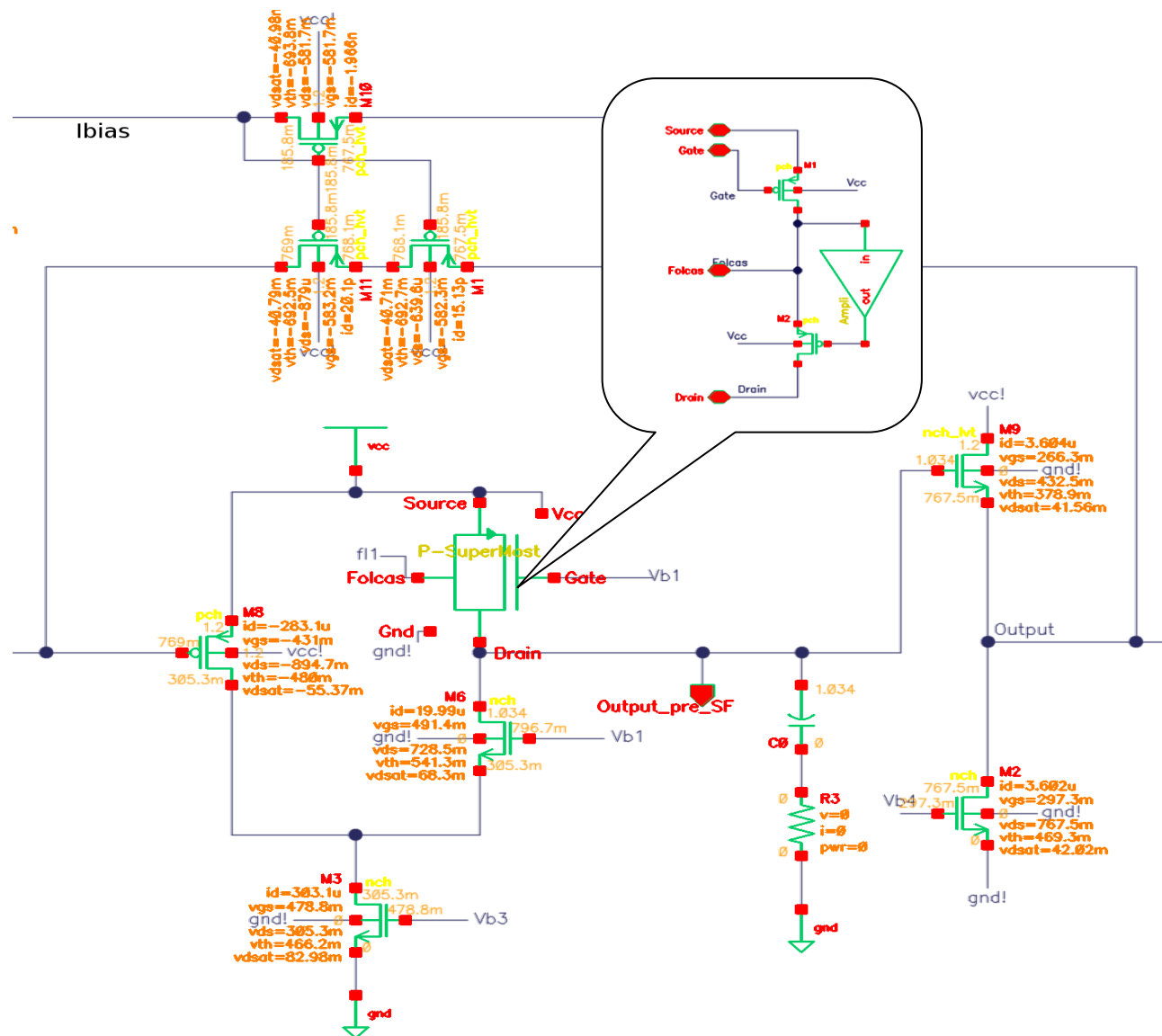
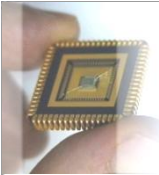
L	I_{ds}	a	b	ENC 20pF	W_{optima}	Consum	IF
0.25 μm	100 μA	47e ⁻	26.2e ⁻	570e ⁻	624 μm	120 μW	0.27
0.25 μm	200 μA	40e ⁻	19.1e ⁻	422e ⁻	781 μm	240 μW	0.42
0.25 μm	300 μA	37e ⁻	15.9e ⁻	355e ⁻	890 μm	360 μW	0.56
0.25 μm	500 μA	34e ⁻	12.7e ⁻	288e ⁻	1046 μm	600 μW	0.79
0.50 μm	100 μA	71e ⁻	28.1e ⁻	633e ⁻	493 μm	120 μW	0.70
0.50 μm	200 μA	63e ⁻	20.8e ⁻	479e ⁻	613 μm	240 μW	1.12
0.50 μm	300 μA	59e ⁻	17.6e ⁻	410e ⁻	694 μm	360 μW	1.49
0.50 μm	500 μA	54e ⁻	14.3e ⁻	340e ⁻	808 μm	600 μW	2.13
0.75 μm	100 μA	94e ⁻	29.8e ⁻	689e ⁻	428 μm	120 μW	1.25
0.75 μm	200 μA	84e ⁻	22.4e ⁻	532e ⁻	528 μm	240 μW	2.02
0.75 μm	300 μA	79e ⁻	19.1e ⁻	460e ⁻	594 μm	360 μW	2.70
0.75 μm	500 μA	74e ⁻	15.7e ⁻	387e ⁻	683 μm	600 μW	3.90
1.00 μm	100 μA	115e ⁻	31.4e ⁻	743e ⁻	385 μm	120 μW	1.89
1.00 μm	200 μA	104e ⁻	23.8e ⁻	581e ⁻	470 μm	240 μW	3.10
1.00 μm	300 μA	98e ⁻	20.4e ⁻	507e ⁻	525 μm	360 μW	4.16
1.00 μm	500 μA	92e ⁻	17.0e ⁻	432e ⁻	596 μm	600 μW	6.11

ENC ~ a + b·Cd



$$ENC = \sqrt{\frac{2}{3} kT \frac{1}{g_m} 1.57 \frac{C_t^2 e^2}{\pi q^2 \tau} + \frac{K_f}{C_{ox}^2 WL} \frac{C_t^2 e^2}{2q^2} + I_{leak} 1.57 \frac{e^2 \tau}{2\pi q} + \frac{kT}{R} 1.57 \frac{e^2 \tau}{\pi q^2}}$$

Hans-Günther Moser, "Silicon detector systems in high energy physics", 2009



Power supply:
1.2V

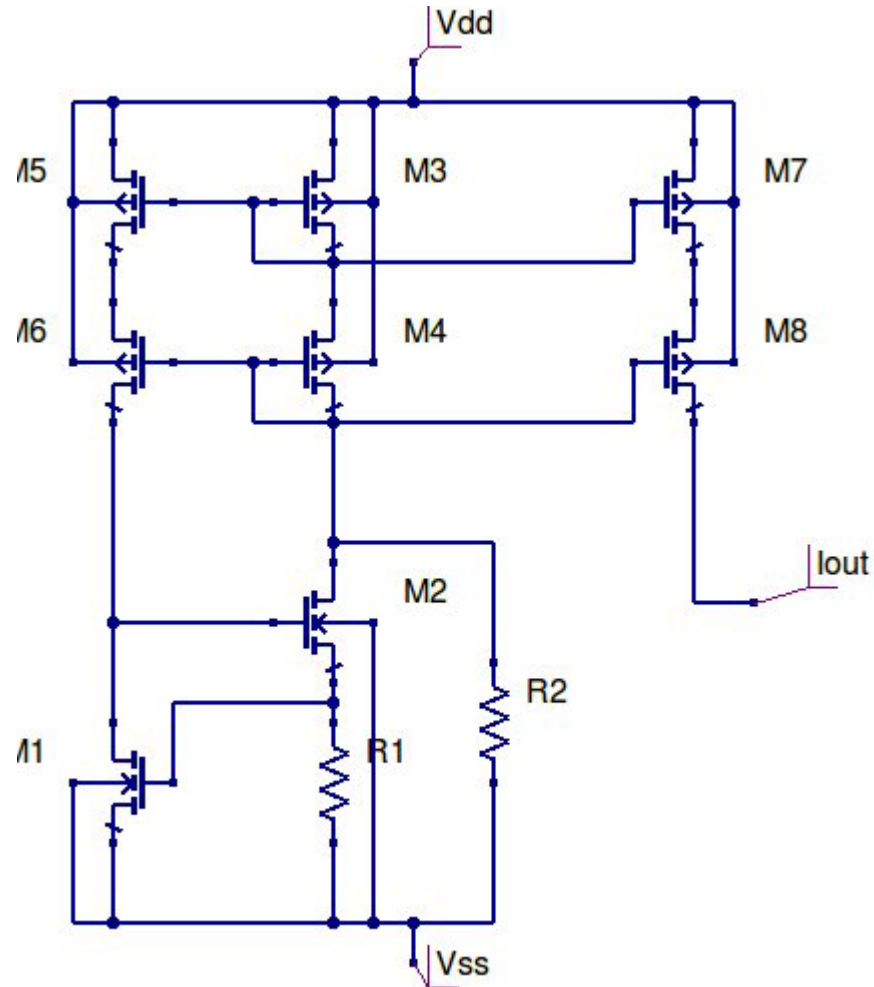
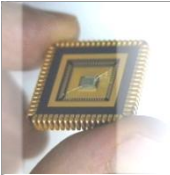
Power consumption:
< 380 μ W

Noise @ 2 μ s shaping time:
A ~ 35,7 e-
B ~ 16,5 e-/pF
[< 400 e- (20pF)]

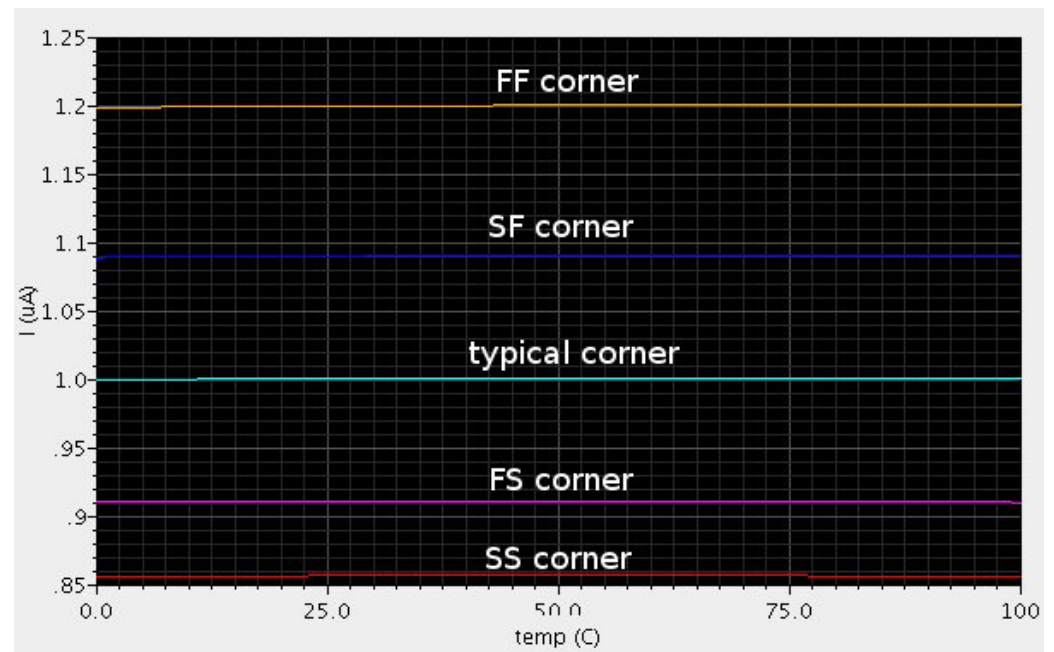
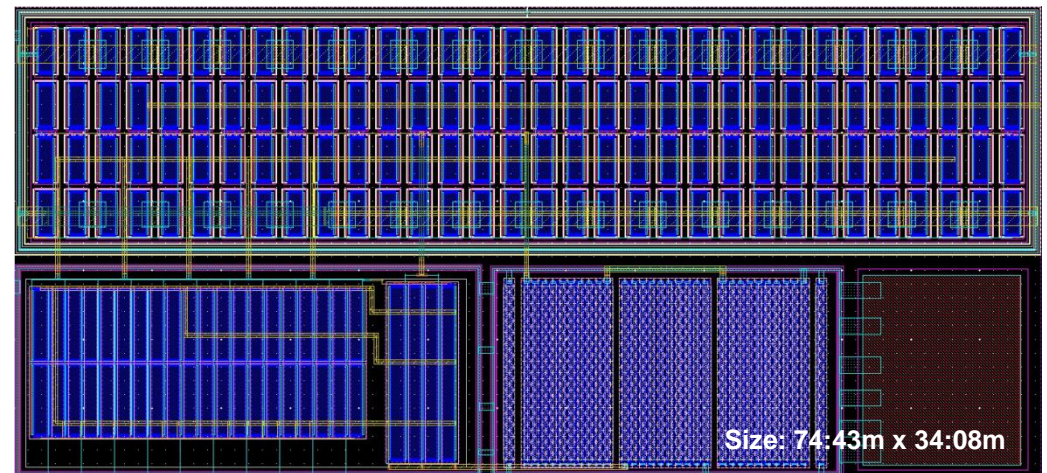
Full scale:
100 MIP

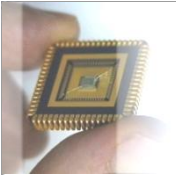
Charge gain:
~ 6.5 mV/MIP

Amplifier:
Gain ~ 69 dB
3dB-BW: ~ 55kHz
PM ~ 66°
* 1 MIP = 24000 e-



$I=1\mu A$, $TC < 30\text{ppm}$ [0:100°C]
 $P=6\mu W$





- **Design of 1 channel:**

- Shaper and sparsifier amplifiers
- Comparator
- Analog pipeline
- ADC
- Biasing DACs
- Digital electronics

- **Multichannel design**

- **Look for interest in other groups for the design to accelerate the design**
- **Obtain more specifications: sensor characteristics, pitch, ..., readout requirements (for example number of pipelines required)**
- **Find budget to prototype**