Bonn / CPPM plans for 3D integration

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ATLAS Pixel Detector Collaboration

Bonn / CPPM project

- **Goal**: Interconnection of the ATLAS FE-I4 chip to sensors using bump bonding and post-processing TSVs from IZM.

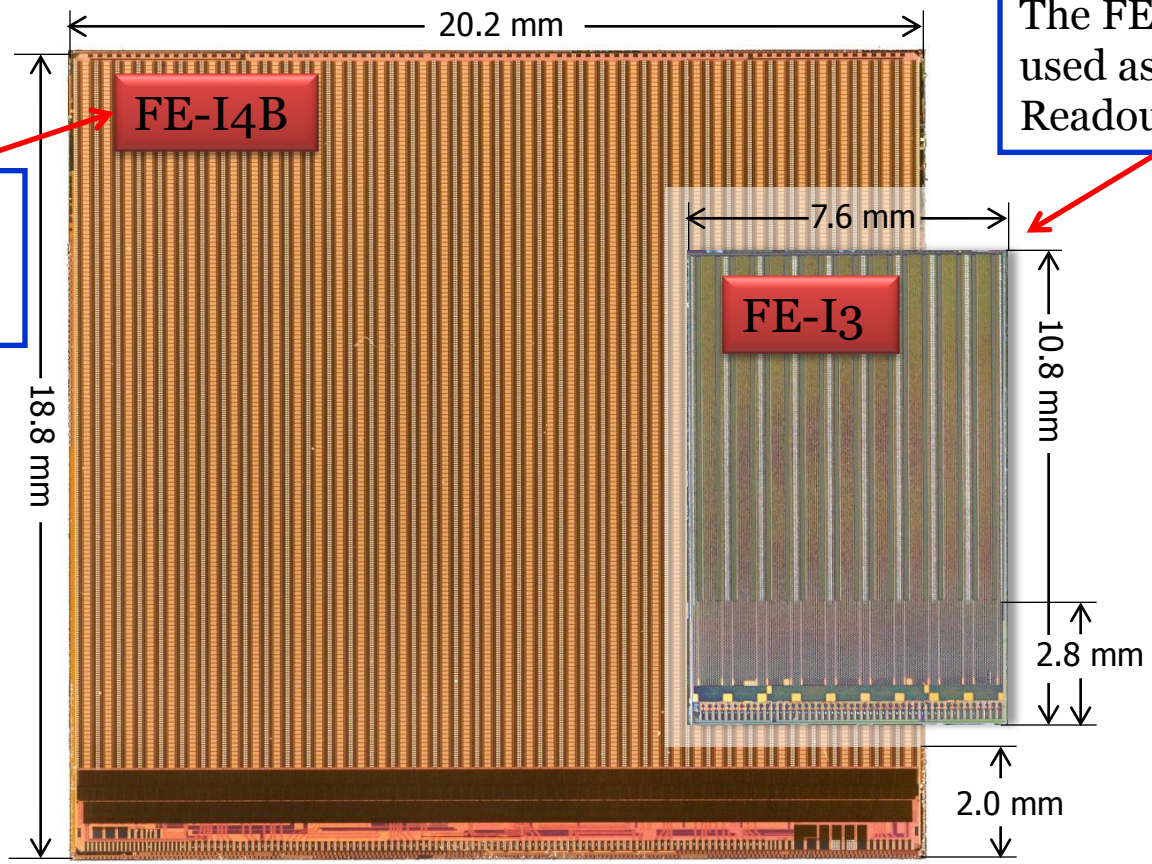
- **Context**: Material reduction, new module concepts, new technologies for High Luminosity LHC upgrade.

- **1st goal at short time-scale**: Demonstrate two-side access (front and back) to a bump-bonded sensor/FE stack, using the FE-I4B.

FE-I4B

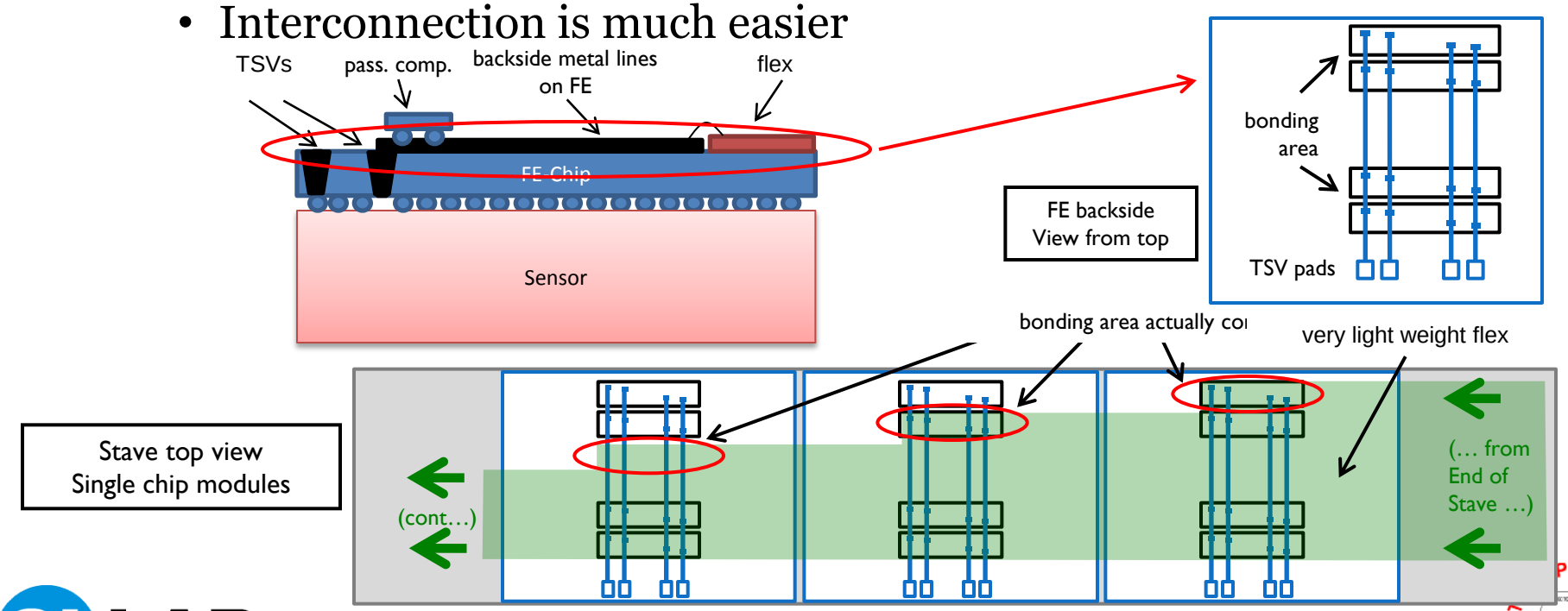
The new FE-I4B for ATLAS IBL project and HL LHC upgrade

The FE-I3 currently used as ATLAS pixel Readout Chip



Module concept with TSV: Sketch

- TSVs + backside metallization → Will allow the use of FE's backside for routing
  - Direct connection of service lines or flex on FE backside
    - Less material: no need for wings, module flex, connectors (IBL as an example: gain **~0.13%X0)**
    - Interconnection is much easier



Current project with TSV

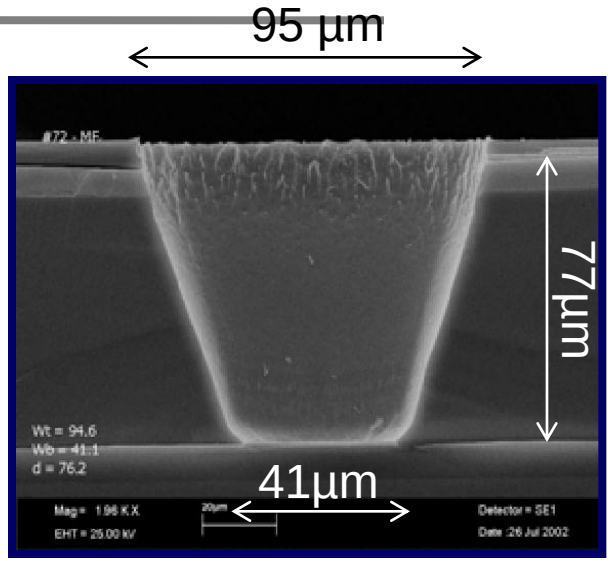
- Long term relationship between Ubonn and IZM Berlin.
  - IZM main bump bonding ATLAS pixel partner.
  - Many developments for future module addressed with IZM: Usage of different sensors, thin IC modules, low cost program…

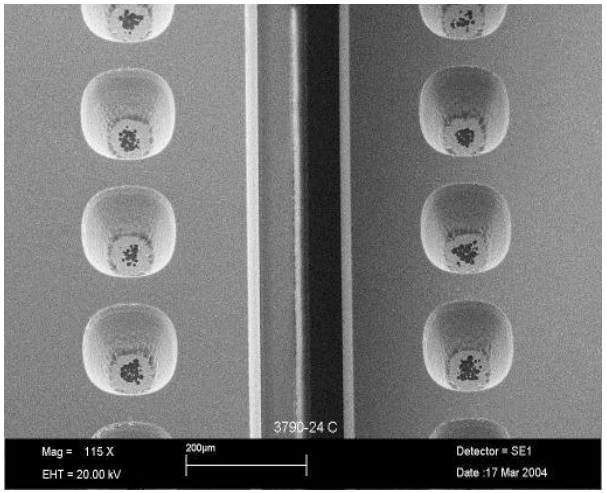
- Started a via-last TSV development with IZM 3 years ago.
  - FE-I2/I3 readout electronics.
  - Tapered side wall / Straight side wall TSVs.

  (both used successfully, tapered side wall TSVs a faster process, better suited to our needs)
  - "Integrated" TSV / Bump Bonding process in-house at IZM.
  - Profits from ultra thin flip chipping R&D (developed for FE-I4 in ATLAS IBL project).

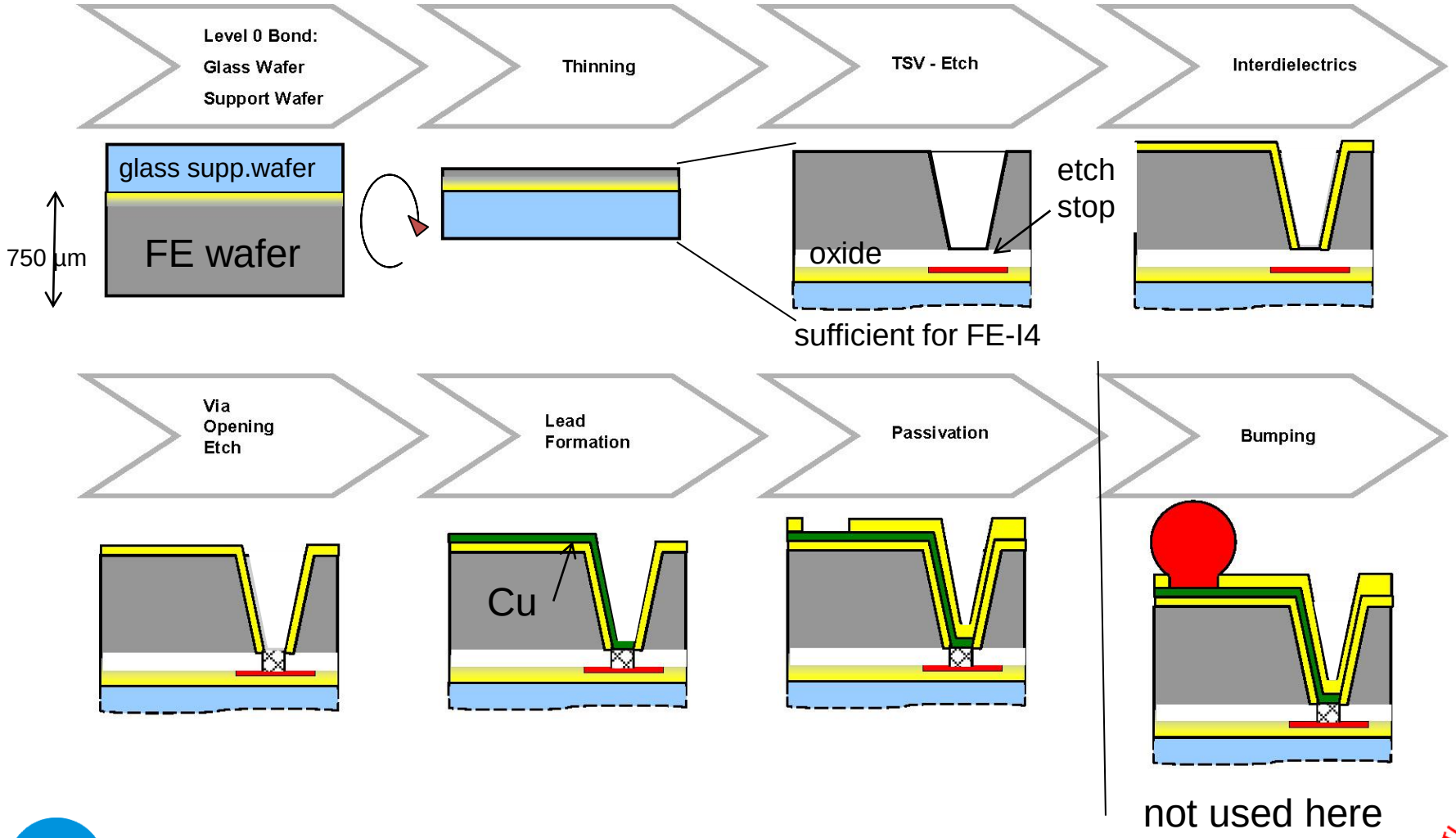
Tapered Side Walls TSV Etching

- **Tapered Side Wall TSV** is a fast process
  - Vias are etched in one step and oxide is deposited afterwards.
- Tapered walls
  - Side wall angle 72°
  - Via diameter on the bottom is 41µm
  - Via diameter on the top is 95µm
  - Si thickness 77µm (in this example)
    - with pad pitch of 150 µm (FE-I2) → maximum die thickness is 100µm



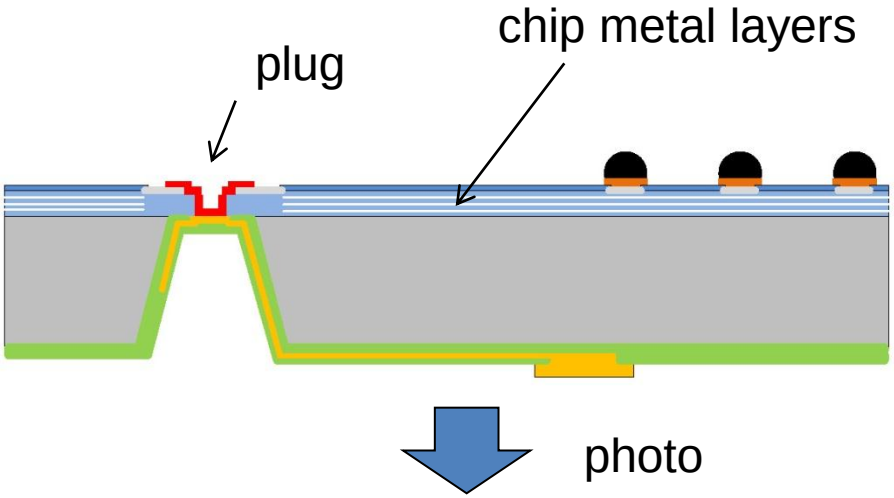


TSV: Main process flow

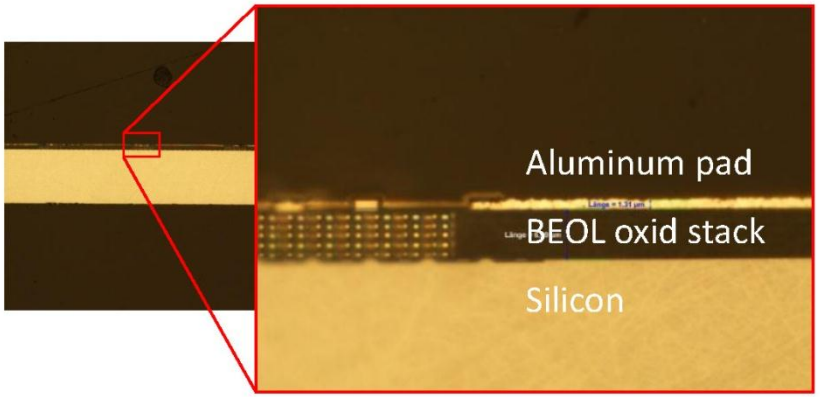


TSV prototypes with FE-I2/3

- **Frontside processing**
  - Cu pad to bond pad interconnect (plug)
  - Bump deposition
  - Dicing

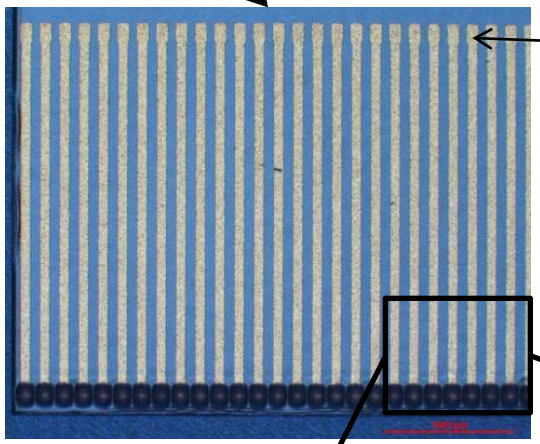


- **Backside processing**
  - Thinning to 90µm
  - Silicon Via etching
  - Passivation
  - Re-Distribution Layer (RDL)

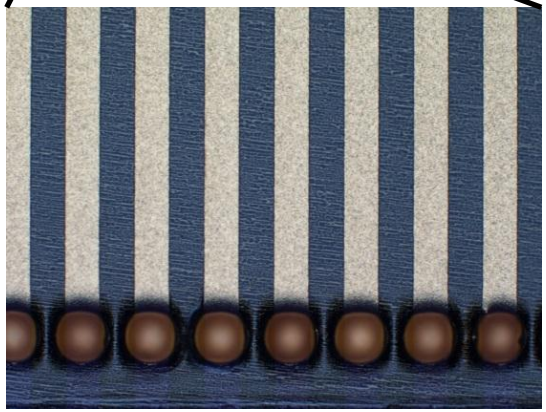


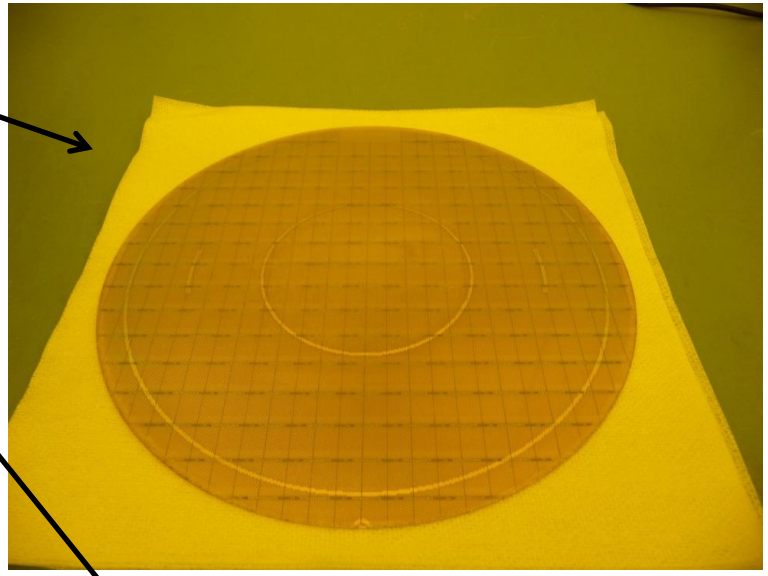
Backside interconnection

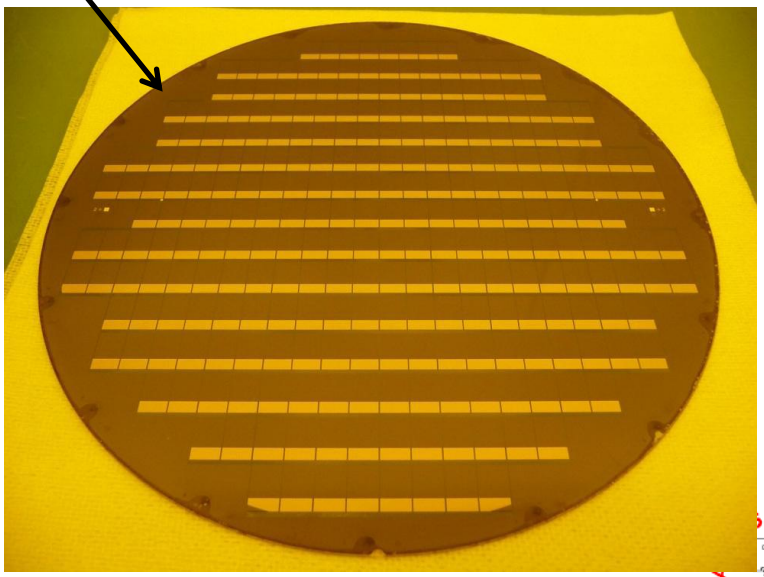
- Frontside on temporary carrier wafer
- Backside with TSV interconnection (RDL)
- Backside RDL on FE-chip



wire bond pads







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Tapered TSVs processing on ATLAS FE-I2 batch

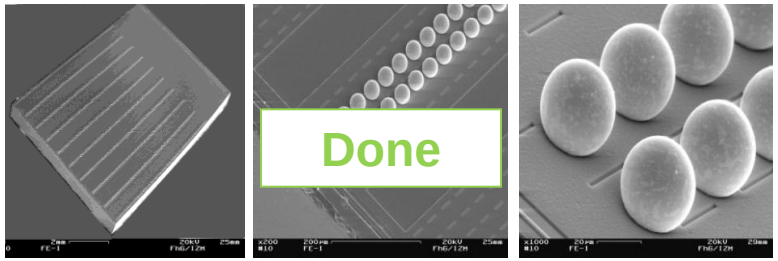
Front side processing

Al pad opening by wet etching

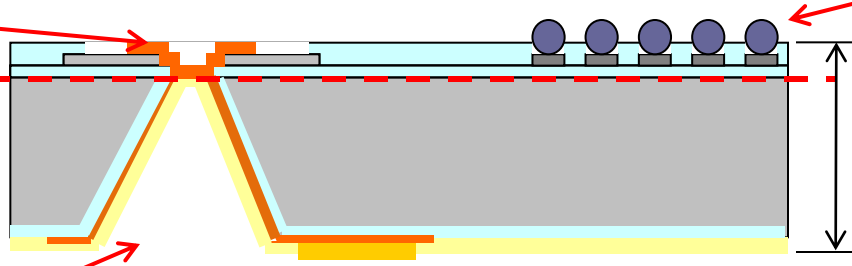
BEOL SiO_2 stack etching

Cu electroplating – interconnection plug to Al pad

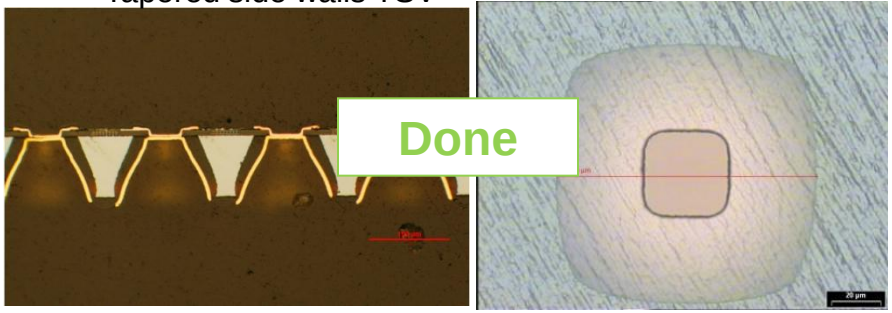
Bump deposition and dicing



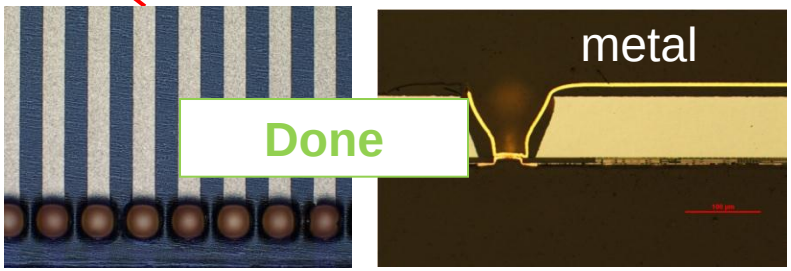
Back side processing



Tapered side walls TSV



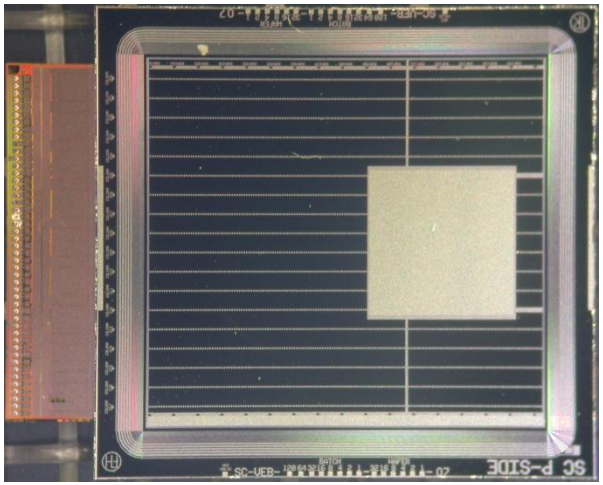
Backside redistribution



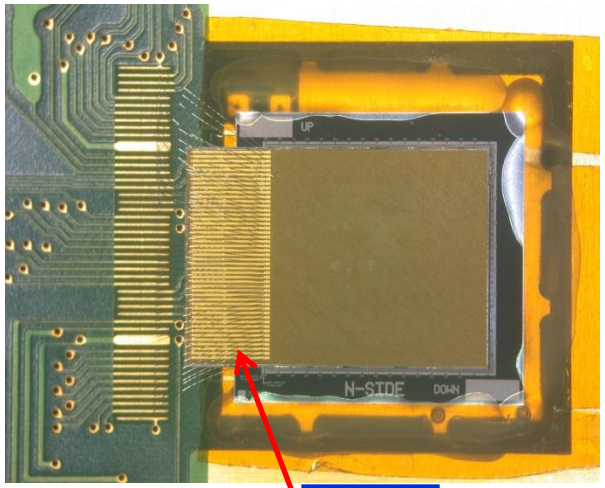
FE-I2 module with TSV

- Received 16 modules:
  - FE-I2 chips, 90µm thick, with tapered TSV and RDL
  - Planar n-in-n sensor
- 2 modules mounted on boards for electrical tests
  - Both modules work fine

Module front side

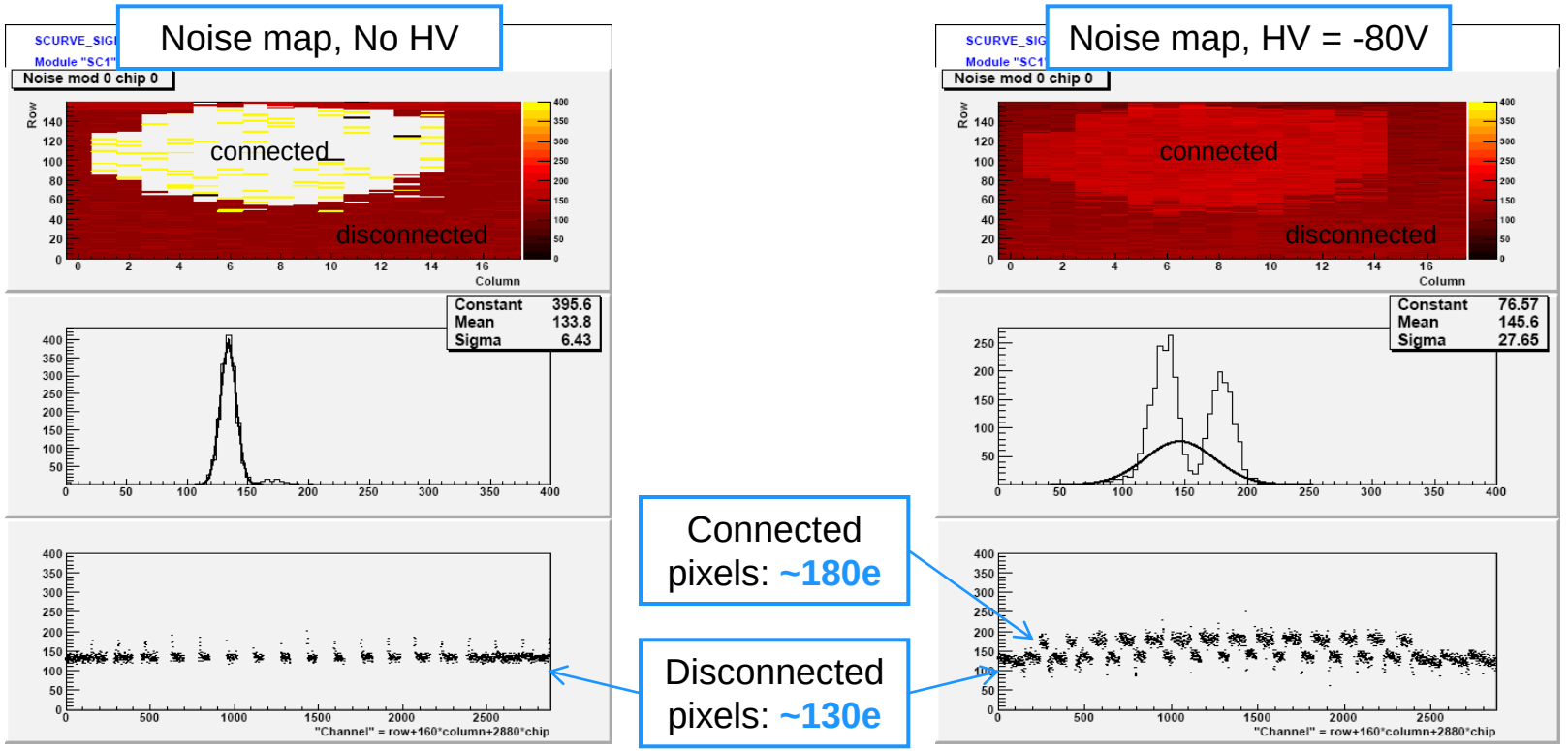


Module on board



Module test using TSVs

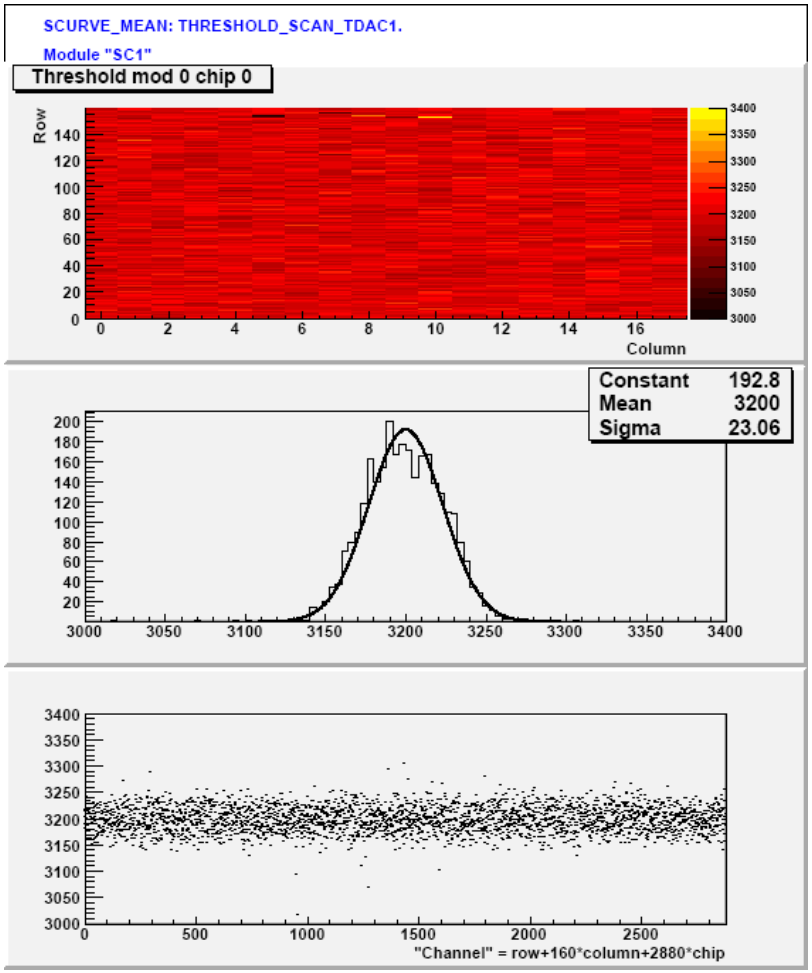
- Used "standard" IC handling method (no handle wafer) → gains time (but of course leads to large area of unconnected bonds).



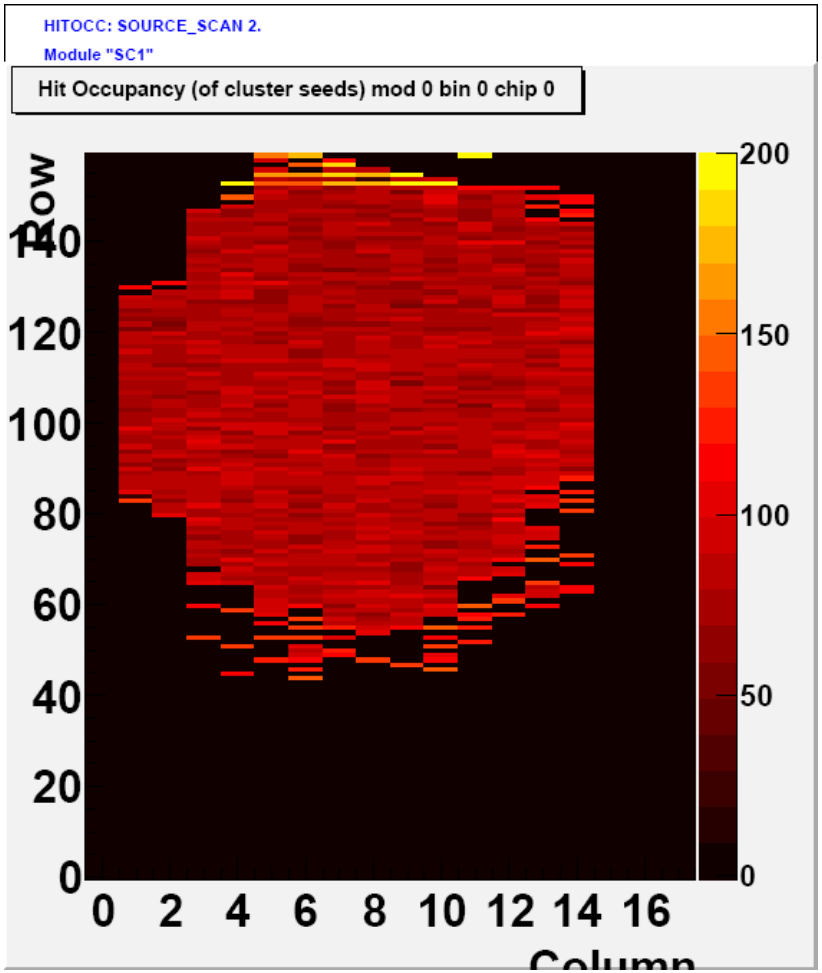
- ENC ~180e-! Module works fine & no indication of extra noise

Source scan with TSV module

Threshold tuning to 3200e

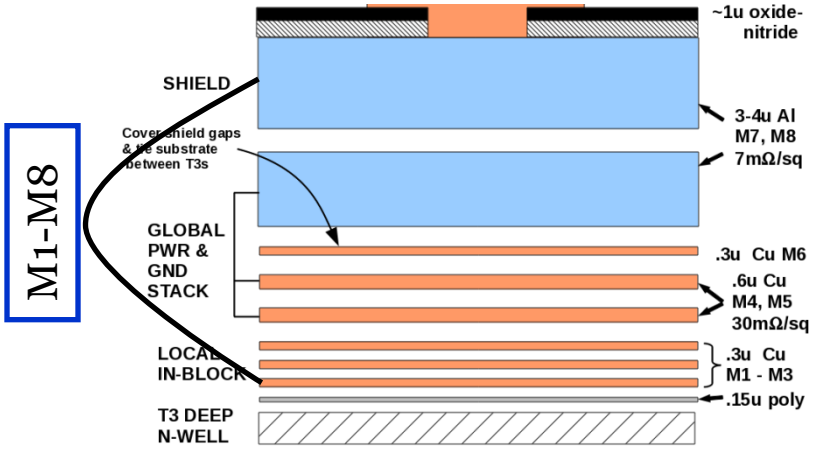


Source scan (Am 241)



Next immediate step: TSV FE-I4A

- Next step: Use FE-I4A IC & same process:
  - 6 times larger than FE-I2/3 but thickness must be 90µm (note IBL chips are 150µm thick): Use thin flip chip method currently used for IBL modules.
  - FE-I4A pads are already tuned for TSV usage (half pad area BEOL only, complete metal stack ➔ No frontside plug needed)



FE-I4 BEOL layer stack

Intermediate goal

- Usage of final version of the FE-I4 IC for IBL, FE-I4B. Tuned for TSV usage + can use the CPPM-developed GDAC to monitor more information (internal voltages, leakage currents, temperature…).

- Assess the potential for TSV of a second vendor (LETI Grenoble, France).

- Test connection to other sensor types (3D silicon, depleted HV CMOS).

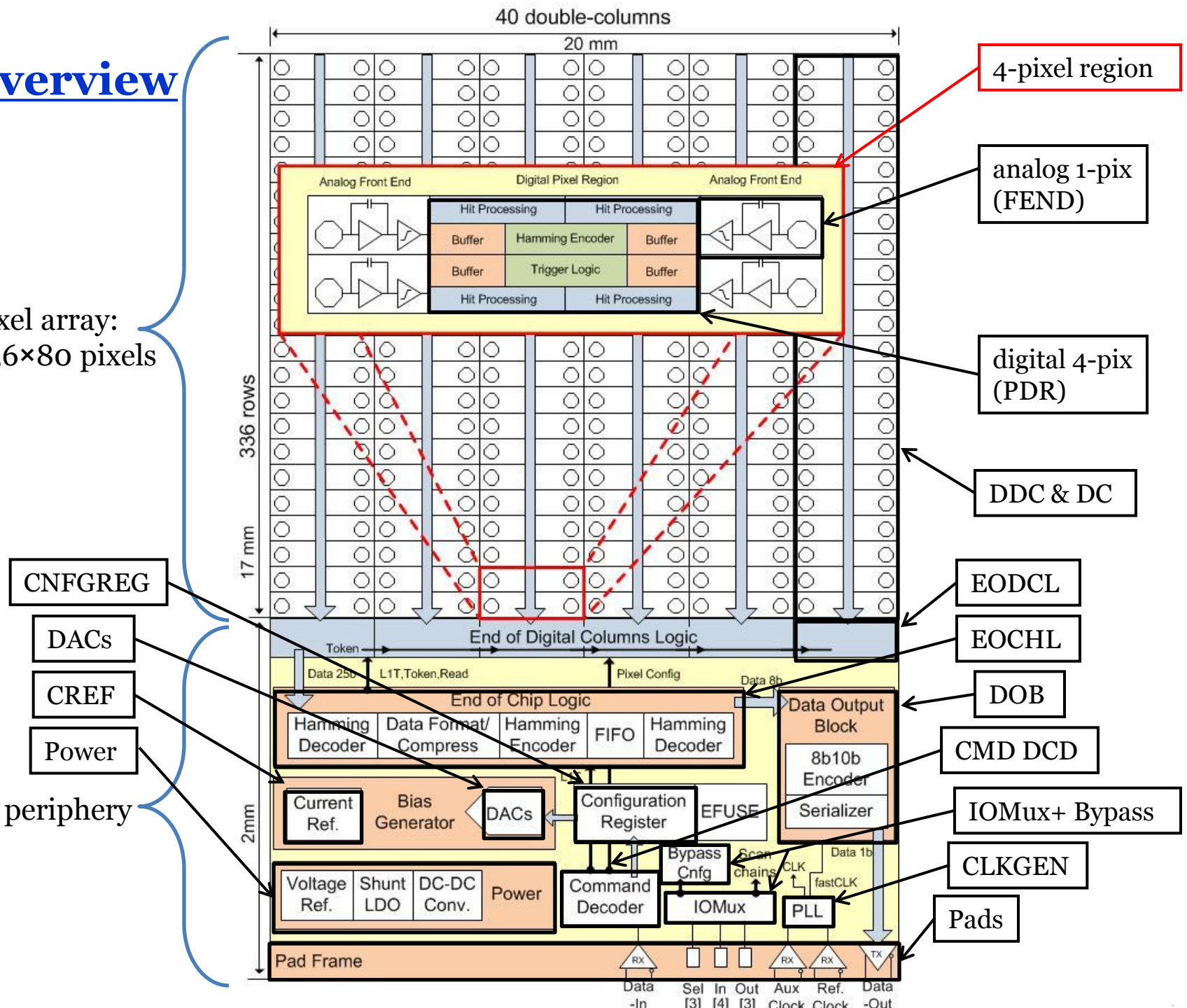
Conclusion

- Successful 1st demonstration of usage of TSV on FE-I2 / I3 ATLAS FE.
  - ICs function well when operated with TSV + backside RDL (equivalent noise, source scan performed).
- A run with FE-I4A will soon start (3 wafers reserved for that). Results expected ~fall 2012.
- TSV on FE-I4B, in-situ IC characterization.
- Developments for IBL and HL-LHC upgrades lead to:
  - **Integrated TSV / Bump-bonding process**.
  - **Handling of large & thin IC**.
- **Goal**: New module concepts using TSV, material reduction, technology exploration for the High Luminosity LHC upgrade.

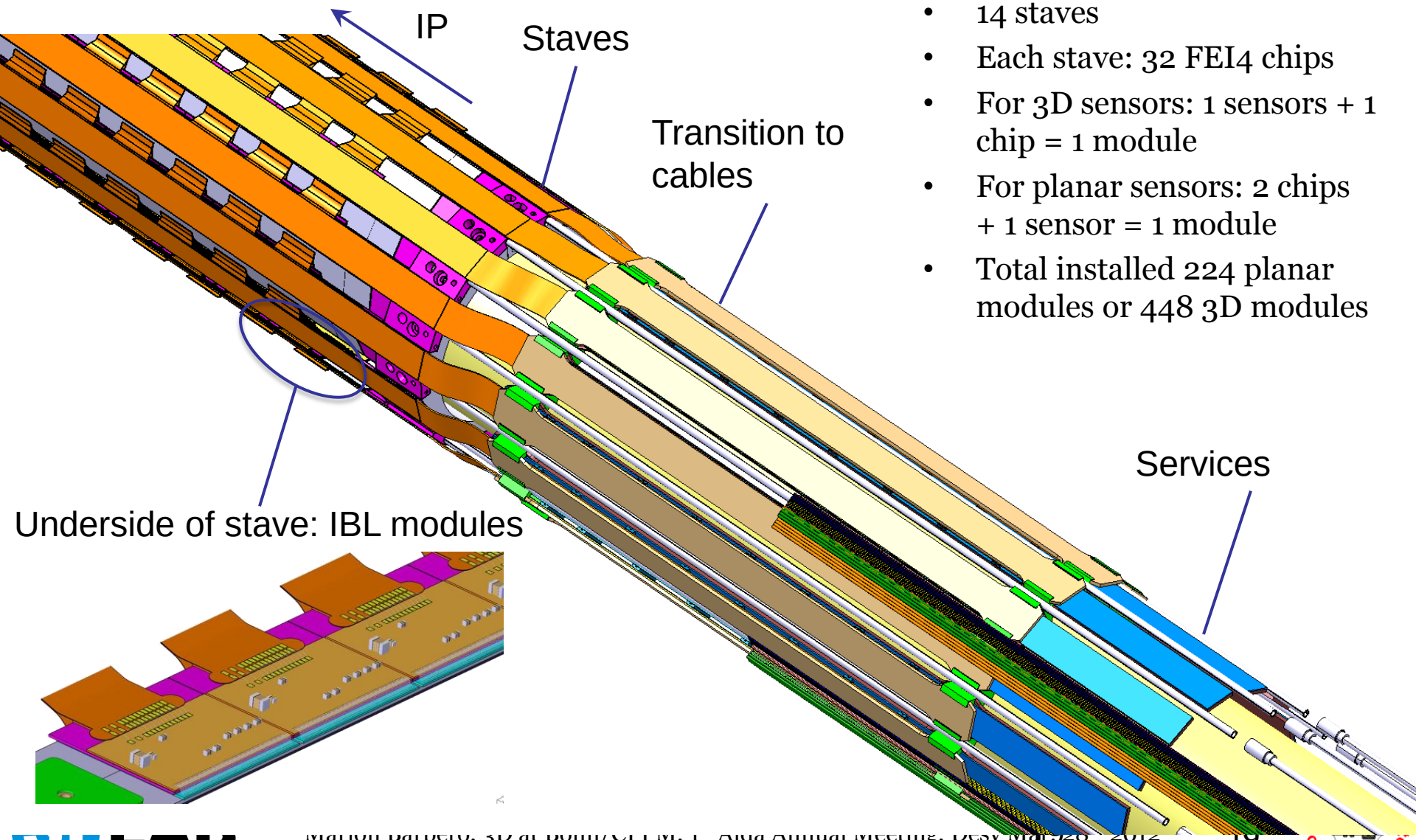
BACKUP

- BACKUP

- **Overview**


40 double-columns
20 mm
4-pixel region
analog 1-pix (FEND)
digital 4-pix (PDR)
DDC & DC
pixel array: 336×80 pixels
336 rows
17 mm
Analog Front End
Digital Pixel Region
Analog Front End
Hit Processing
Hit Processing
Buffer
Hamming Encoder
Buffer
Buffer
Trigger Logic
Buffer
Hit Processing
Hit Processing
CNFGREG
DACs
CREF
Power
periphery
EODCL
EOCHL
DOB
CMD DCD
IOMux+ Bypass
CLKGEN
Pads
End of Digital Columns Logic
Token
Data 25b
L1T,Token,Read
Pixel Config
Data 8b
End of Chip Logic
Hamming Decoder
Data Format/ Compress
Hamming Encoder
FIFO
Hamming Decoder
Data Output Block
8b10b Encoder
Serializer
Current Ref.
Bias Generator
DACs
Configuration Register
EFUSE
2mm
Bypass Cnfg
Scan chains
CLK
Data 1b
fastCLK
Voltage Ref.
Shunt LDO
DC-DC Conv.
Power
Command Decoder
IOMux
PLL
Pad Frame
RX
RX
RX
TX
Data -In
Sel [3]
In [4]
Out [3]
Aux Clock
Ref. Clock
Data -Out

Stave and module arrangement



- 14 staves
- Each stave: 32 FEI4 chips
- For 3D sensors: 1 sensors + 1 chip = 1 module
- For planar sensors: 2 chips + 1 sensor = 1 module
- Total installed 224 planar modules or 448 3D modules