Interconnection of a 3D front-end chip to edgeless/slim-edge and CMOS sensors with advanced techniques

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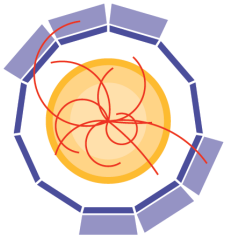


AIDA

1st Annual Meeting
28-30 March 2012, Desy

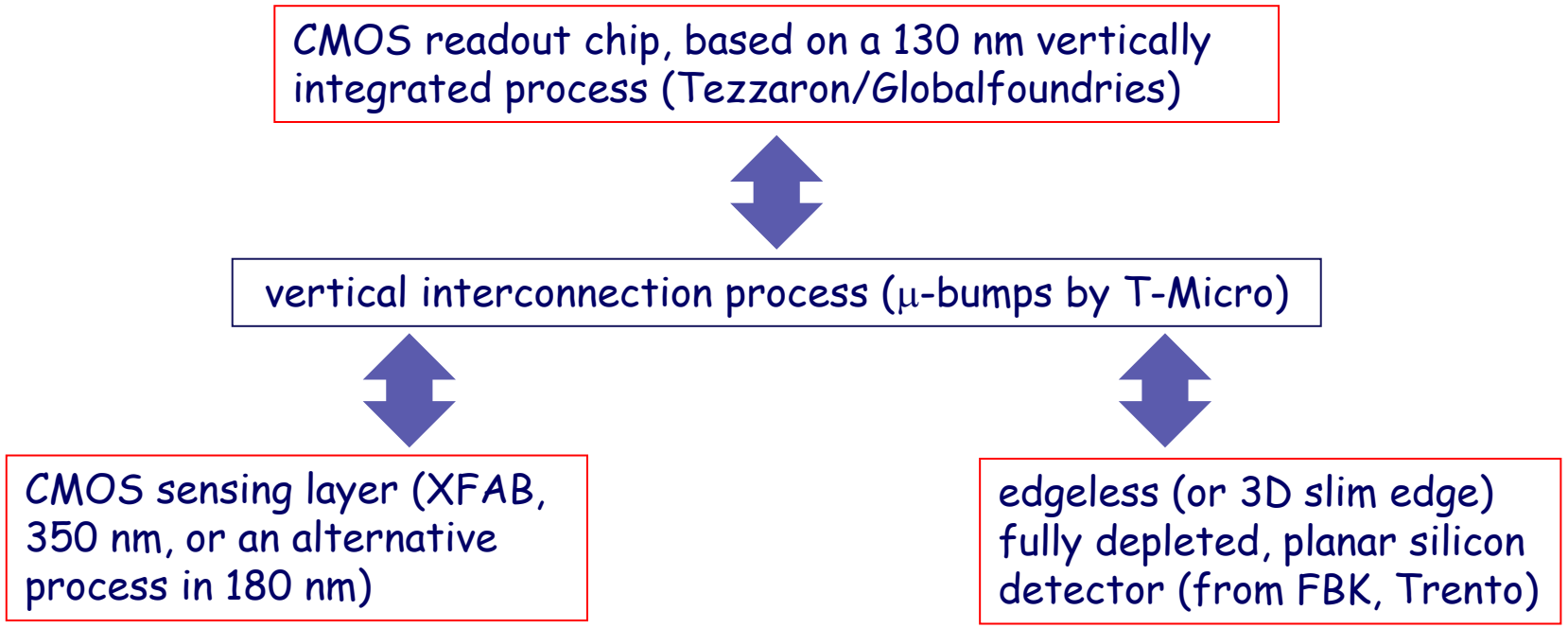
for the IPHC-IRFU / INFN collaboration

OUTLINE

- Sensing layer - CMOS sensor and edgeless/slim edge high resistivity sensors
- Readout chip – homogeneous, dual layer, vertical integration CMOs process
- Readout chip to sensor vertical integration – T-micro μ–bump technology
- Financial structure and timescale of the project

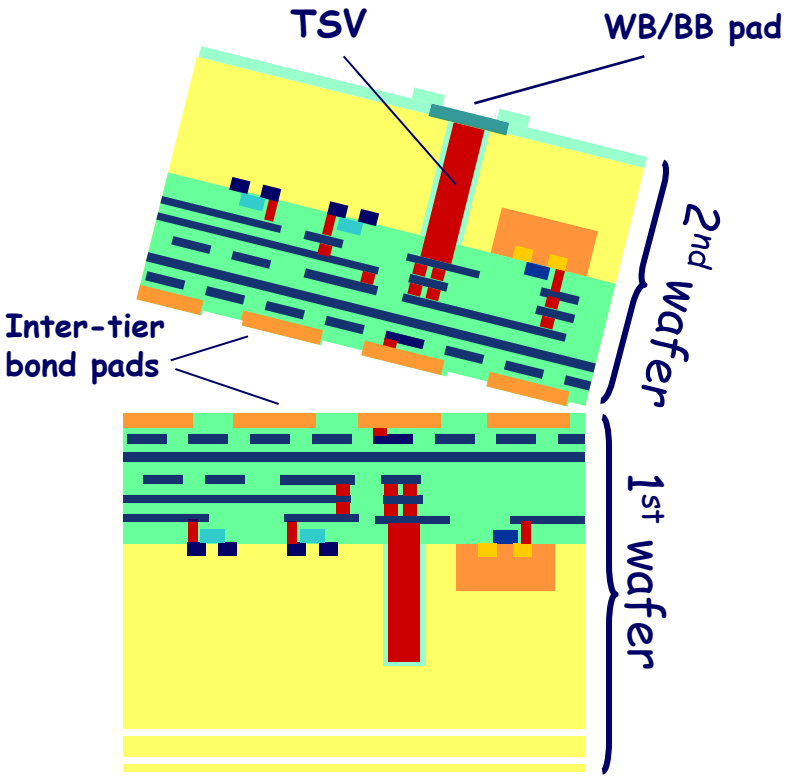
Goal of the project

- **Design and fabrication of a multi-tier pixel sensor resulting from the vertical interconnection of a readout chip and of a sensing layer**



- **The project is to be regarded mainly as R&D, although the proposed device is aimed for applications to experiments at the next generation colliders – SuperB, HL-LHC**

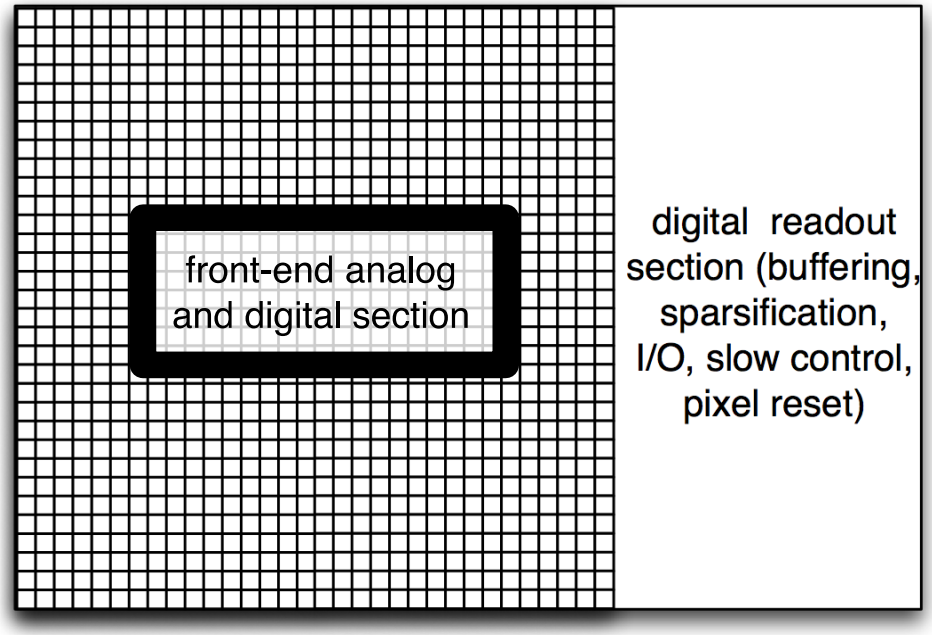
Tezzaron vertical integration (3D) technology



- In wafer-level, three-dimensional processes, multiple strata of planar devices are stacked and interconnected using through silicon vias (TSV)
- 3D processes rely upon the following enabling technologies
  - Fabrication of electrically isolated connections through the silicon substrate (TSV formation)
  - Substrate thinning (below 50 μm)
  - Inter-layer alignment and mechanical/electrical bonding
- Tezzaron Semiconductor technology (via middle approach, vias are made between CMOS and BEOL) can be used to vertically integrate two 130 nm CMOS layers specifically processed by Globalfoundries

- Globalfoundries provides a 130 nm CMOS process with several different options; chosen one features 1 poly, 6 metal layers, 2 top metals, dual gate (core and thick oxide devices, 3.3 V), N- and PMOS with different V_{th}

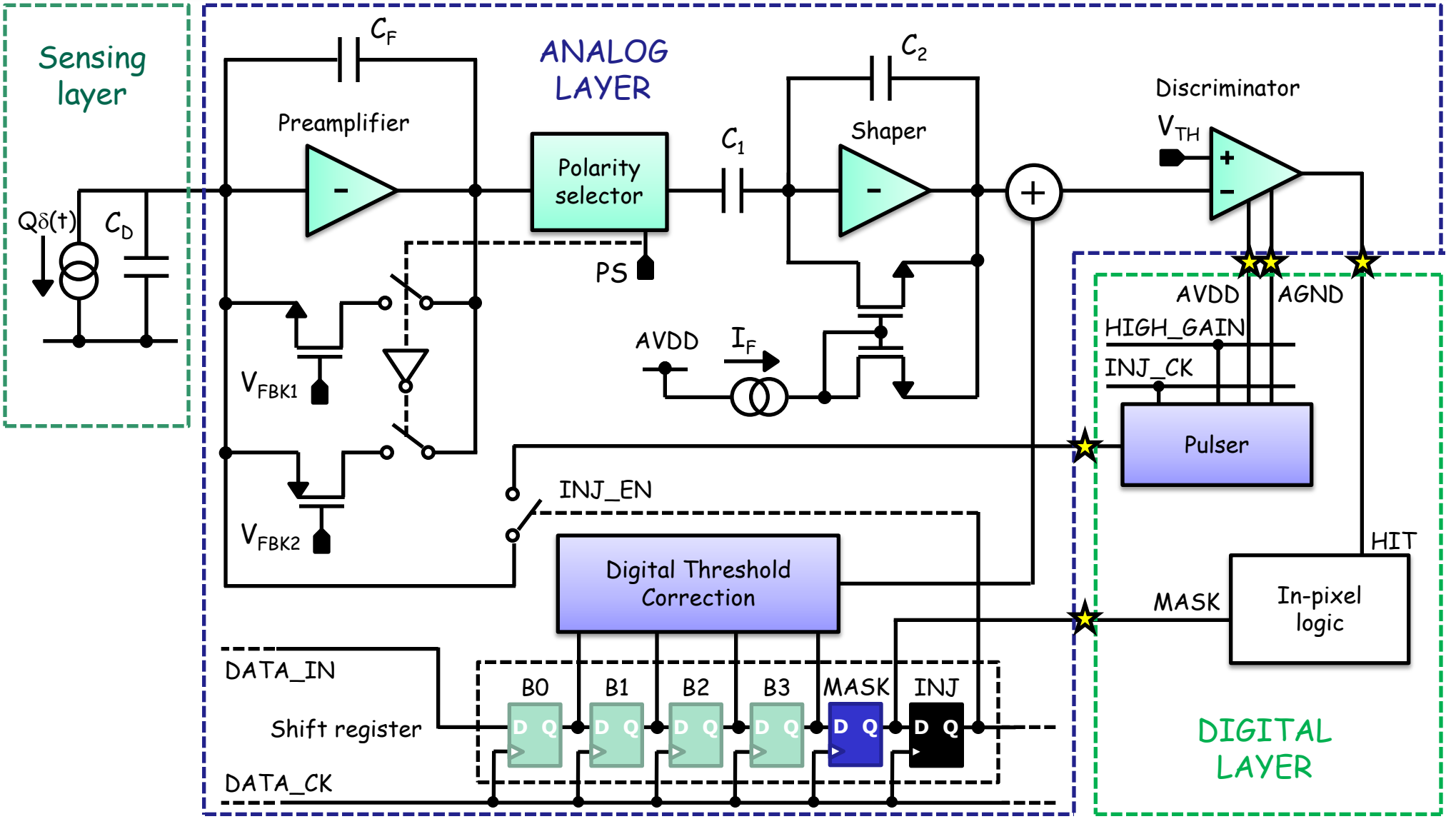
CMOS readout circuit



- Mixed signal (analog and digital) readout chip including
  - a front-end section with a periodical structure (50 µm pitch) complying with the sensor geometry – charge preamplifier, shaper, threshold discriminator, digital blocks performing data sparsification and communicating with the readout section
  - a readout section taking care of buffering, sparsification, I/O, slow control, pixel reset

- The digital readout architecture can work in data push or data pull mode (both solutions are implemented together with the possibility to select one or the other depending on the application requirements)

Readout chip front-end

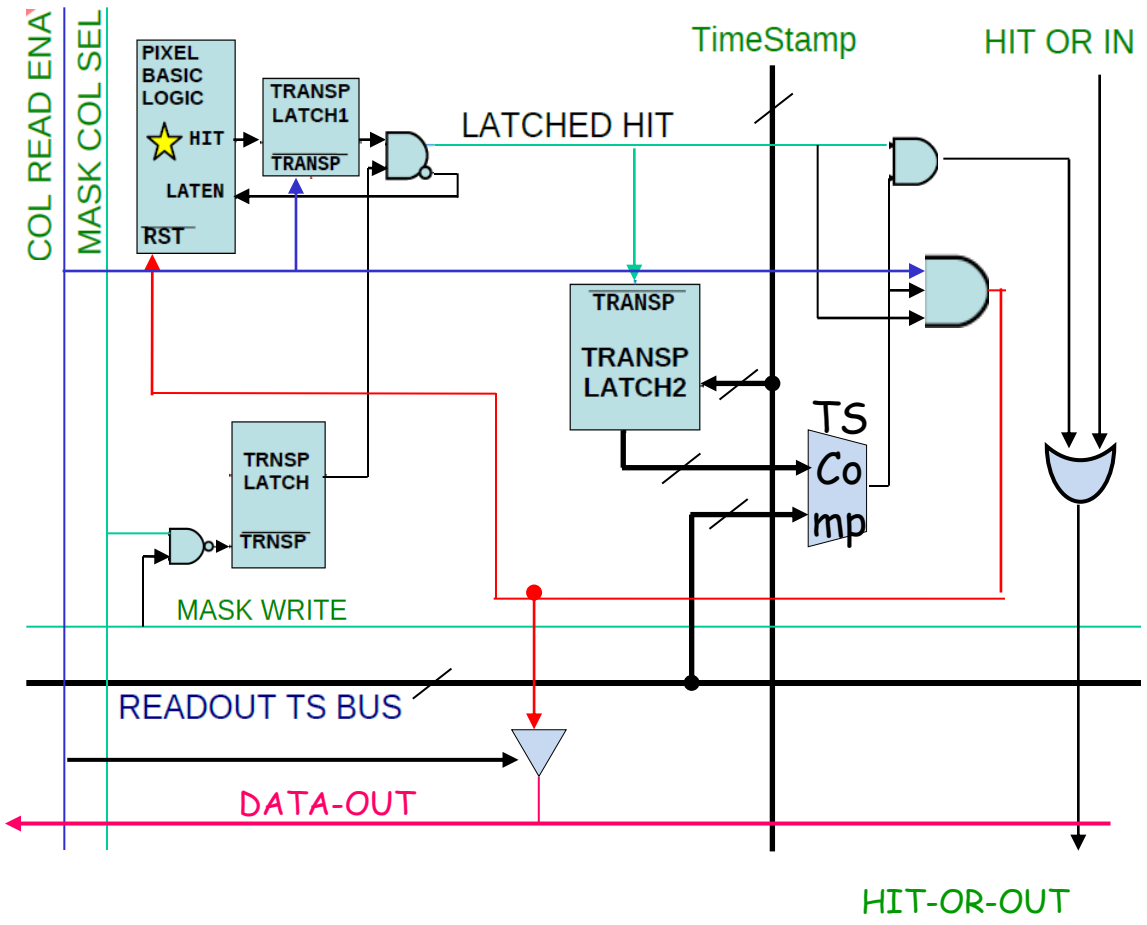


Analog front-end performance

Preamplifier Input Device [μm/μm]	18/0.25
Analog Power Dissipation [μW/pixel]	13.5
Peaking Time (Q_{inject} =16000 e-) [ns]	250
Charge sensitivity [mV/fC]	48
ENC @C_D = 150 fF [e- rms]	180
Threshold dispersion (before/after correction) [e- rms]	500/60

Time ordered readout with in-pixel time stamp

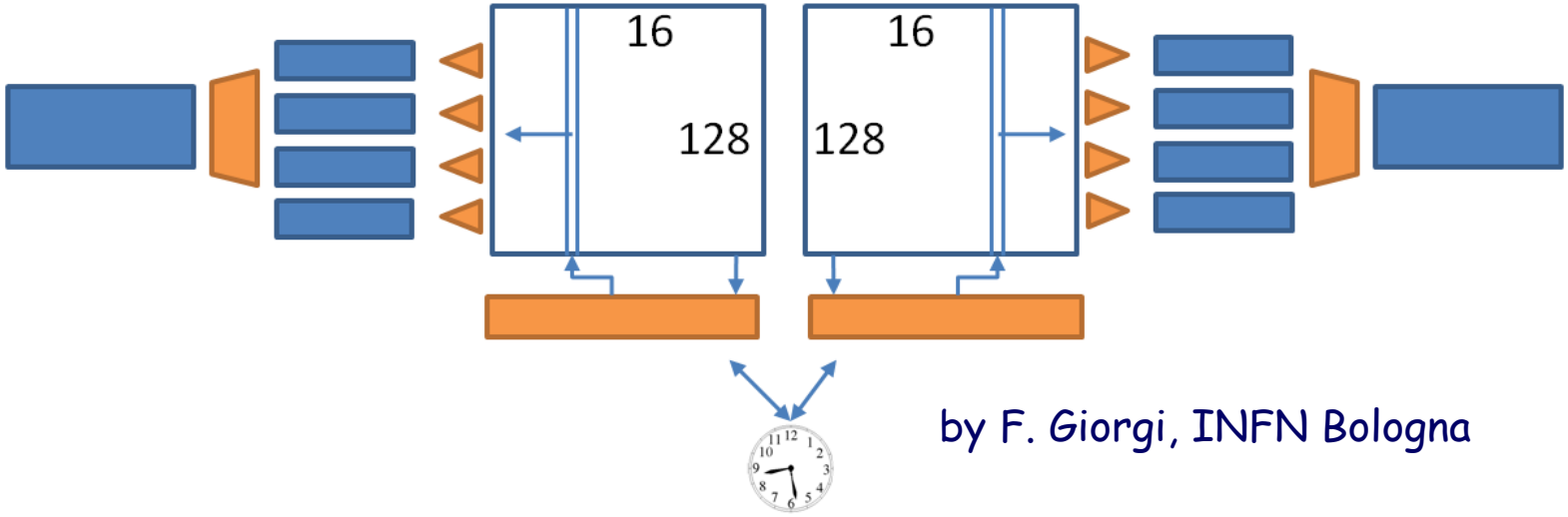
- Timestamp (TS) is broadcast to pixels; pixel latches the current TS when fired
- Matrix readout is timestamp-ordered
  - A readout TS enters the pixel and a HIT-OR-OUT is generated for columns with hits associated to that TS
  - A column is read only if HIT-OR-OUT=1
  - DATA-OUT (1 bit) is generated for pixels in the active column with hits associated to that TS
  - More in pixel logic with 3D integration



by F. Morsani, INFN Pisa

Readout architecture

- Can work both in data-push and data-pull mode
- Designed to sustain 100 MHz/cm^2 hit rate and 100 ns resolution
- 32x128 elements (2 sub-m. 16x128), 3.5 x 10 mm chip area
- Rows divided in 4 sparsifiers, each managing 32 rows (corresponding to 8 zones, W_{zone}=4 pixels)
- Power dissipation: 140 mW@200 MHz



by F. Giorgi, INFN Bologna

CMOS sensing layer

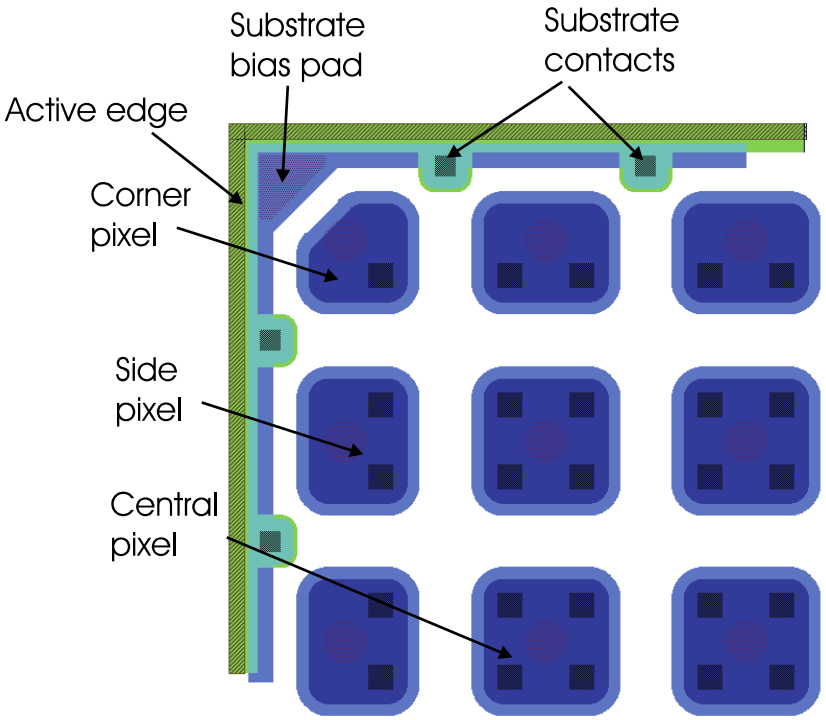
- CMOS sensors are getting used, or being considered, in a growing number of charged particle detectors mainly because of their high granularity, low material budget, integrated front-end electronics and low cost

- CMOS sensing tier to be realized in a CMOS process selected based on performance and cost considerations
  - XFAB 350 nm CMOS process, featuring a high resistivity, 15 μm thick epitaxial layer
  - an alternative 180 nm CMOS process, featuring higher radiation tolerance

- In both cases, the chips can be manufactured in engineering runs with restricted reticule area (so called MLM option), with a substantial reduction of the costs

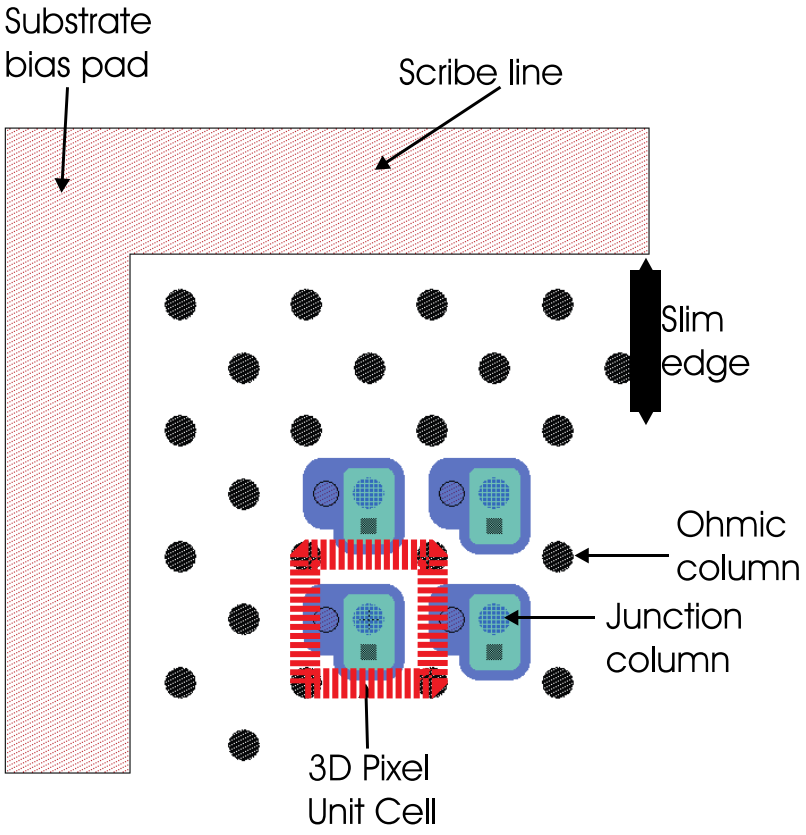
- The sensor may benefit from a prototyping step taking place in 2012 to finalize the choice between the two processes

Fully depleted edgeless sensors (FBK, Trento)



- Deep Reactive Ion Etching (DRIE) is used to obtain deep and narrow trenches around the active area ➔ no more need for cutting
- Trenches and back-side of the sensors are heavily doped so as to behave like ohmic contacts ➔ the active volume is surrounded by ohmic walls, except for the front-side
- A support wafer (could be an epitaxial wafer) is needed to keep the sensors together after trenches are etched; to separate the sensors, the support wafer is removed ➔ overall material budget is minimized
- A critical feature is the distance between the trench and the outermost biased electrode (actually, with a 20 μm distance, 200 V can be applied without breakdown) ➔ smaller pixels on the sensor sides, the smallest being in the corner to accommodate the substrate contact

Fully depleted 3D slim edge sensors (FBK, Trento)

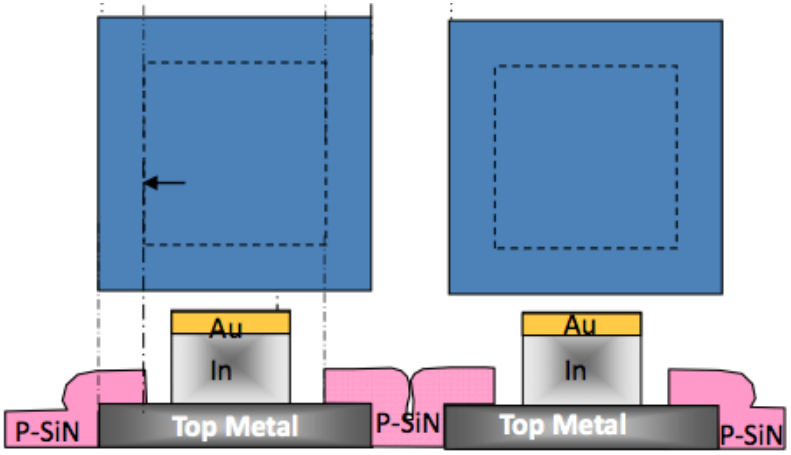


- 3D sensors feature columnar electrodes of opposite doping types etched all the way through the substrate by DRIE
- Distance between the electrodes is independent of the substrate thickness and can be made very small ➔ reduced charge trapping effects and smaller operating voltage in irradiated devices
- Active edge (and use of a support wafer) is not compatible with double side technology but a slim edge approach is feasible – multiple fence of ohmic column to prevent the depletion region from spreading from the active volume to the cut line
- A small inefficient region at the edge is present, nevertheless this solution would largely improve the dead area features of currently available pixel systems

T-Micro μ-bumping process

- Very high interconnect density, with small bond pads (squares with a side of 5 or 10 μm, depending on the bump size, 2x2 μm^2 or 8x8 μm^2) both on the sensor and the readout sides ➔ more room for top metal routing, in particular for power and ground lines, smaller capacitive coupling

- T-Micro has provided guidelines concerning mainly
  - marks for rough and fine alignment (through IR imaging, image data alignment system to be installed)
  - design around bump (landing pad top metal size, pad opening size)
  - daisy chain test structures



- Initial cost: about 60 kEuro/10 chips (stacked) – 80% goes into development (process optimization). After process optimization, cost per (stacked) chip is 1/5-1/10

Advantages of the proposed approach

- Sensor granularity presently forbids implementing a large amount of functions per pixel, with restricted data rate handling capabilities as a consequence; the project should enable a substantial increase in the complexity of the in-pixel functionality ➔ **improved data rate capability while keeping pixel pitch compliant with point resolution requirements in advanced tracking applications**
- Prototypes developed within the project should demonstrate that most, if not all, of the peripheral circuitry integrated in present sensors can be implemented on top of the sensing area ➔ **material budget improvement, 3- or 4-side buttable chip modules**
- In the case of CMOS sensors, the main limitation lies in the fact that commercial processes providing acceptable charge sensing performance tend to have a relatively large feature size, limiting functional density and radiation hardness; use of a readout tier fabricated in a process with a significantly smaller feature size than the sensing layer can **increase the functional density, improve radiation tolerance** and **reduce the costs**

Financial structure of the project

Item	Funding Agency	Resources
CMOS sensors (XFAB, 350 nm CMOS)	CNRS	80 kEuro
Edgeless sensors (FBK, Trento)	INFN (VIPIX experiment)	20 kEuro
Slim edge 3D sensors (FBK, Trento)	INFN (TRIDEAS experiment)	33 kEuro
Readout chip (T/G, 3D 130 nm CMOS)	INFN (VIPIX experiment)	125 kEuro
Sensor-to-chip vertical integration (T-Micro)	AIDA WP3 and INFN (VIPIX experiment)	55 kEuro (INFN) + 145 kEuro (100 kEuro from CNRS and 45 kEuro from INFN AIDA WP3 budget)

Timescale

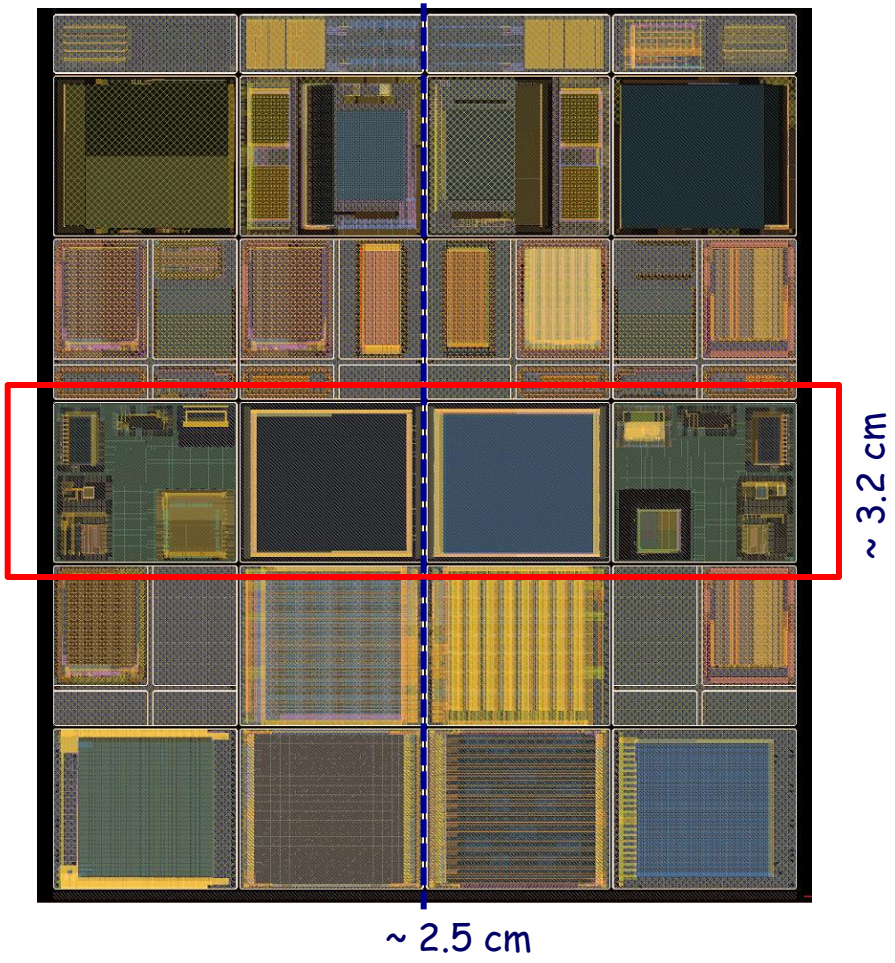
For each task in the table, the delivery time with respect to the AIDA project start date is indicated

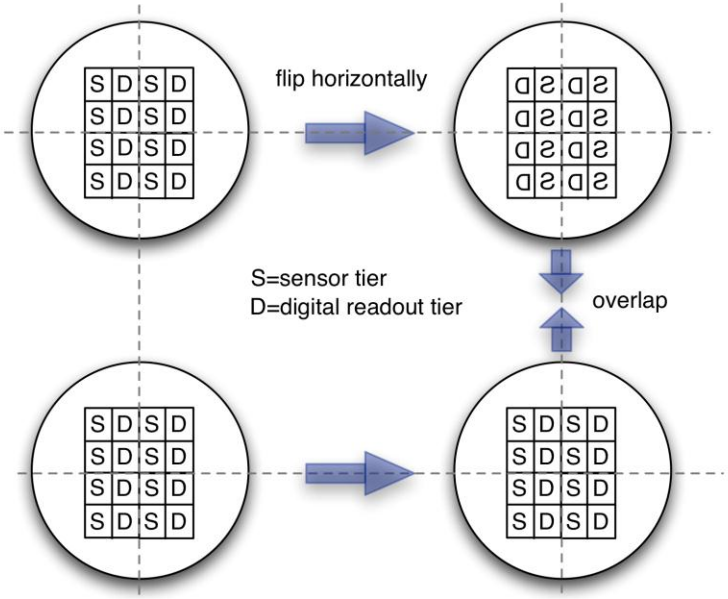
Task	Delivery time
Edgeless sensor design (FBK)	Month 14
Edgeless sensor production (FBK)	Month 23
CMOS sensor design (IPHC-IRFU)	Month 26
CMOS sensor production (IPHC-IRFU)	Month 29
Readout chip design (INFN)	Month 17
Readout chip production (INFN)	Month 26
Readout chip-to-sensor vertical integration (T-Micro)	Month 41

Backup slides

The 3D-IC collaboration

- Several groups from US and Europe have been involved in the first 3D MPW for HEP (pixel and strip readout chips for ATLAS, CMS, B-factory, ILC) and photon science applications (X-ray imaging)





- Single set of masks used for both tiers to save money
  - identical wafers produced by Chartered (now Globalfoundries) and face-to-face bonded by Tezzaron
  - backside metallization by Tezzaron

DNW MAPS test structures

- Small test structures
  - single pixels with and w/o detector emulating capacitor shunting the readout channel input (analog only)
  - 3x3 DNW MAPS matrices (analog only, for charge collection tests)
  - 8x8 and 16x16 DNW MAPS matrices (analog and digital, for readout architecture test)