R&D towards a 3D - Via last interconnect Technologies for Pixel detectors

Atlas IN2P3 project

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Why do we go for 3D technologies, for HL-LHC. Criteria to be fulfilled :

- Better granularity & 4 size abuttable devices (Shrink pixel dimensions to decrease the form factor of the final device)
- Low material budget (Submicron technologies + thin sensors using innovative interconnect techniques: slid, microbumps…)
- Radiation hard Si detectors (Oxygenated silicon) and electronics (CMOS 130 nm and 45 nm)
- Low power dissipation systems (low noise electronics and use of TSV technology in place of wire bonds, bumps…)

Prospects

In parrallel : To exploit and combine two major technology advances and evaluate potential beneficts

- Use 130 nm CMOS and potential availability of 65 nm in Research laboratories in close cooperation and coordination with CERN-Mic

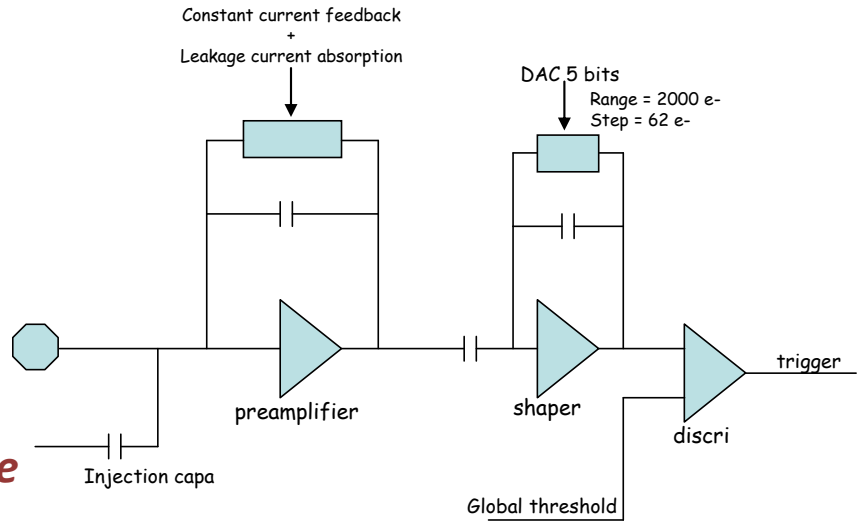
(process of building a 65 nm « club » or task force)

- Take advantage of « open » TSV providers in Europe to demonstrate the feasability of TSVs on functional detector chips.

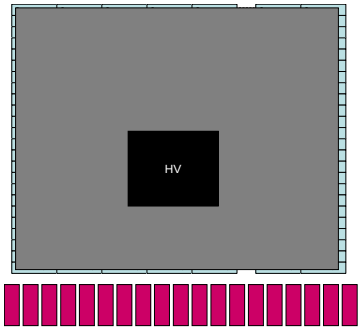
OMEGAPIX2 project : CHIP for pixel readout (IBM 130 nm) chartered-Tezzaron

Targets :

- Low threshold (1000 e)
- Low noise ~300 fF
- Cope with high leakage current (up to 100 nA per channel)
- 8 bits local threshold adjustment
- Time-Over-Threshold measurement
  - 3 bits
  - ***Clock multiplier (40Mhz to 160 Mhz) possible***
  - ***Optimized readout for maximum charge measurement accuracy and event pile-up***
- On pixel memory of ***up to 3*** event between each Lv1 clear
- Ambitious goal is to couple this chip to a sensor and bring it in test-beam for performance study, radiation damage studies
- Entangled with Slim Edge sensor R&D to produce 4 side buttable device



3 bits
Range = ~ 10,000 e-
Step = ~ 1250 e-



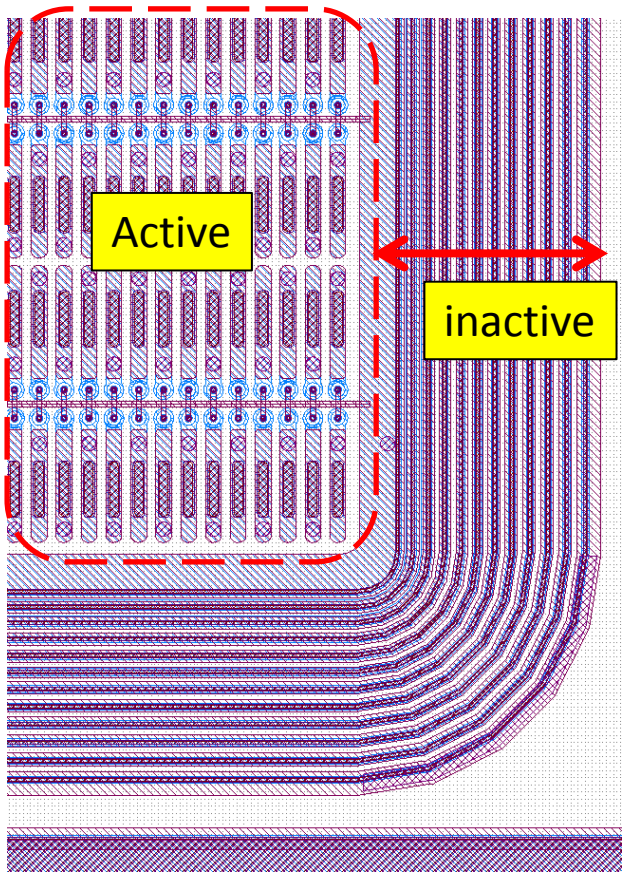
Submitted end 2011

OMEGAPIX2 sensor For ATLAS HL-LHC

- Reduction of Phi resolution has been shown to be more beneficial to ATLAS tracking performance than Z resolution -> **Pixel of 35x200 um**

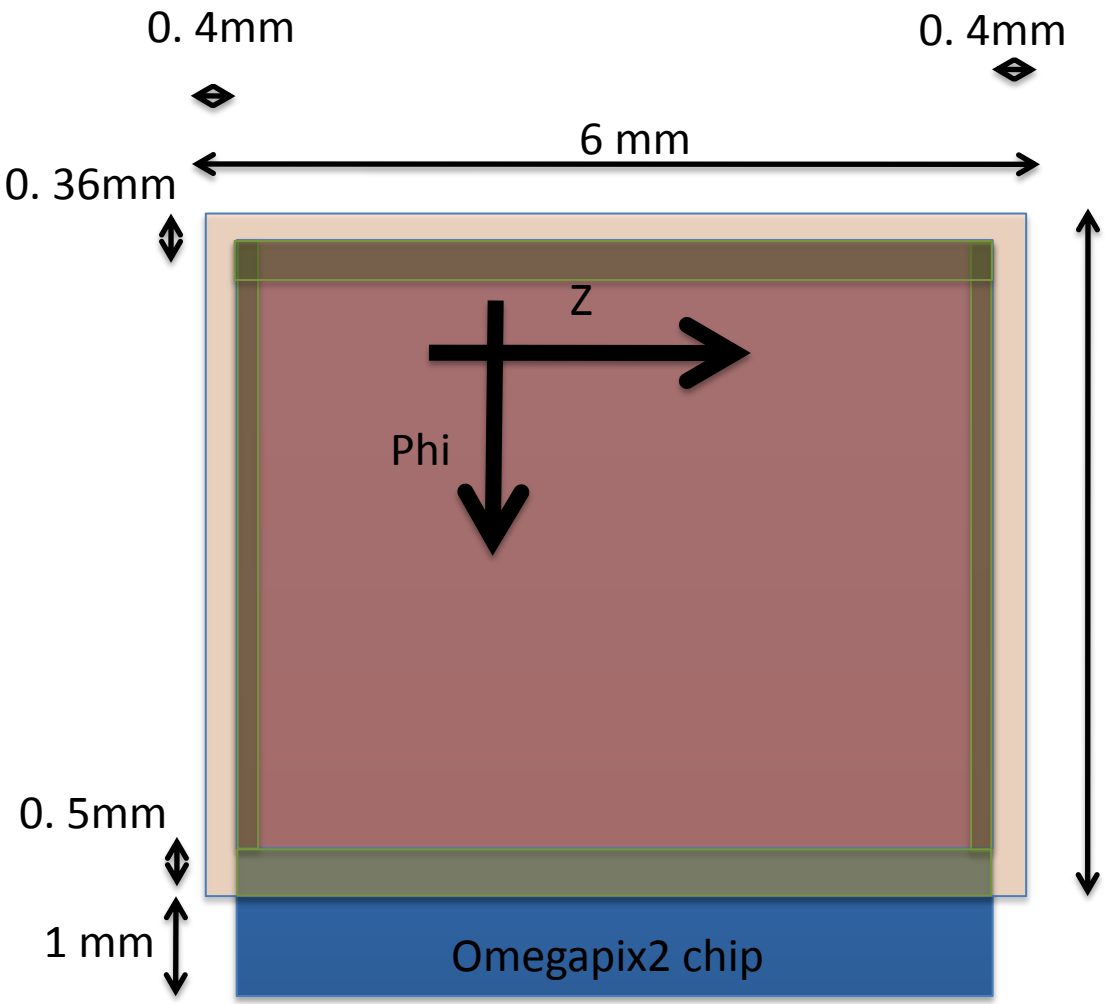
- OMEGAPIX2 will provide a complete read-out chain usable in testbeam and other complete standalone system test

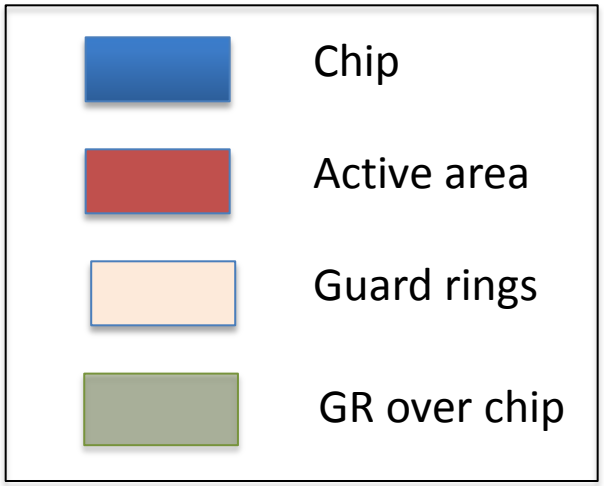
- The chip could provide spectroscopic measurements at low luminosity (ie details charge measurement) and fast operation at higher luminosity



Planar Pixel Sensor

Sensor developpement: Guard Ring Sensor





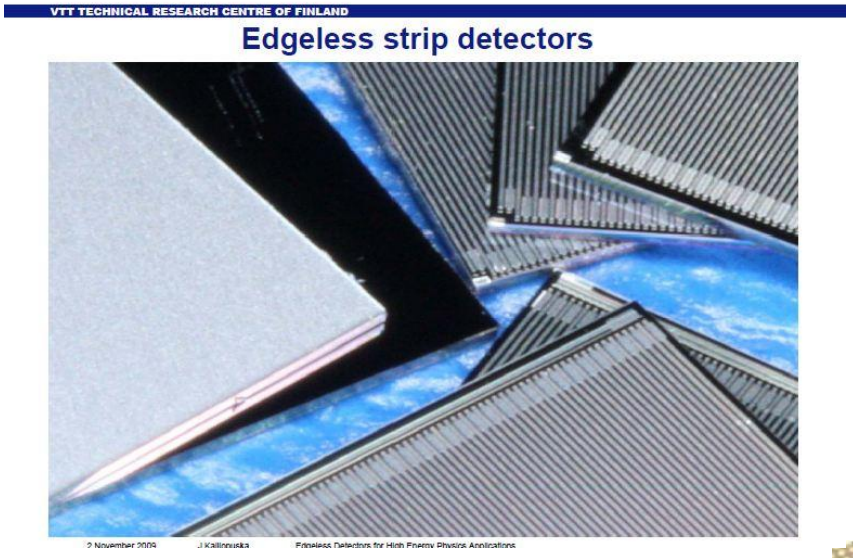
In X : 24 pixel of 200 microns
In Y : 96 * 35 microns

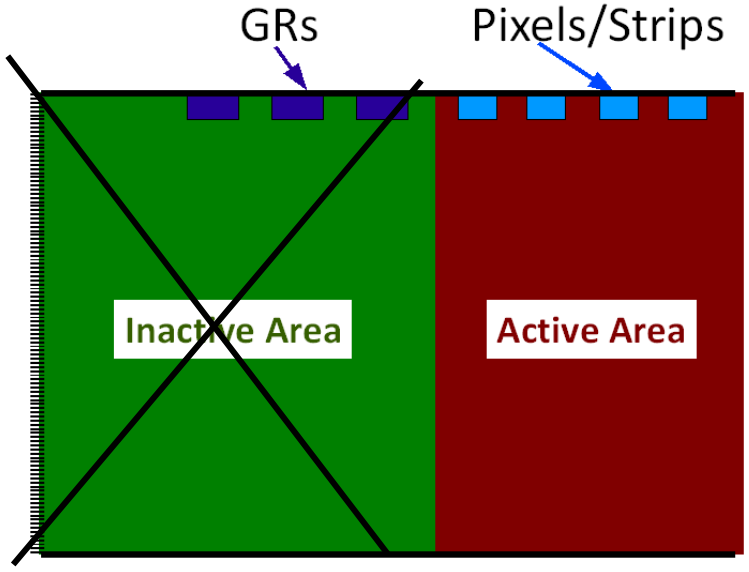
Active zone : 4.8mm x 3,36

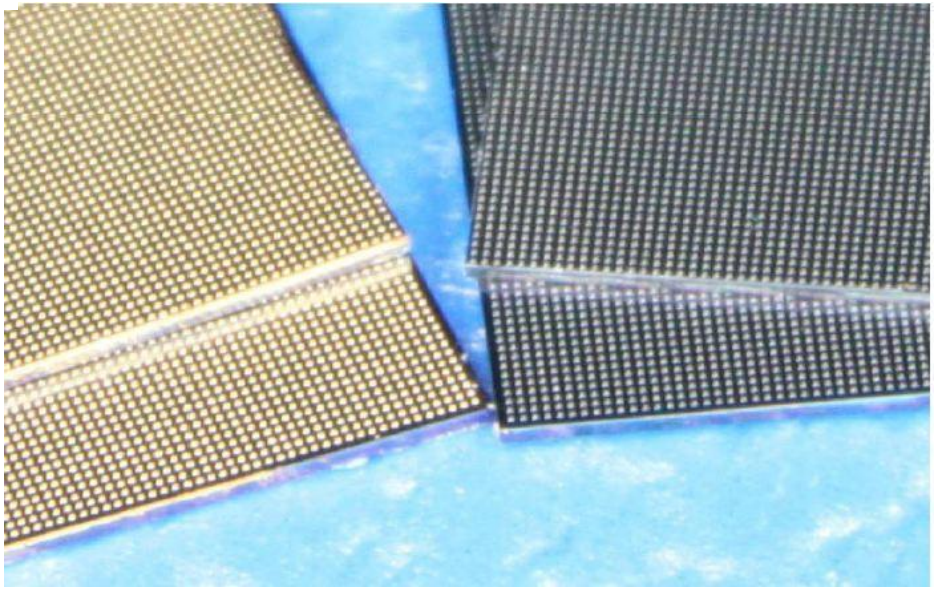
The GR are overlapping the chip by
100 um on the Z edges and by
140 um on the top Phi edge

Foundry Cis

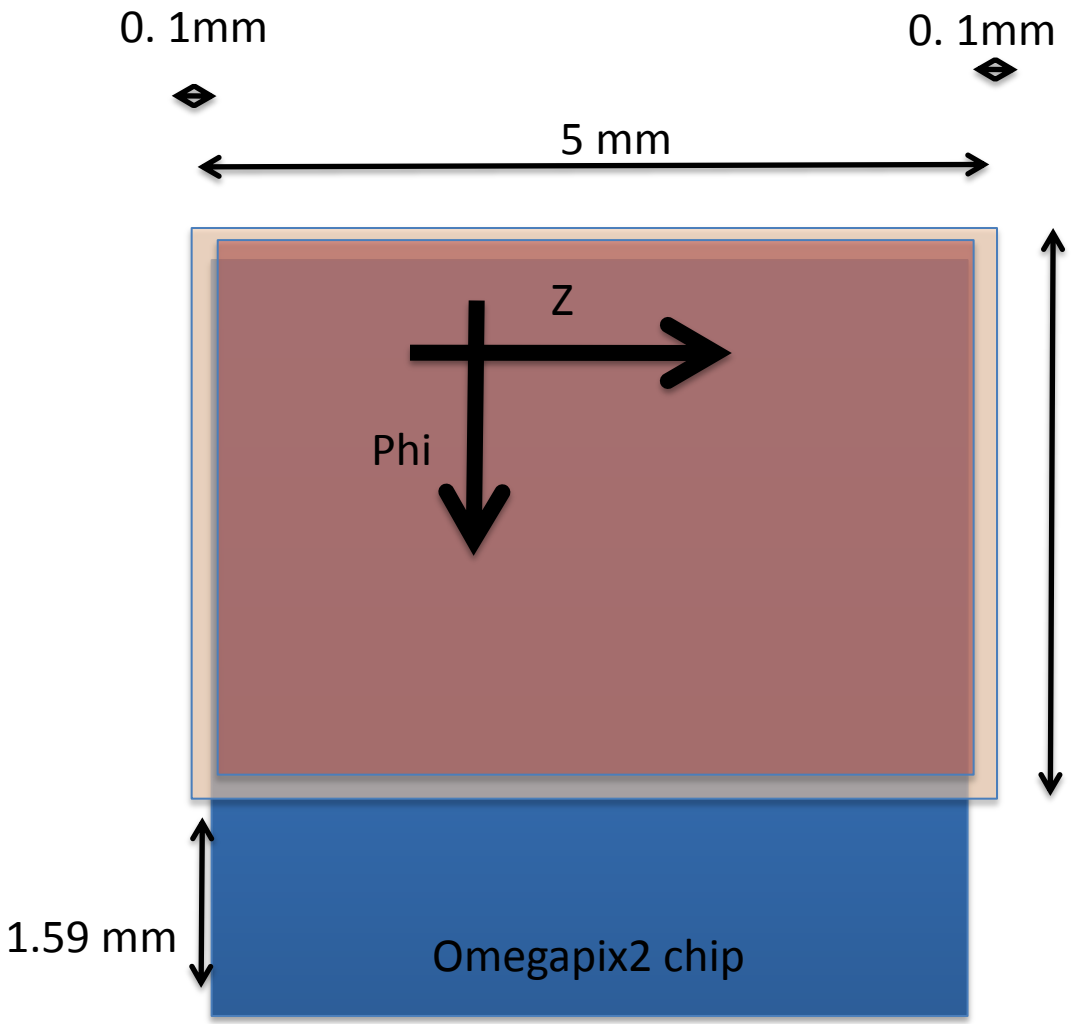
Towards Edgless sensor technology

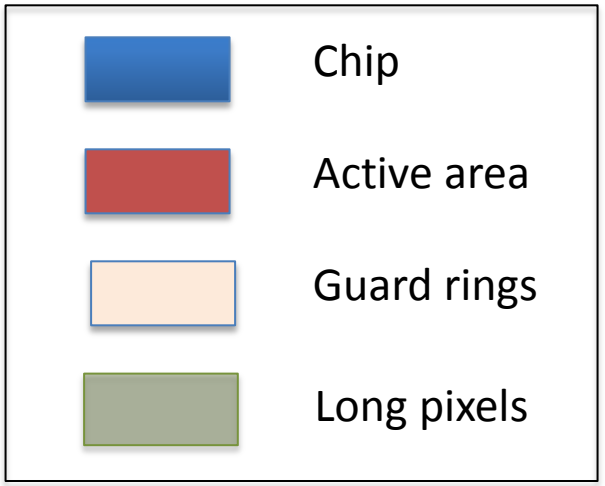






Sensor developpement: Active Edge Sensor





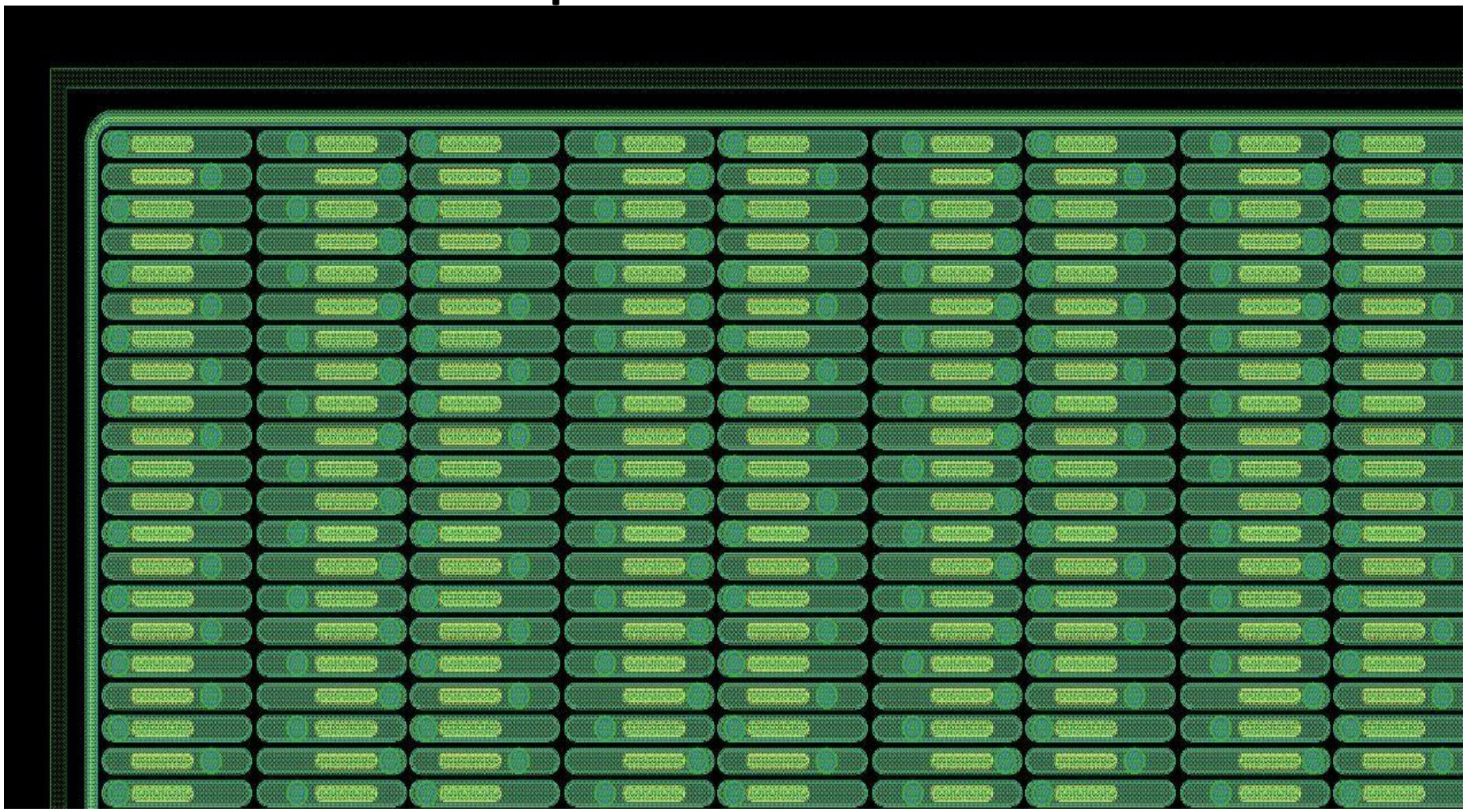
In X : 24 pixel of 200 microns
In Y : 96 * 35 microns

Chip 5x5mm

100 um edges in z side
50 um edge in phi side

Foundry VTT

VTT Edgless pixel matrix under production

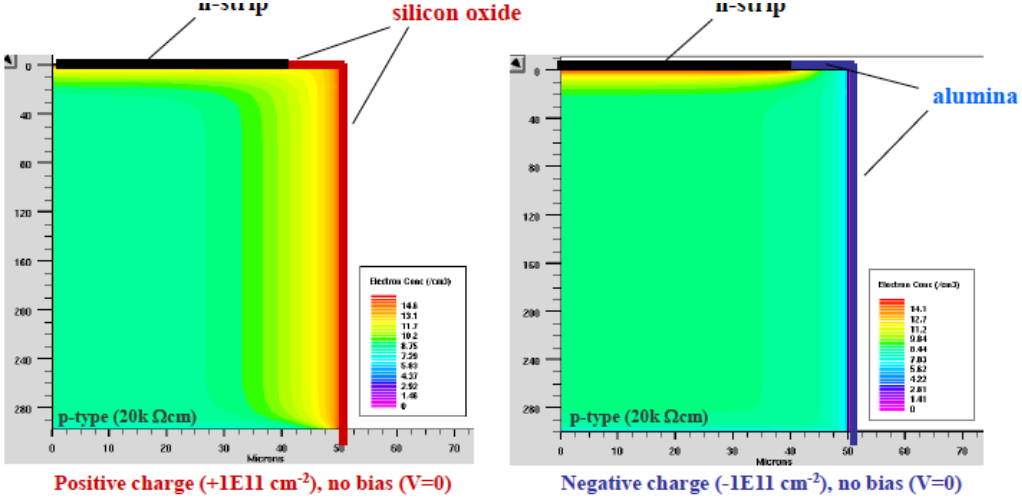


Promising approach :RD 50 Slim Edges

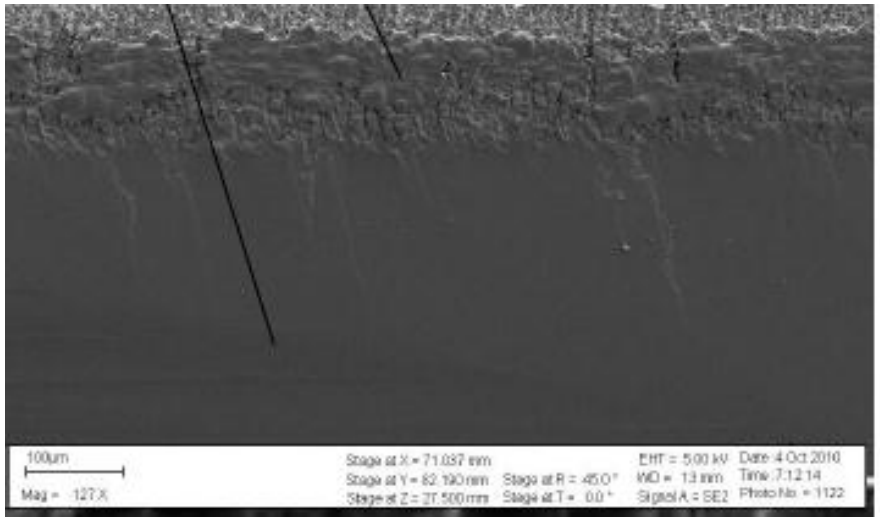
Slim edge is achieved through post-processing by creating a clean cut at the edge of the sensor:

- Laser scribing
- Cleaving

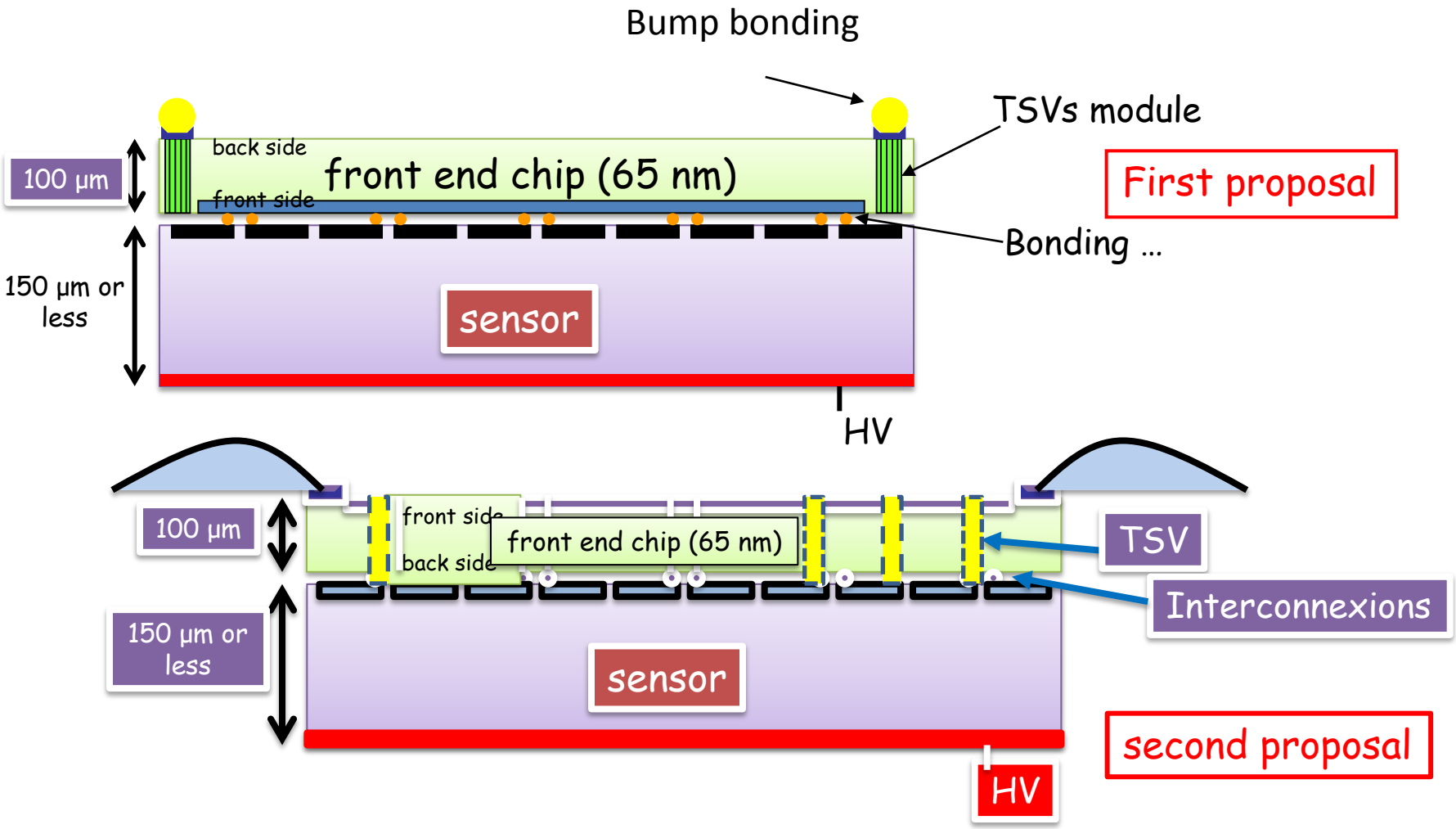
Passivation of the edge using Alumina **Atomic Layer Deposition** can be used with new material to control oxide charge and control potential drop in the sensor.



- silicon oxide → electrons path from n-strip to sidewall
- alumina → electrons "pushed away" from sidewall

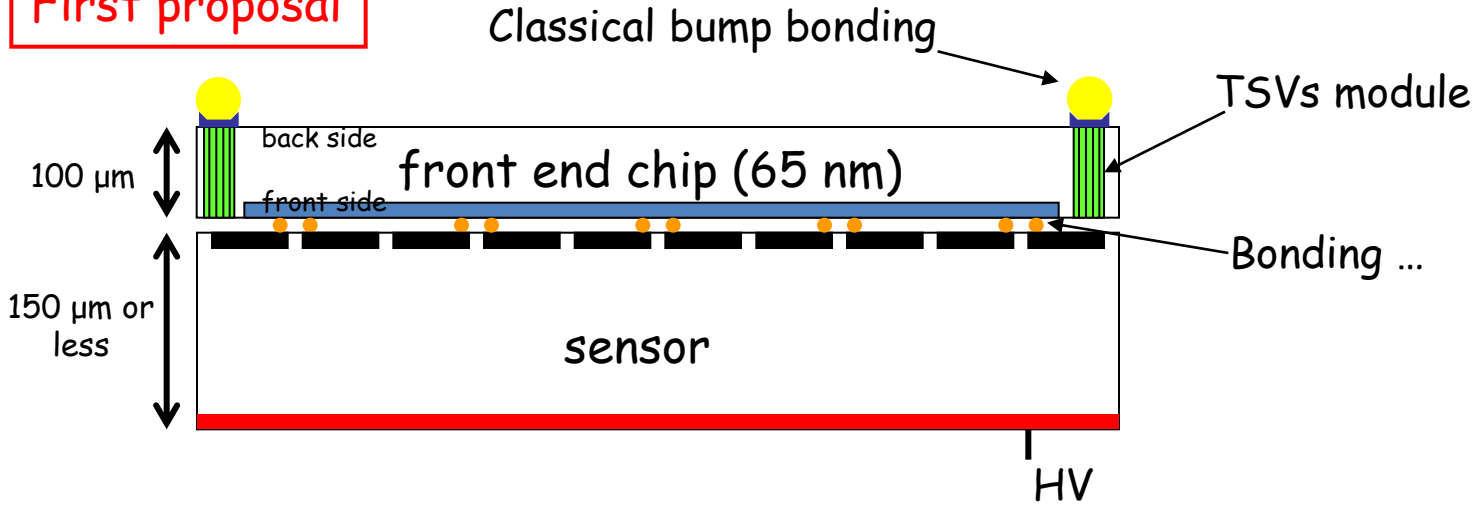


Santa Cruz



Via Last AIDA project: LAL + LPNHE+ LAPP

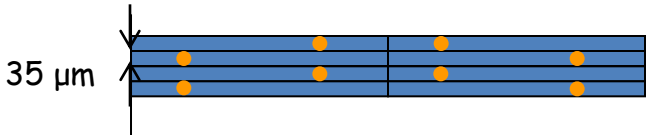
First proposal



Process steps

- Front end chip fabrication in 65 nm techno (IBM) with analog and digital signal processing and sensor fab
  - ✓ no pads, only available area for futures TSVs
- via-last post-processing
  - ✓ I/O access by the chip's back side
  - ✓ Several TSVs for one pad => better yield
- thinning up to reach TSVs, back metallization (100 µm final thick)
- bonding sensor: ~ 35 µm pitch

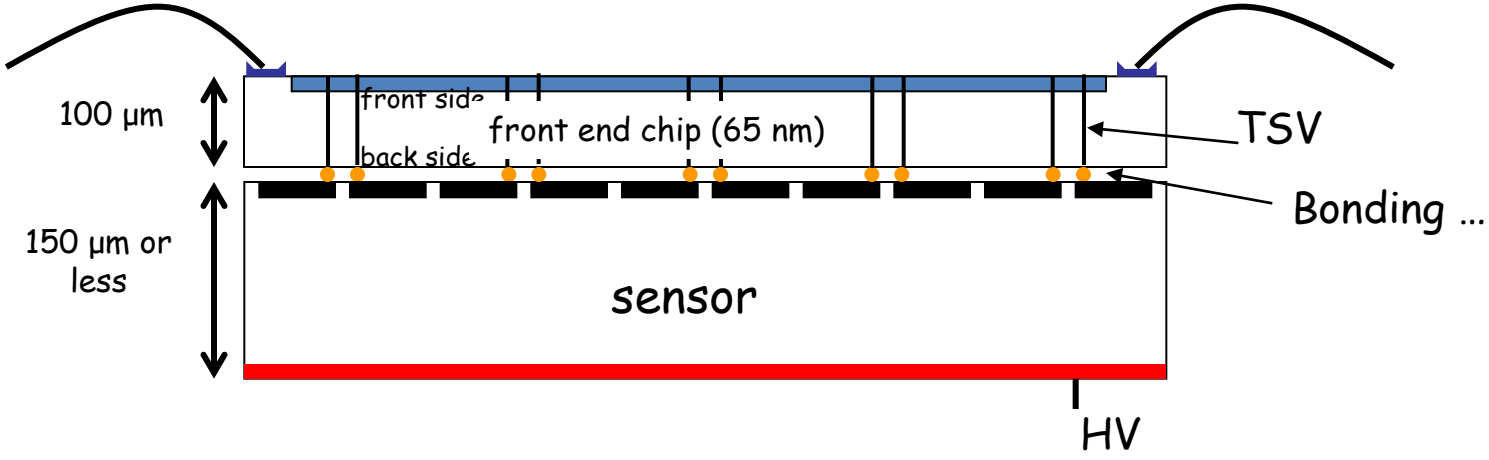
Matrix organization



Pixel bonding will be placed in alternance to get minimal pixel width

Second proposal

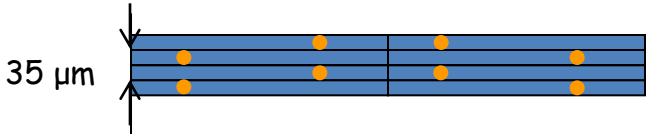
Much more ambitious!!



Process steps

- Front end chip fabrication in 65 nm techno (IBM) with analog and digital signal processing and sensor fab
- via-last post-processing
  - ✓ one TSV by pixel
- thinning up to reach TSVs, back metallization (100 µm final thick)
- bonding sensor: ~ 35 µm pitch

Matrix organization



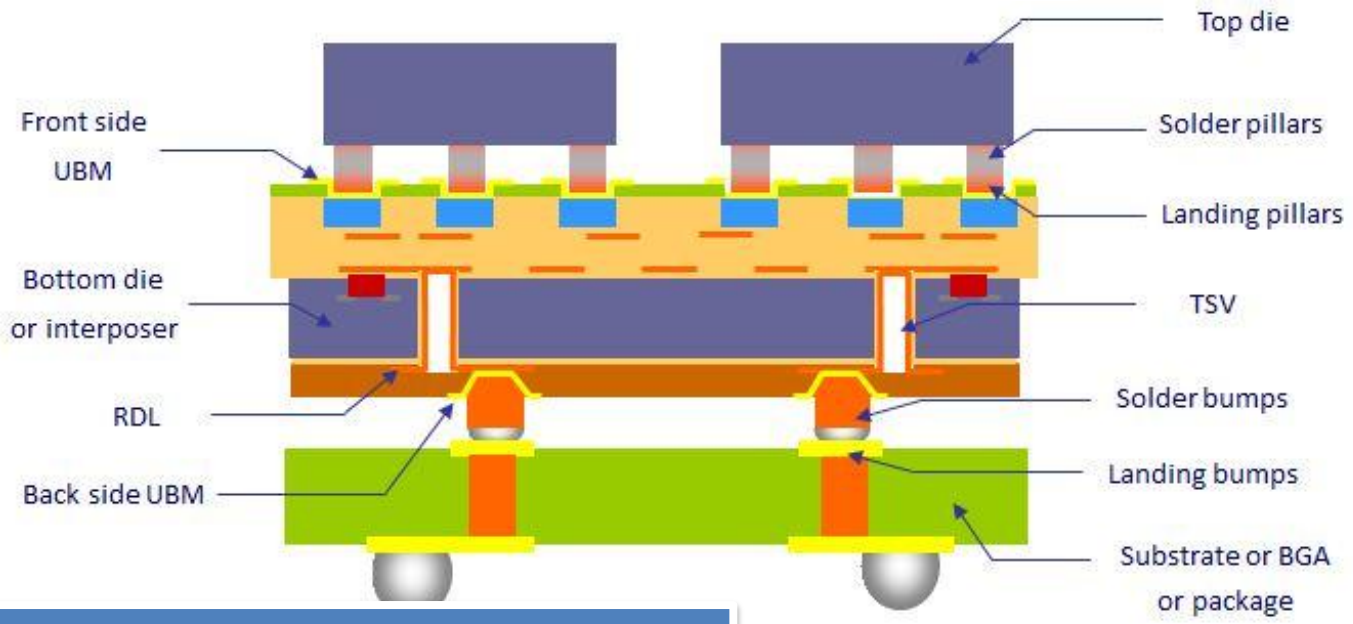
Pixel bonding will be placed in alternance to get minimal pixel width

Exploit industrial know how

Open 3D™ Initiative (LETI-GRENOBLE)

General information

- **The purpose of this specification guide is to give a maximum of information to LETI in order to prepare the technical proposal**
  - The customer must fill the column "customer answer"
  - The orange cells are mandatory to fill
  - The blue cells are optional



Meeting scheduled April 20th,2012 at Grenoble

Industry offers

institute	TSV					interconnection			wafer size	
	diameter	aspect ratio/depth	filling	pitch	type	type	pitch	diameter		
CEA Leti	30µm 40µm 60µm	1.5:1 03:01 02:01	Cu liner	80µm	from backside to M1	solder pillar (Cu- SnAg) solder bumps (Cu SnAg)	50µm 120µm	25µm 80µm	200/300 mm	for TSV?
CMP/MOSIS	100µm	2.5:1 (250 µm)	Cu liner?	400µm	via middle with 0.35 µm CMOS					2 Tier 3D by Tezzaron Austria Microsystems
EMFT	2 µm 10 µm	> 8:1 4:1 (40µm)	Tungsten Tungsten/C	4µm 20 µm	apect ration: 16:1	SLID (SnCu)	< 30 µm	25 µm	200/300(?) mm	
IZM	15 µm large (100µm?)	50 µm	Cu filling Cu lining	30 µm large (>100 µm?)	interposer tapered	SnAg(Cu), CuSn, Au, In Au nano porous	20 µm?	10µm	300	Dresden
IMEC	25µm	2:1 (50µm)	Cu filling	40µm	via last	CuSn (in)	20µm (10µm?)		200	
	5µm	4:1 (20µm)	Cu filling	10µm	via middle (with 130nm in- houswe CMOS)				200	
VTT	60µm (top)	2:1 (120µm)	Cu lining	90µm	tapered (86deg)	SnPb, InSn, PbSn, SnAg	25µm	50µm	150 µm (TSV)	
T-Micro	0.5-2.8 µm (tapered) 2.5 µm	< 40µm < 55 µm	tungsten polysilicon	~10 µm small	via last via first	microbumps + adhesive	5µm	2µm	200mm (or larger?)	

Project forecast & Time scale

- A-operation: is to get slim edge Pixel sensors (IZM) with Omegapix2 chip- 05/2012
- B-operation is to get edgless pixel sensors (VTT) with Omegapix2 chip- 05/ 2012
- Third step is to have an Omegapix ASIC readout 130nm (end 2013)and later-on 65nm
- Deliver a 4 side abuttable monolithic edgless device where I/O signals are routed vertically through the readout chip (~2015)

Thank you

VTT slim edges sensors

Slim edge is achieved through:

- Extreme quality of the sensor surface
- Implantation of the edges after etching

Important requirements:

- Implementation of p-spray and moderated p-spray implantation in VTT process
- Radiation hardness