SLID-TSV interconnection of FE-I4 modules at EMFT

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In collaboration with

Fraunhofer EMFT

Max-Planck-Institut für Physik
(Werner-Heisenberg-Institut)

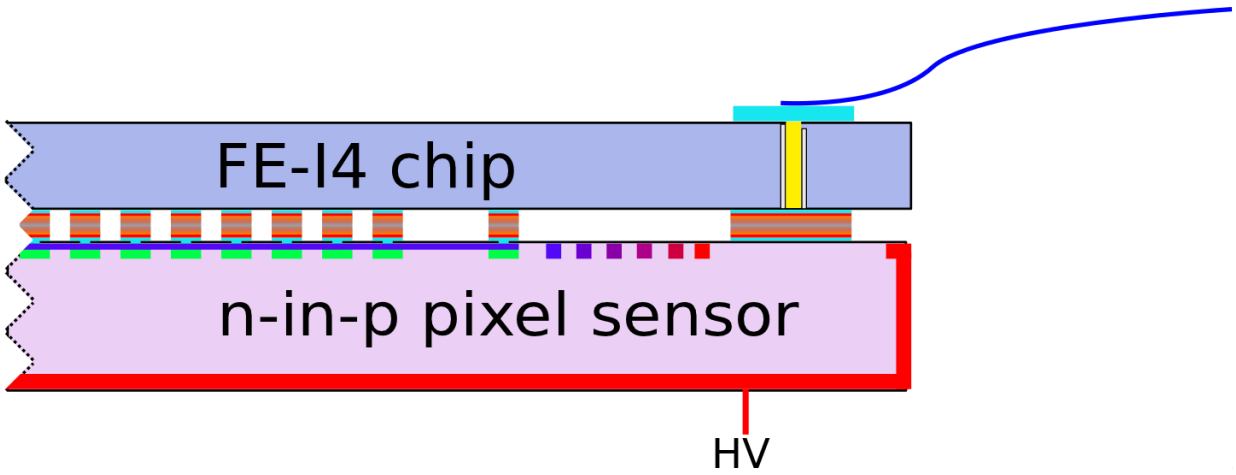
Contents

Interconnection of FE-I4 modules with SLID and TSV

Demonstrator module for SLID and TSV technologies based on ATLAS FE-I4 chip and n-in-p pixel sensors with a thickness of (150-200) μm:

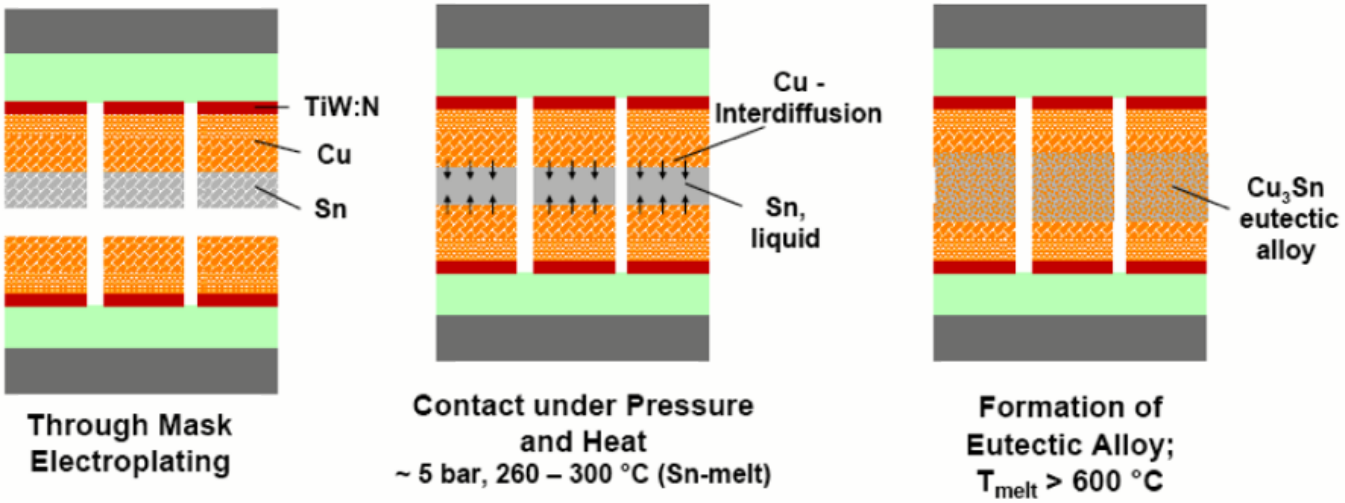
- SLID as possible alternative to bump-bonding.
- TSV with Via Last approach below the wire bonding pads to test the possibility of transport signal and services across the chip.

R&D on the FE-I4 modules will profit from the experience gained with the SLID interconnection of FE-I3 devices.



R&D targeted to the inner layers of the upgraded pixel detectors at HL-LHC, to reduce material budget and increase the module active fraction.

SLID: Solid Liquid Inter-Diffusion



Alternative to bump bonding

Pros

- Allows for vertical integration (T_{melt}).
- Arbitrary geometries possible and smaller pitches.
- Less process steps $\rightarrow$ lower cost.
- Wafer to wafer and chip to wafer possible.
- Strength: 0.01 N per connection

Challenges

- Planarity of 1 μm needed.
- No rework possible
- Chip-to-chip not possible at the moment
- Homogeneous pressure needed

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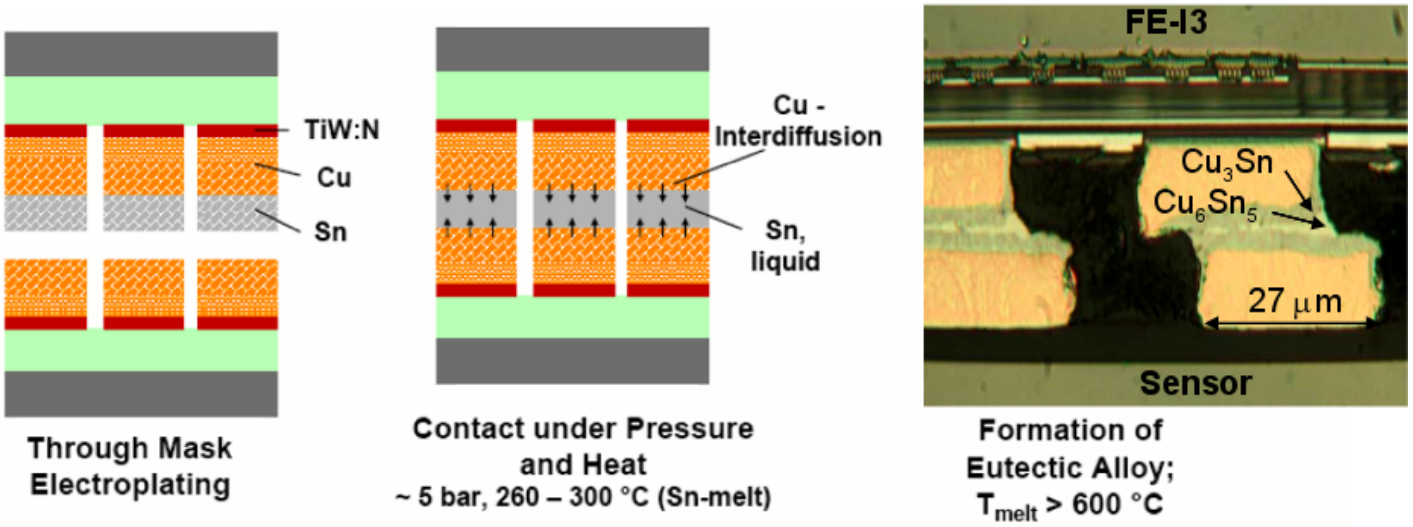

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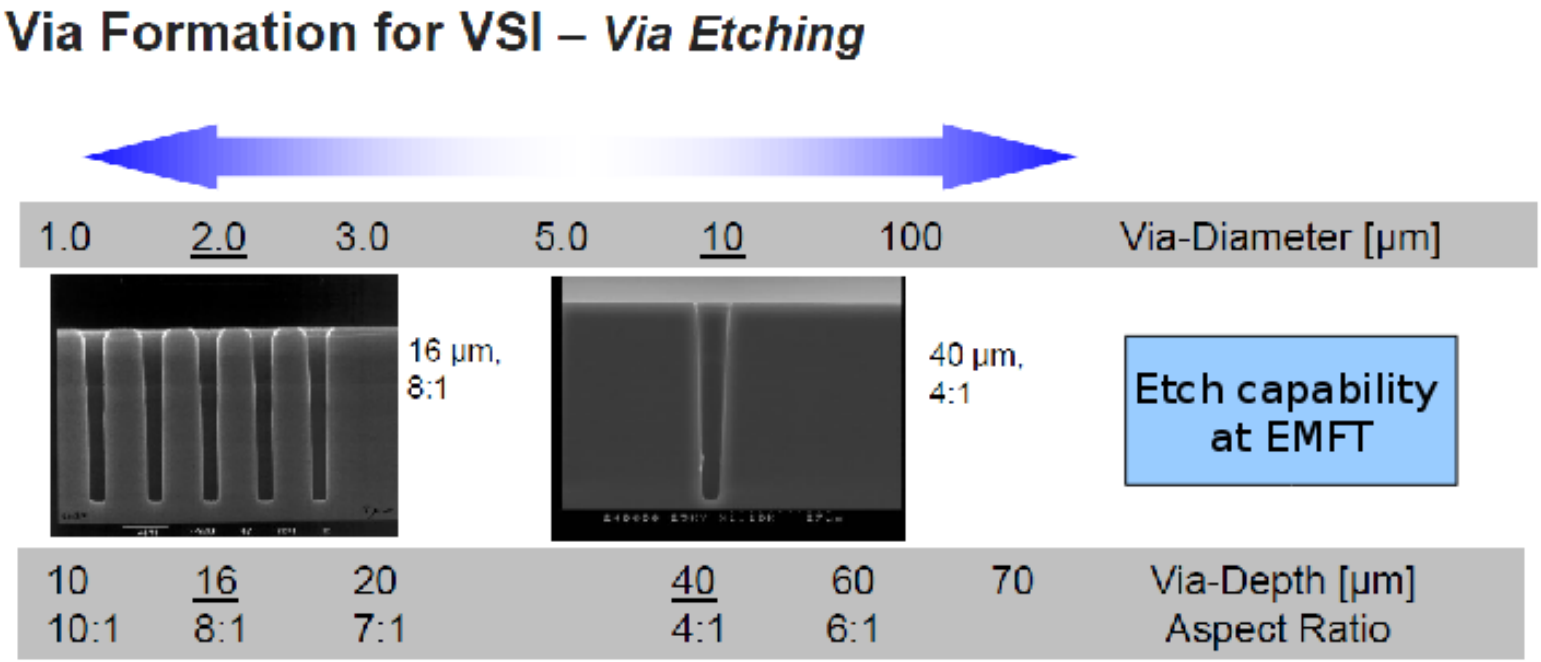
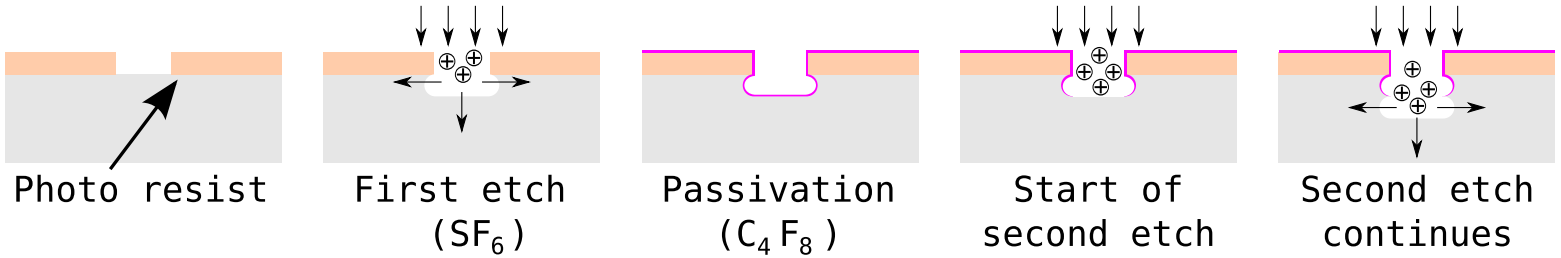
Through Silicon Vias at EMFT

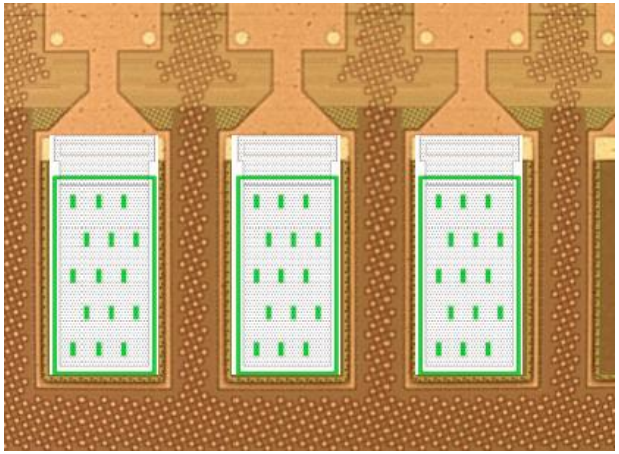


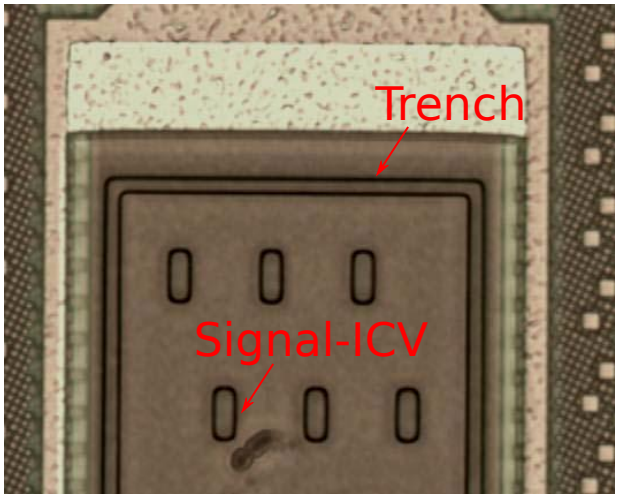
Potential of high density vertical wiring
→ possible extension of the technology to pixel by pixel TSVs

Bosch Process



1. Via-etching in Bosch-process.
2. Insulation with TEOS (low T)
3. Tungsten filling of vias.
4. Thinning to desired thickness of chip.
5. SLID-interconnection.

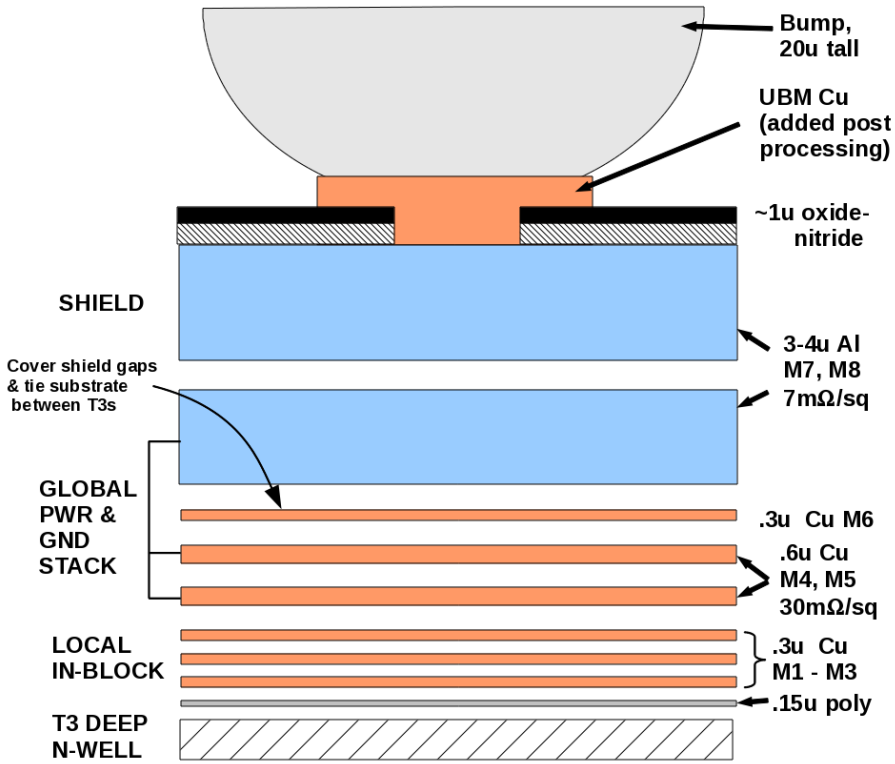




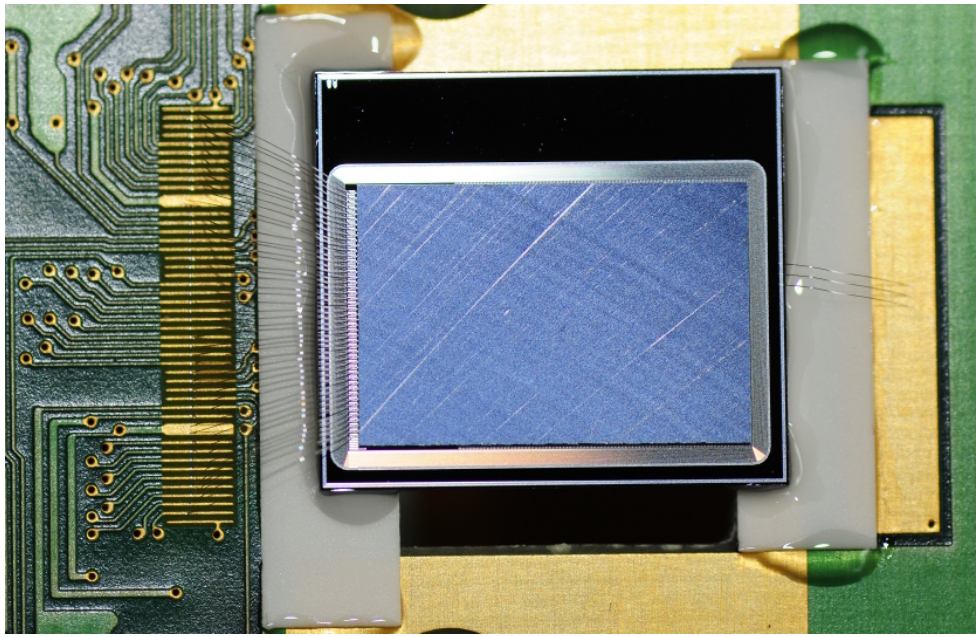
FE-I4 - TSV etching from the backside?

The possibility to etch TSV on the wire bond pads has been foreseen in the design :

- Half of the wire bonding pad is empty in the BEOL layers
- Top metal layer of the pad is connected to the first metal layer
- In principle no front-side processing needed



What could be the final chip thickness when etching from the backside?

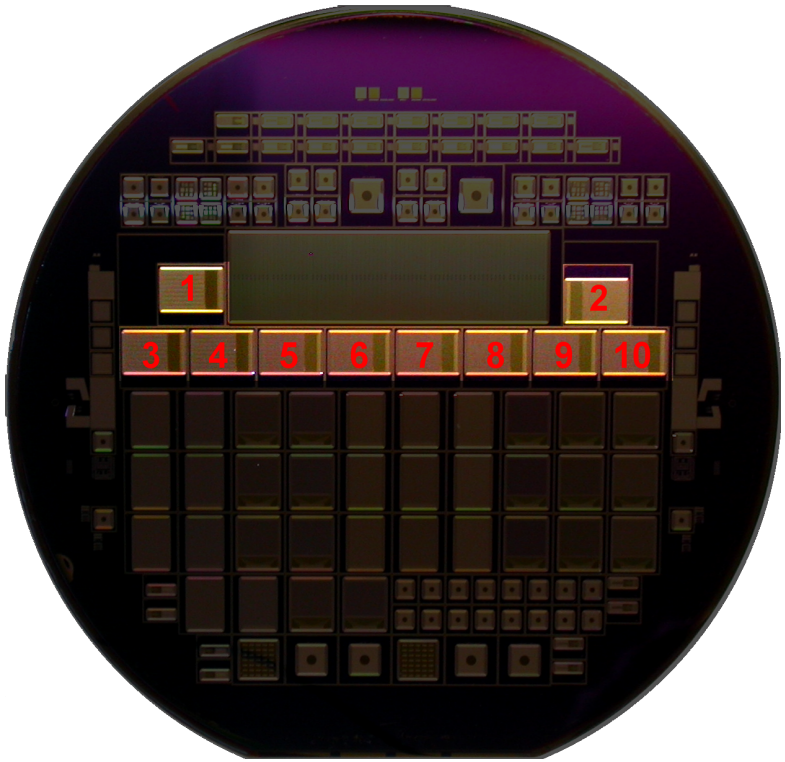


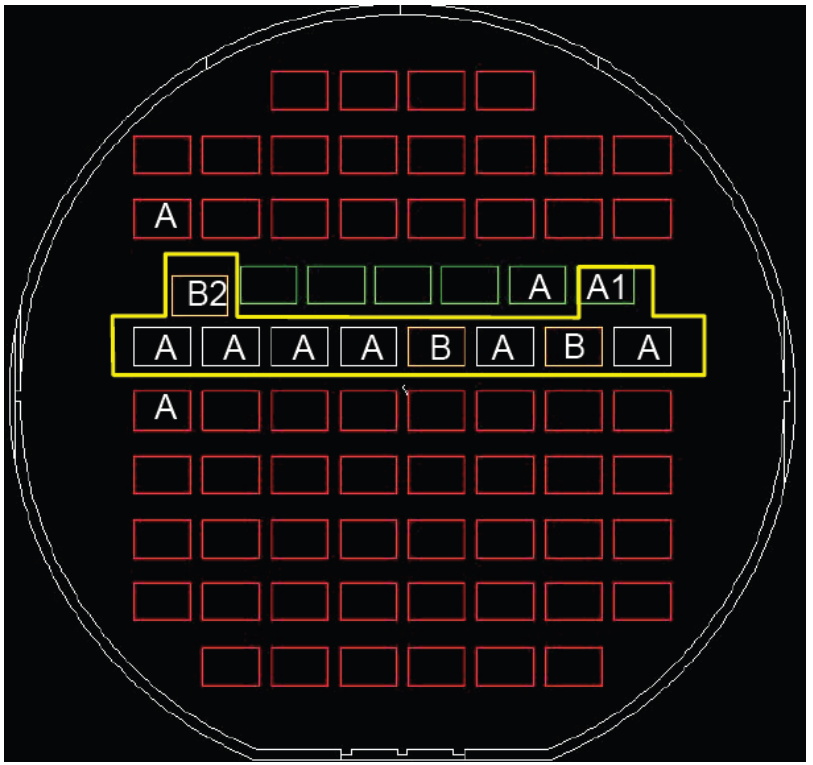
Experience with FE-I3 SLID Module

Chip to Wafer Interconnection

Challenge: Alignment precision of chips on handle wafer

The handle wafer has to be populated with chips, then both wafers have to be aligned

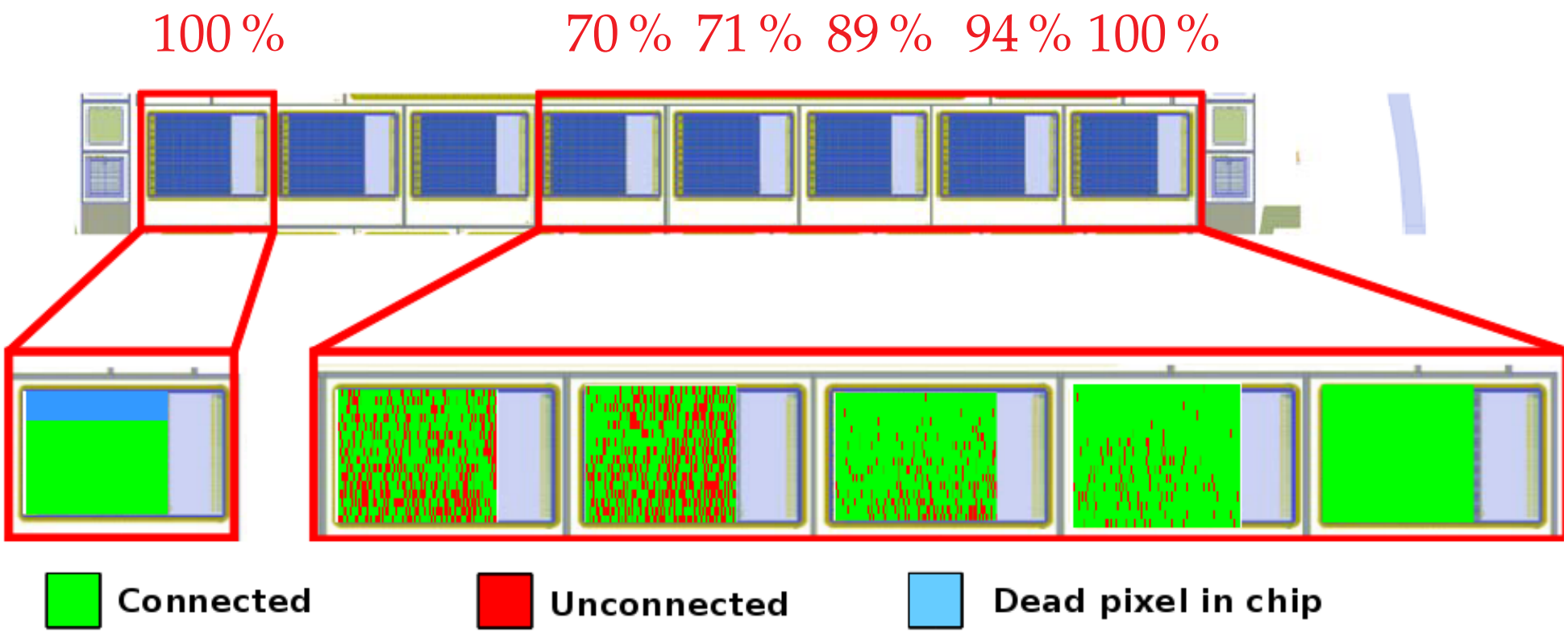




Pad size: $27 \times 60\,\mu\text{m}^2$ and minimal pad distance of $23\,\mu\text{m}$
Alignment precision is $\approx 10\,\mu\text{m}$ but rotations are also involved.
$\Rightarrow$ Solution could be the use of self-alignment.

Overview of the SLID Interconnection Efficiency

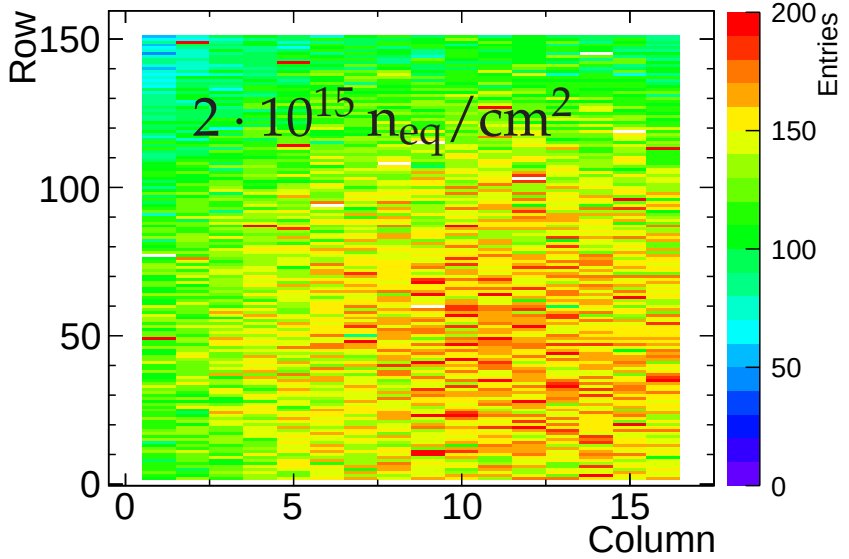
- Number of not connected channels is rising towards centre of wafer due to imperfect opening of the BCB. Not related to SLID, Solvable by SF_6 plasma descum.
- Stable after irradiation up to $2 \cdot 10^{15}\ n_{eq}/cm^2$ and thermal cycling (-50 – 20) °C.



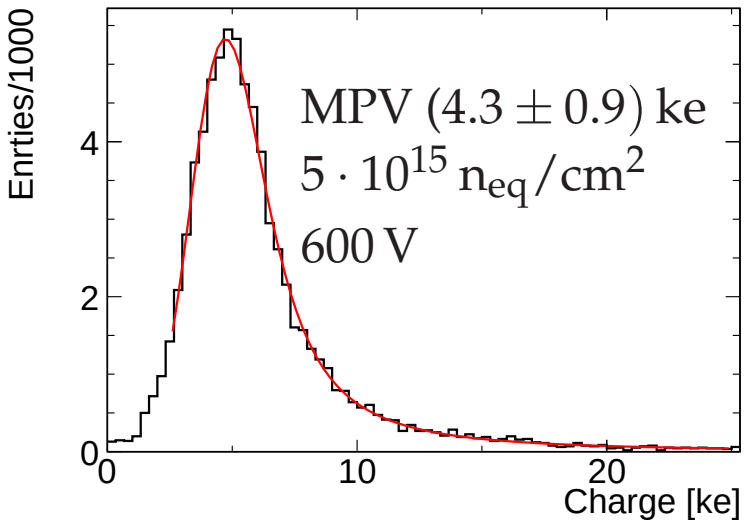
Charge Collection after Irradiation

- Irradiations
  - Ljubljana: $(2\,\&\,5)\cdot 10^{15}\,n_{eq}/cm^2$
  - KIT: $6\cdot 10^{14}\,n_{eq}/cm^2$
- Tuned threshold of 2500 e, Noise of 170 e
- Full charge recovered for all fluences

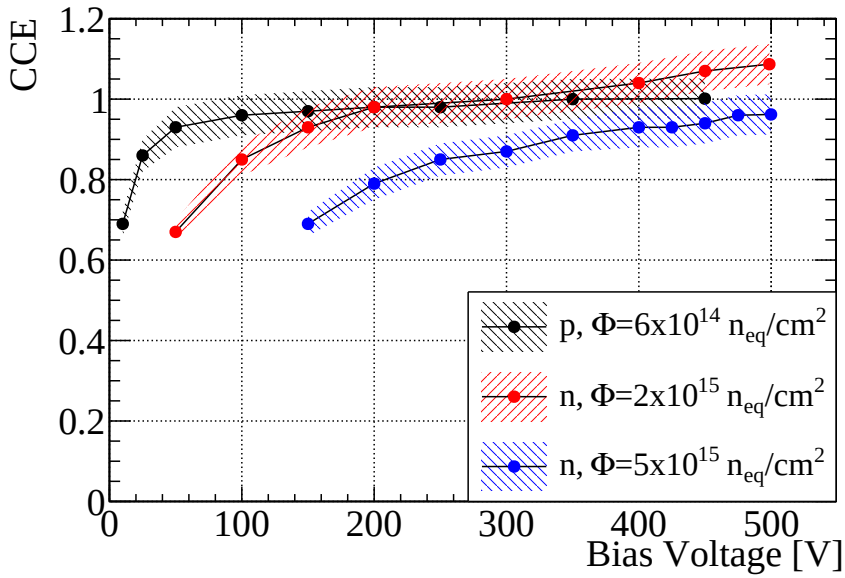
Hitmap



^{90}Sr Measurement

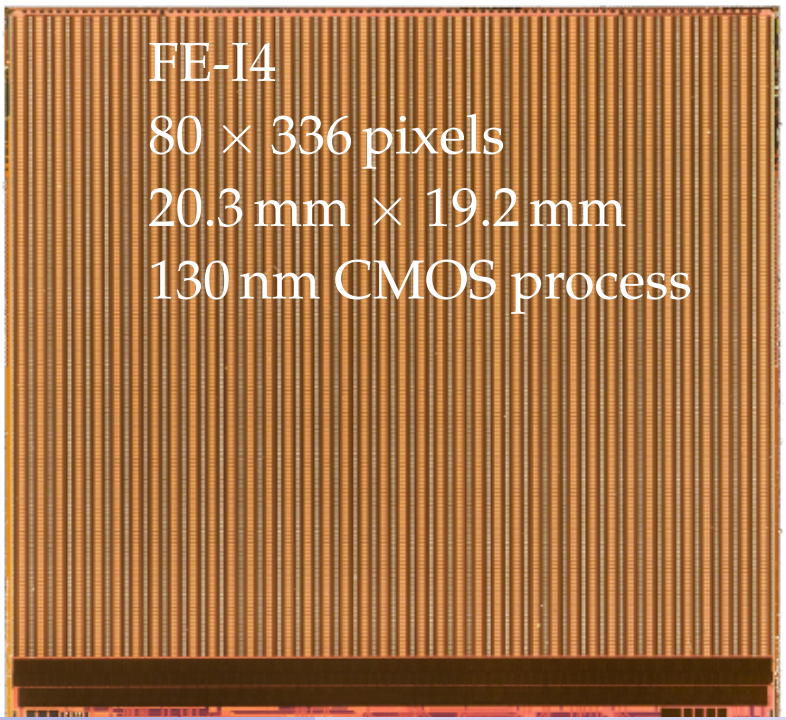


CCE



Status as of March 2012 (1)

- First wafers of the second chip version (FE-I4B) just coming back from IBM $\rightarrow$ 3 Wafers bought, available for R&D soon. FE-I4A wafers are already available for studies.
- The possibility to etch TSV from the backside to the first metal below the the wire bond pads has been foreseen in the design.
- New versions will be developed for post-IBL ATLAS pixel upgrades: 3D compliant?

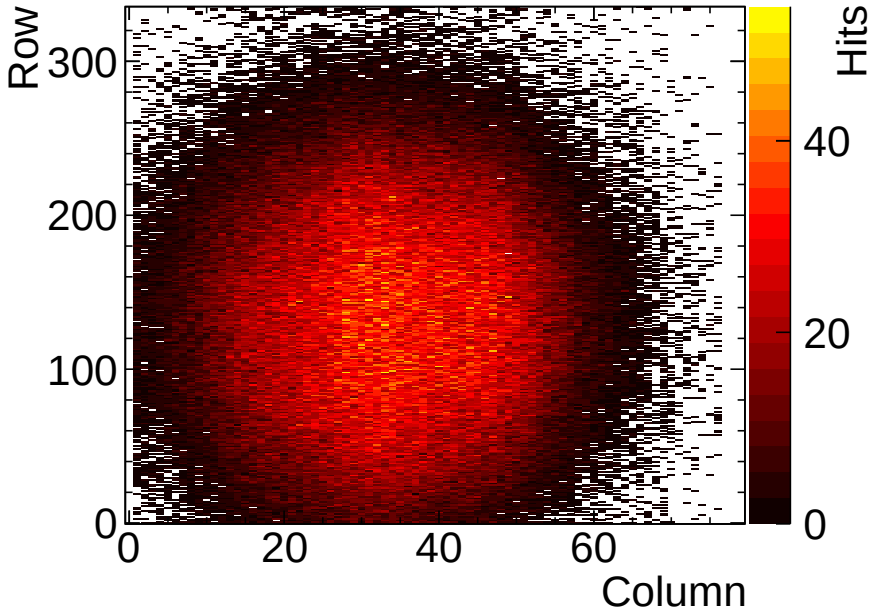


Status as of March 2012 (2)

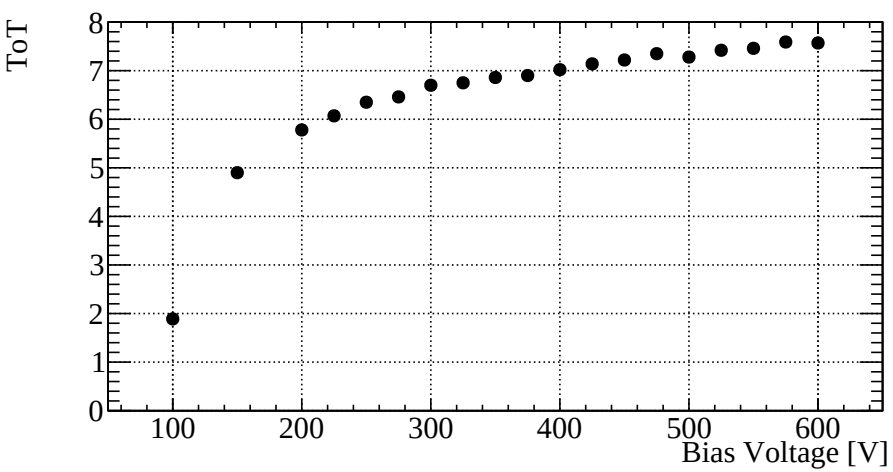
- Many FE-I4 modules built by now for IBL qualification and more generic R&D with different kinds of sensors
- Most of them interconnected with bump-bonding (IZM)
- The chip has demonstrated with all the different technologies excellent properties in terms of noise, threshold, radiation resistance

First data on n-in-p FE-I4 modules before and after irradiation available: 150 μm active thickness, produced at MPP/HLL, standard bump-bonding

Before



$2 \cdot 10^{15}$ n_{eq}/cm^2



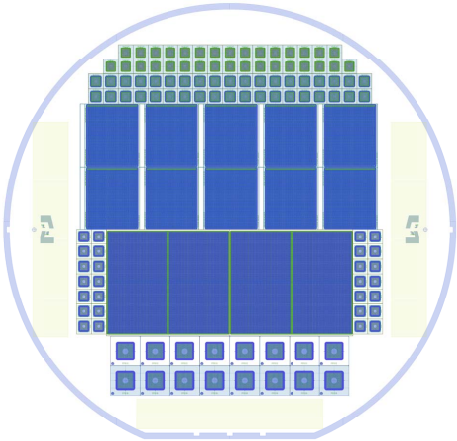
FE-I4 Compatible Sensor Production

Common Conditions

- n-in-p FE-I4 sensors uniformly distributed on 6" wafers ≈20 SCM
- 150-200 μm thickness

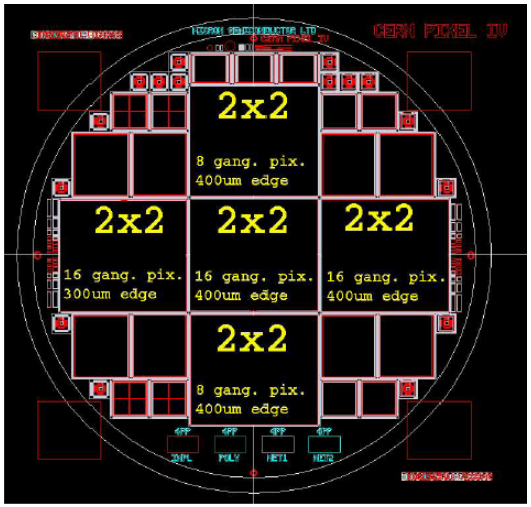
CiS

- Launching 6" line at the moment
- Already produced successfully n-in-p FE-I4 sensors



Micron

- Established production capability of n-in-p sensors on 6" line (down to 150 μm without handle wafer)
- Already produced successfully n-in-p FE-I4 sensors



Schedule & Finances

Time-line:

Step	From	To
Sensor procurement	Jul. 12	Sep. 13
TSV etching, ASIC wafer thinning and electroplating	Jul. 12	Nov. 13
Sensor wafer electroplating	Sep. 13	Nov. 13
SLID interconnection	Dec. 13	May 14
Evaluation	Jun. 14	Jan. 15

Cost:

Costs estimated from on-going projects with EMFT and CiS

Item	Cost
12 sensor wafer (masks & processing) at CiS	30 k€
3 FE-I4 wafers	7.2 k€
TSV & SLID (2 assemblies) by EMFT	150 k€

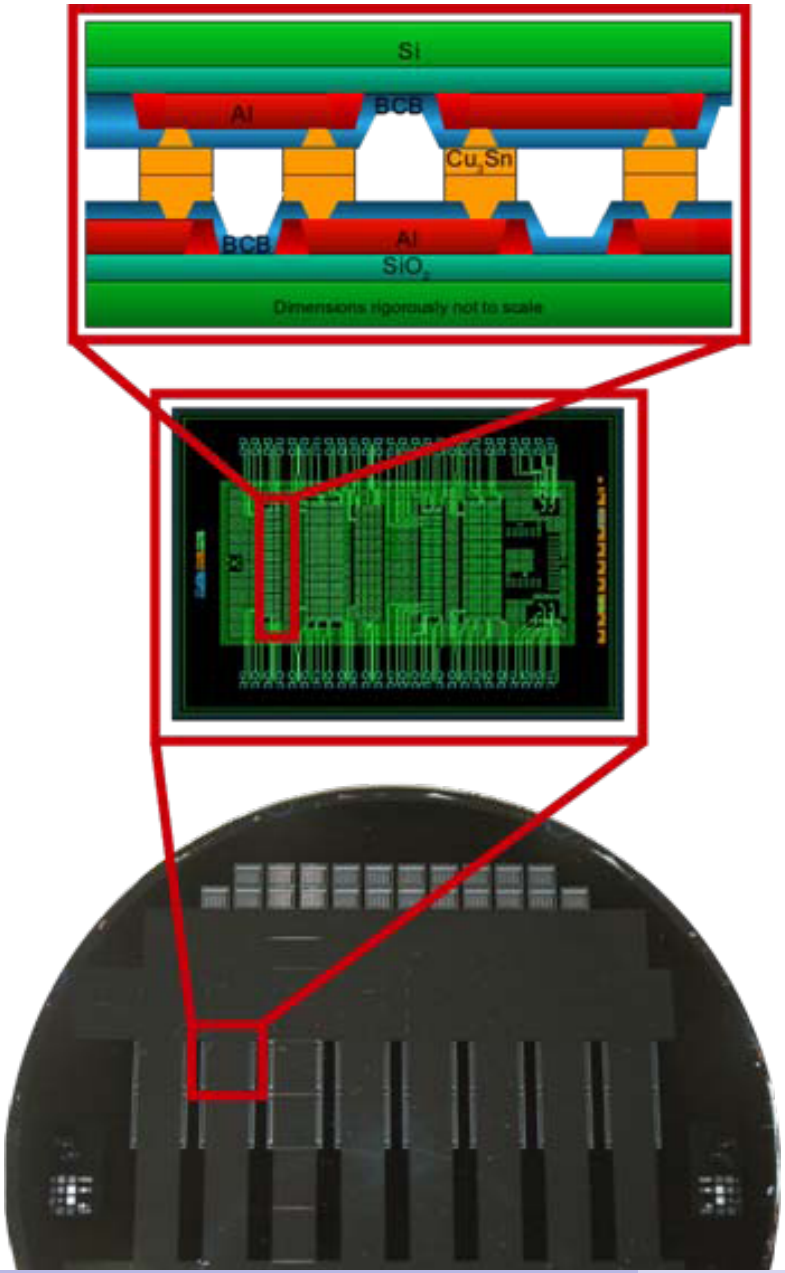
- In addition: 8 months of one FTE.
- AIDA WP3 contribution (60 k€ via MPP) covers partially fabrication & material.
- Rest funded by MPP, LAL, LPNHE, Glasgow, & U. Liverpool.

Testing Programme

- Different tasks shared among the five participating institutions:
  - Sensor testing before SLID preparation at EMFT
  - Electrical characterization of the FE-I4 modules with the USBpix system to determine:
    - SLID connection efficiency
    - Influence of TSV in terms of threshold noise
- Post-irradiation characterization of the devices, also through beam tests with the Eudet and TimePix telescopes
- Development and testing of a TSV quad module

BACKUP

Daisy Chains: Wafer-to-Wafer SLID



- Aim: Determine the feasibility of the SLID interconnection within the parameters needed for ATLAS pixels.
- Deliberate aplanarity were introduced to study the sensitivity $\rightarrow$ Up to 1 μm aplanarities do not affect efficiency.
- SLID efficiencies measured with daisy chains (wafer to wafer connections).

Pad width in μm^2	Pitch in μm	Aplanarity	SLID inefficiencies
30×30	60	0	$< 1.2 \times 10^{-4}$
80×80	115	0	$< 8.9 \times 10^{-4}$
80×80	100	0	$< 7.8 \times 10^{-4}$
27×60	50, 400	0	$< (5 \pm 1) \times 10^{-4}$
30×30	60	100 nm	$< (10 \pm 4) \times 10^{-4}$
30×30	60	1 μm	$< (4 \pm 3) \times 10^{-4}$

Connection Strength

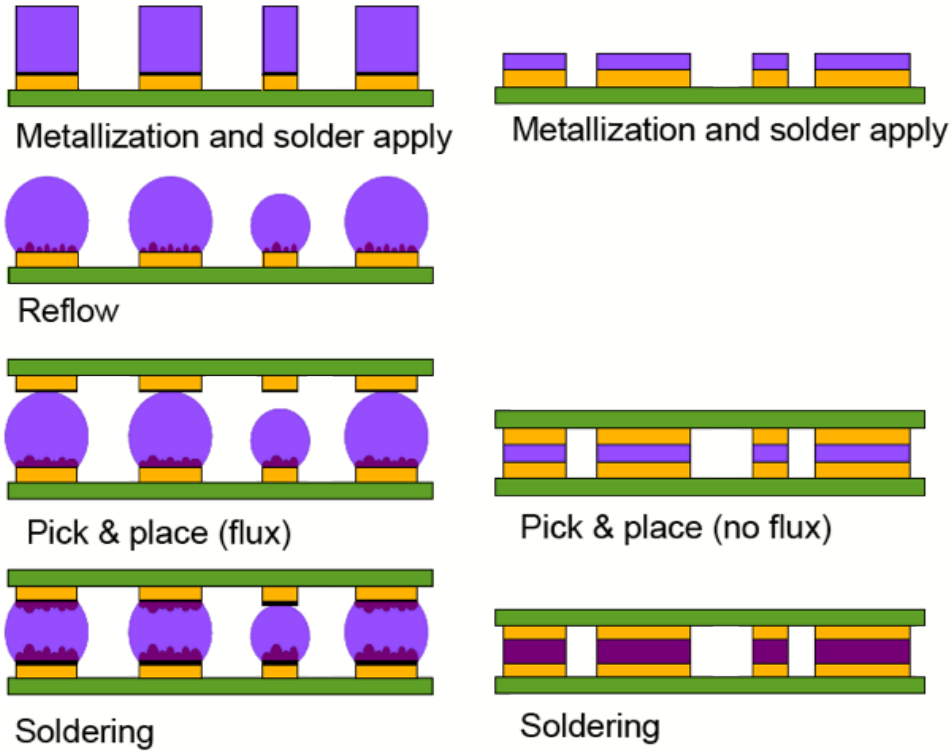
The chips of the lower half of the wafer are pulled off to:

- get an idea of the connection strength.
- see if there are systematics, hinting to problems in the process.

Findings:

- Order of 0.01 N per connection. similar to other interconnection technologies.
- There is no clear correlation between strength and alignment (extreme cases not considered).
- Caveat: Underlying structures are not homogeneous.

SLID vs. Bumb Bonding

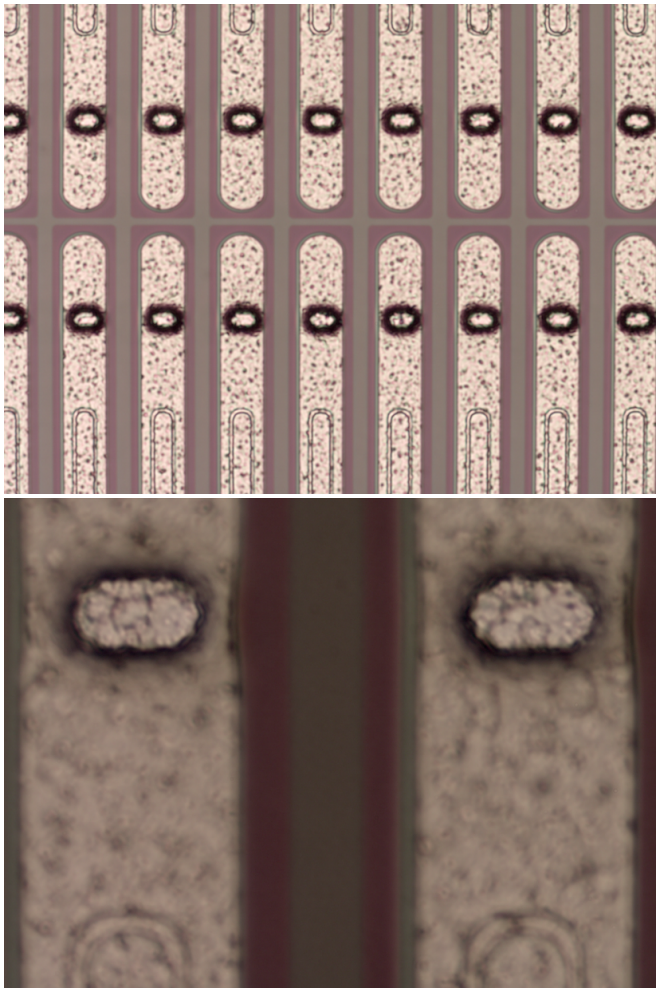


1. Apply metal layer to sensor and chip.
2. For bump bonding, the sensor is heated such that the solder-metal layer melts and become ball like. Smaller pads result in smaller balls (less material).
3. Chip and sensor a brought together.
4. The stack is heated. For bump bonding smaller balls cannot form a good connection.

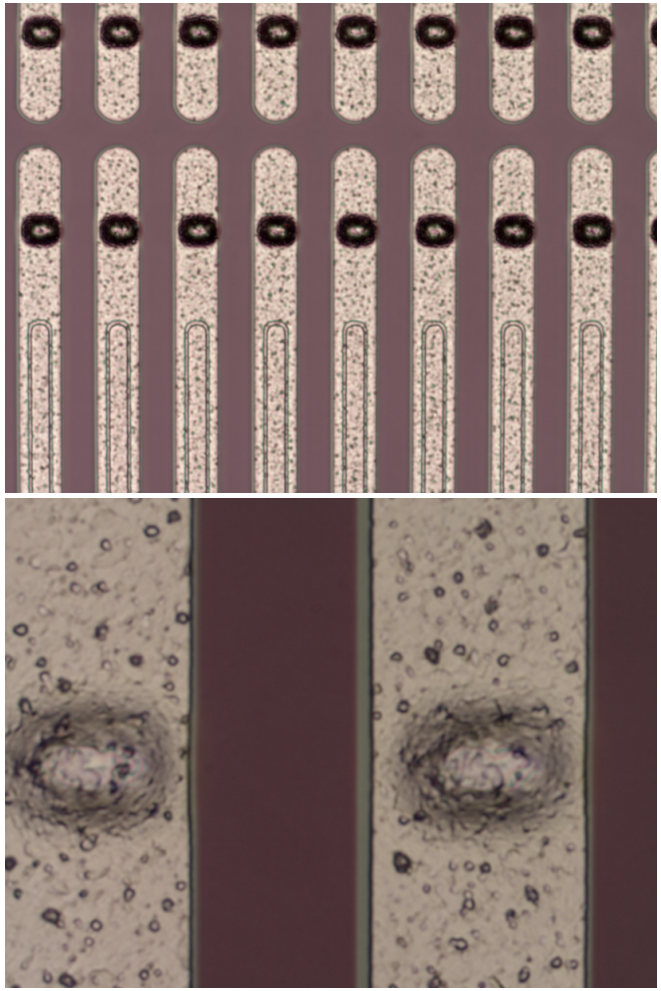
Cause: BCB-Imperfections

The BCB has to be opened to allow for the contact between chip and sensor.
This operation did not fully succeed.

Good



Bad



Solution: Plasma descum process with SF_6