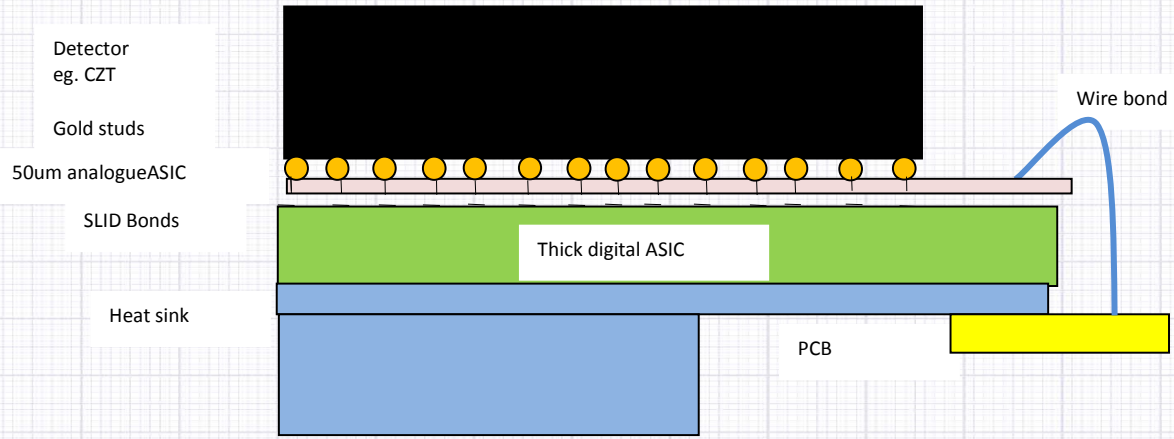
Uppsala plans for WP3.2

- Uppsala has joined the RAL/STFC effort
- The goal is to make a 4-side buttable pixel tile based on a 2-tier ASIC development by the RAL group.



Images courtesy of RAL/STFC. For more details, see presentation by P. Seller at AIDA WP3 meeting October 4. 2011

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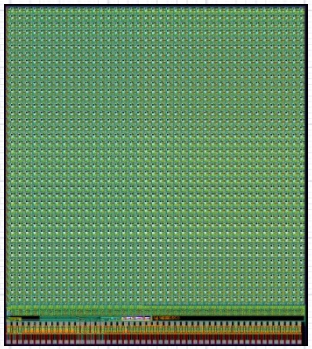
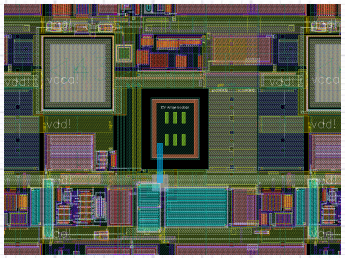
ASIC - 4040 pixel ASIC

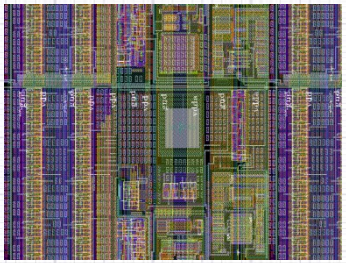
- RAL has developed a 2-tier ASIC for 3D integration
  - Tier 1: Analogue, 1600 pixels
  - Tier 2: Digital ADC



4040 ASIC



3D upper layer



3D lower layer

- Status: ASIC are tested and they work

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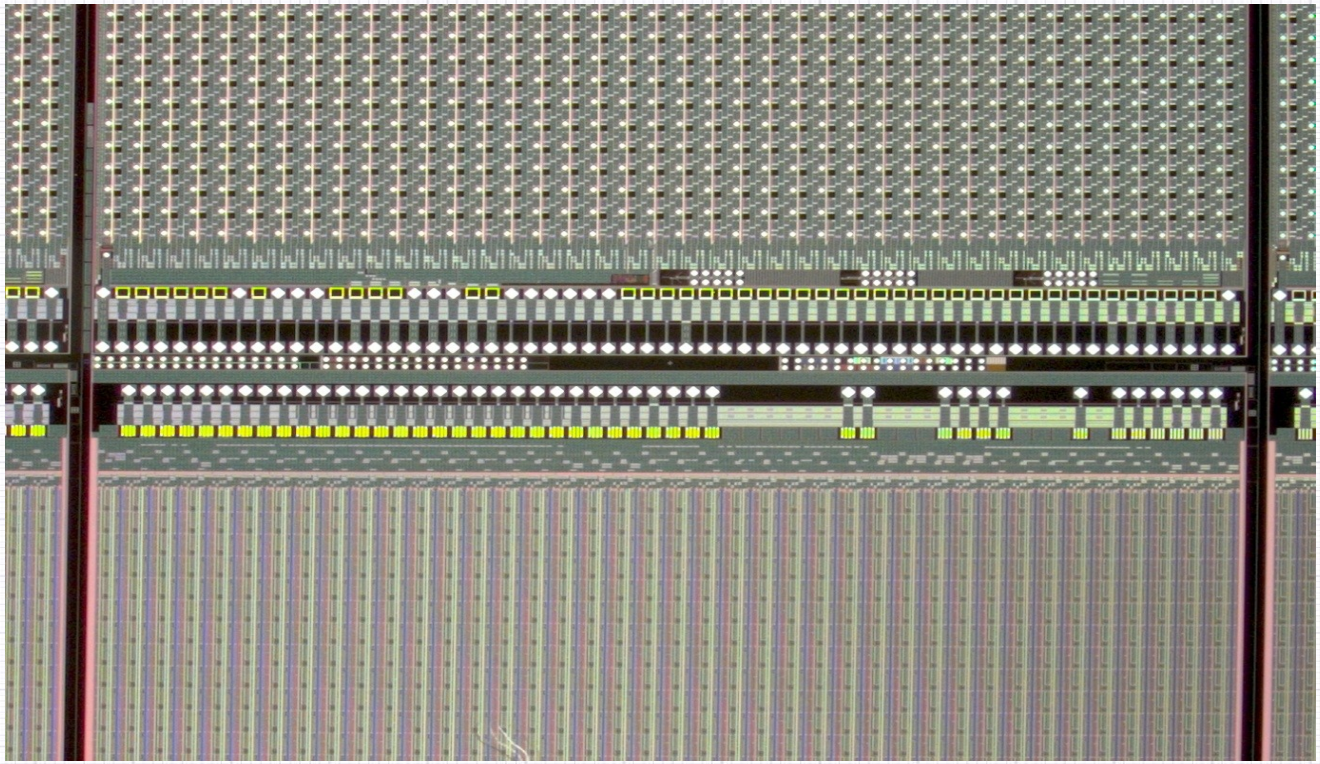
3D preparation

- Contract for making TSV on analogue was placed already last year and wafers have been shipped
- Meeting with EMFT for discussing SLID interconnection in April



Upper layer

Lower layer

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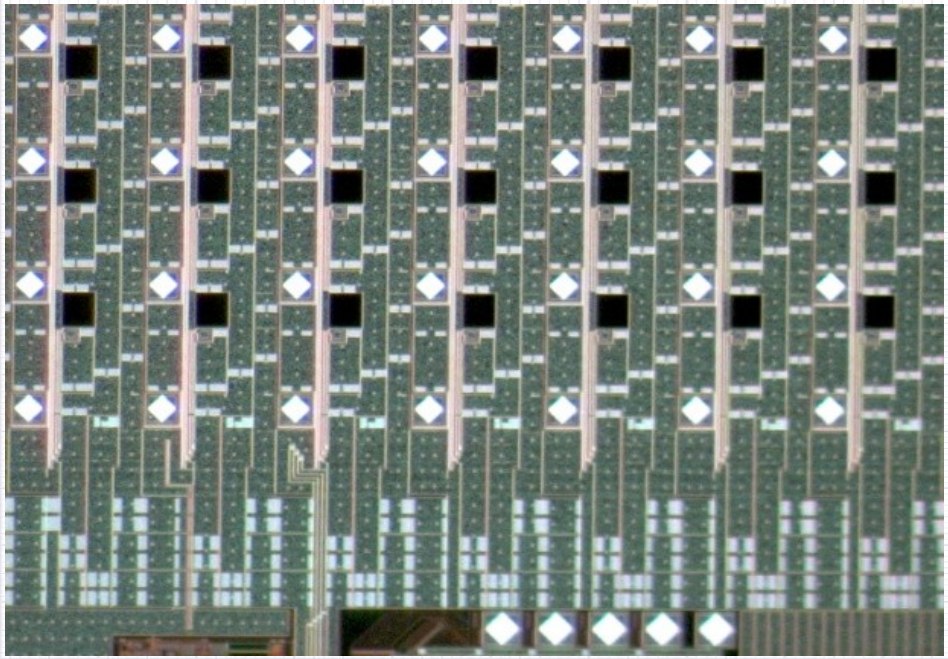
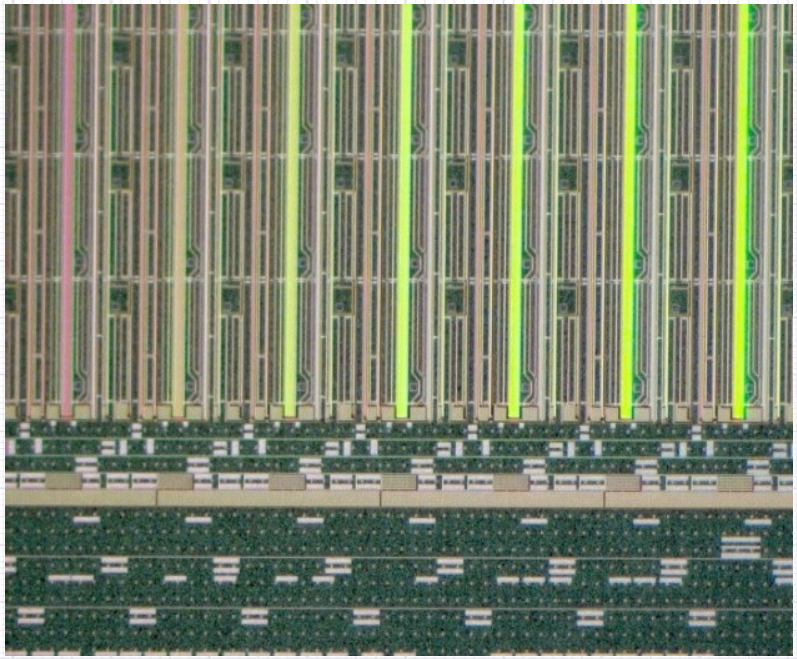
Collaboration and AIDA





Zoom-in on ASIC showing the TSV regions

- Uppsala and RAL will meet in May to discuss format and details of future collaboration
- The project need to be formalised in AIDA