



AIDA-WP3

Status and Plans @PM12

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Goal: increase FF with 3D stacking of APD arrays

- 1) Pixel design
- 2) Plans for the next Tezzaron run
- 3) Alternative solutions



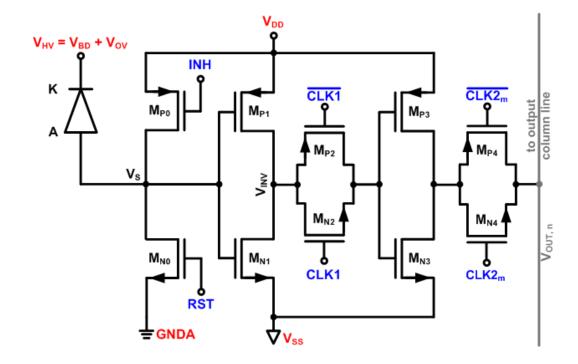






Pixel design: Pixel schematic

- Powering → V_{HV} & GNDA (sensor), V_{DD} & V_{SS} (electronics)
- Control signals → INH & RST (sensor), CLK1 (transmission gate to enable readout electronics), CLK2 (transmission gate to enable output column line)



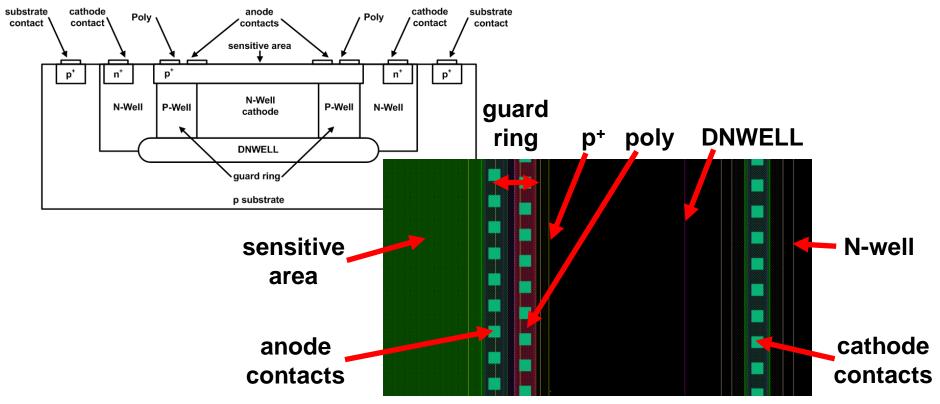






Pixel design: Sensor layout

- The deep-submicrometer SPADs are more noisy due to the presence of STI (amongst other factors).
- It is possible to physically separate the STI interface from the SPAD multiplication region using a polysilicon gate that represents a stop mask for n⁺ and p⁺ implantations.



C. Niclass, A Single Photon Avalanche Diode Implemented in 130-nm CMOS Technology, IEEE J. Quantum Electron. (2007).



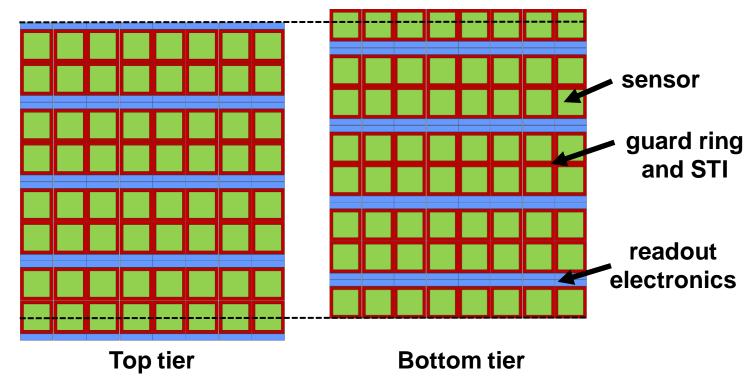






1) Identic top and bottom tiers. Rows vertically flipped.

- The top and bottom tiers are displaced to maximize the FF
- Sensor size \rightarrow 20µm x 20µm in both tiers
- \circ FF \rightarrow 93%











2) Sensor & electronics (top tier), sensor only (bottom tier).

o Bottom tier sensitive areas overlapped with top tier death areas

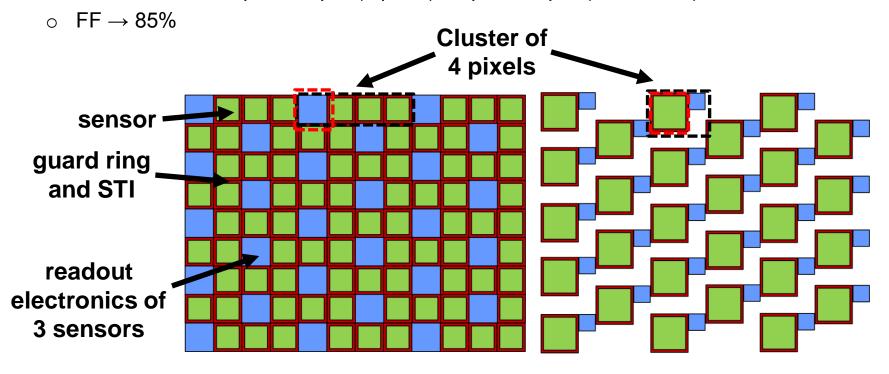
Sensor size \rightarrow 8µm x 8µm (top tier), 20µm x 30µm (bottom tier) Cluster of \circ FF \rightarrow 96% 5 pixels sensor guard ring and STI readout electronics of 5 sensors Top tier **Bottom tier**







- 3) Similar idea, with reduced pixel size and sensor & electronics in both tiers.
 - Sensor size \rightarrow 18µm x 15µm (top tier), 23µm x 20µm (bottom tier)



Top tier

Bottom tier

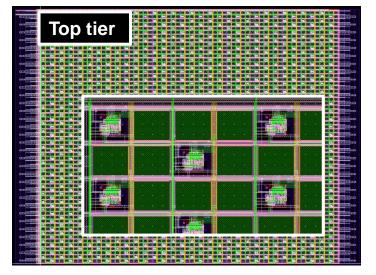


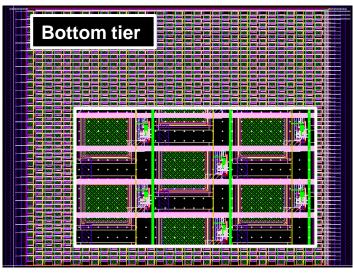


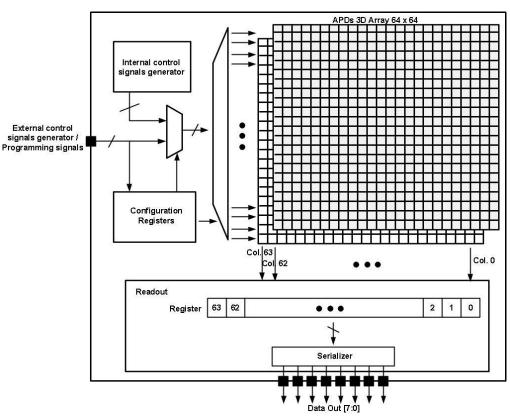




Plans: Top&Botom tiers, ctrl and RO.







The plan is to send the design for the Tezzaron run via CMP 20th September 2012

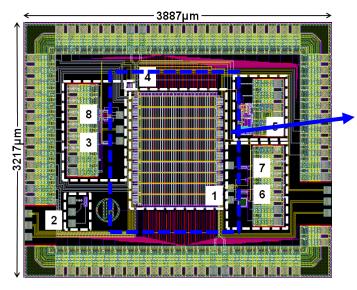








Alternative solutions: HV-AMS



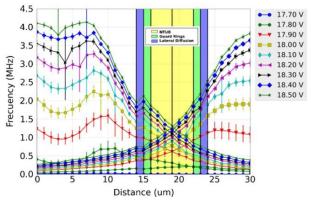
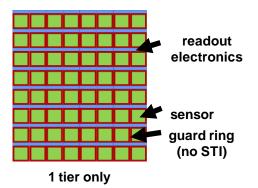


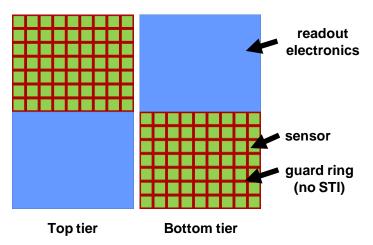
Fig. 16. Detection frequencies measured by scanning a 30 keV electron beam onto two neighbouring pixels in the array.

A. Vilà, Characterization and simulation of Avalanche PhotoDiodes for next-generation colliders, Sens. Actuators, A (2011).



In 0,35um HV-AMS with our pixel structure the ring is sensitive
→ c.a.100% FF with 2 tiers seems feasible

1) sensor&readout in both tiers:



2) Or, sensor on top tier and electronics on bottom tier



