WP 9.5 task analogue HCAL

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AIDA kickoff meeting
16-18 Feb. 2011, CERN

The Goal

Advance tungsten as a realistic alternative to steel for the absorber structure of the hadronic calorimeter of the future linear collider detector

- Validate shower simulations for tungsten
  - stronger role of neutrons than in iron
  - to be done with scintillator and gaseous devices
- Gain engineering experience with tungsten
- Develop electronics integration solution for a very compact HCAL
- Study timing issues
  - physics: signals from delayed de-excitations
  - algorithms: tag neutron signals
  - operation: time stamping for background rejection

The group structure

CERN optical test stand to assess time-stamping capabilities of active readout
engineering of tungsten absorber structure

MPI M test stand with a radioactive source for characterization of scint. tiles

LAL highly integrated ASICs with independent ch.-by-ch. trigger and read-out

U.Hei. SiPM ASIC (cooperation with LAL) with improved ToF measurements

DESY multi-layer system integration, compact DAQ, calibration and power supply interfaces, and cooling

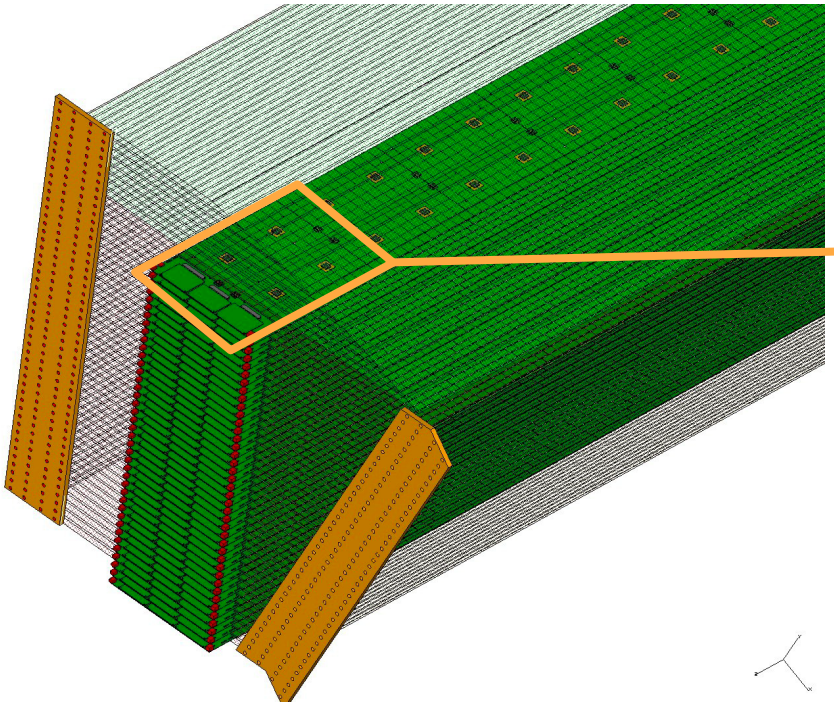
U.Wup. scalable LED-Calibration system (collaboration with Bergen)

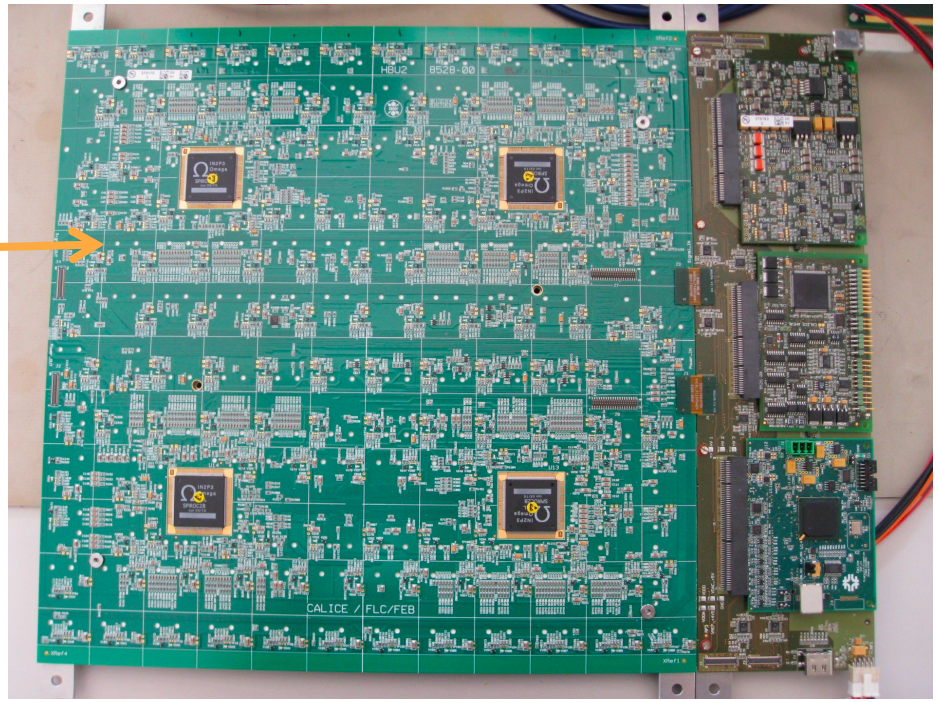
Prague adaptive power supply system with temperature compensated bias voltage (collaboration with Bergen)

Bergen SiPM voltage adjustment procedure and adaptive power supply

Entering new: Uni. Mainz, Uni. Hamburg

AHCAL structure





Signal sampled by scintillating tiles
→ 3x3x0.3cm^3, 2592 tiles per layer

Long term:
Establish mass test of tiles
Develop multi-layer DAQ
Integration of electronics

Short term:
commission HBU (tiles, ASIC, LED)
4-HBU test in hadronic shower
4D hadronic shower study

Test beam – First MIP results

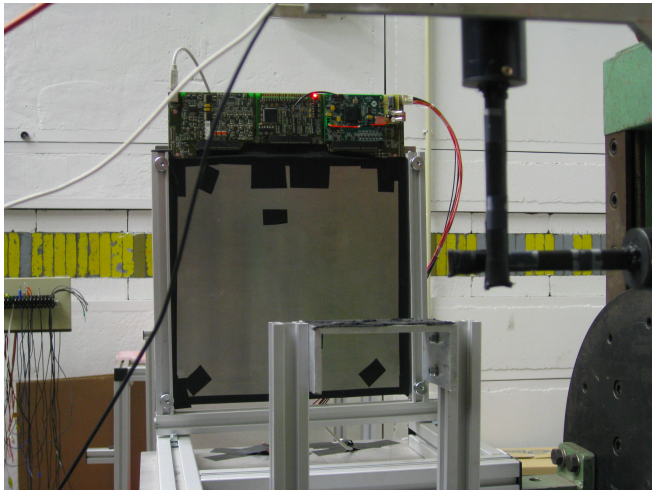
HBU2 in DESY test beam

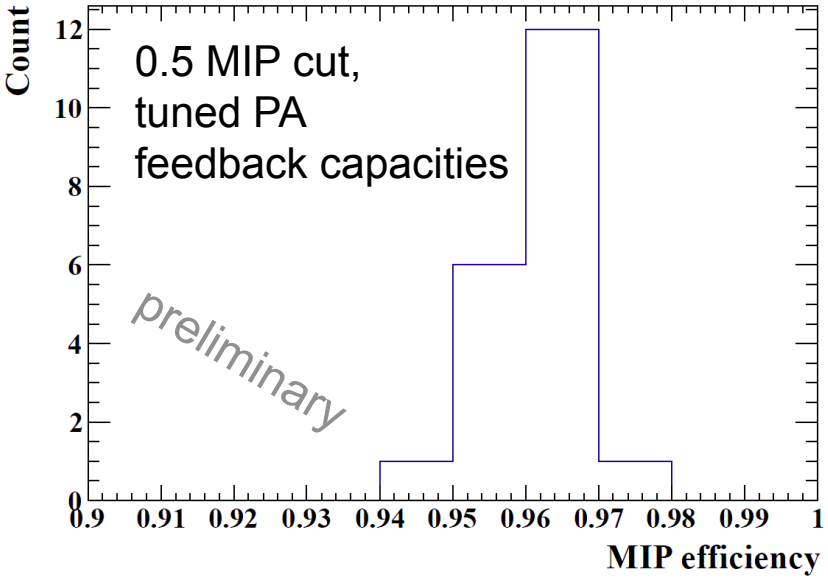
- Test functionality in test beam environment
- Measure MIPs with 2 GeV electron beam

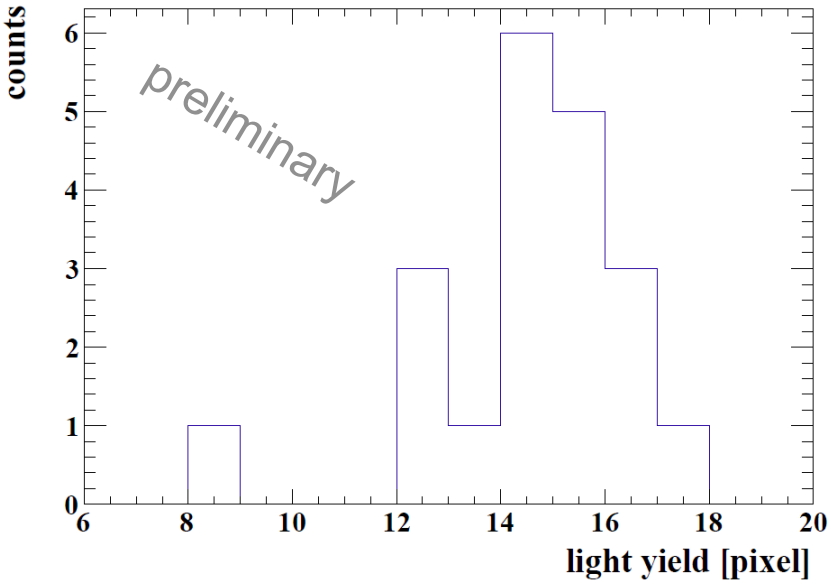
  → ~15 pixels per MIP
- Test channel-wise gain and autotrigger

adjustment and **optimize MIP efficiency**

→ Good results





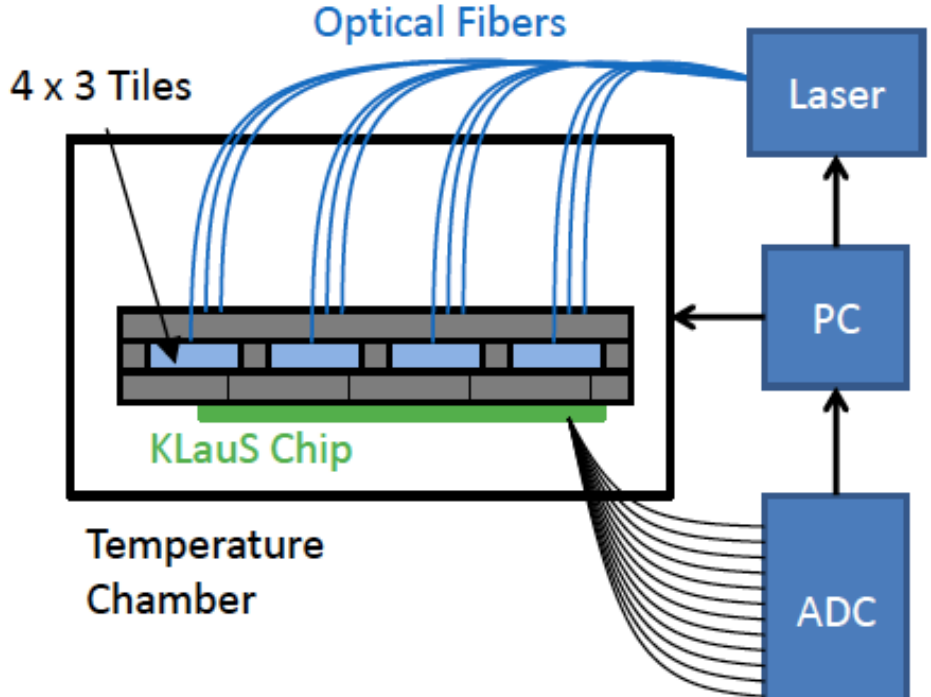


Mass test of tile production

450 + 470 tiles delivered to DESY of which 144 tiles to Heidelberg for characterization
➔ Enough for 4 HBU

Heidelberg

- Automated measurement with 12 tiles in parallel
- Picosecond laser with 12 optical fibers
- Readout with KLauS Chip + ADC
- T=10°C – 34°C (in ca. 3.5 hours)
  - ⇒152 tiles in 5 days
- SPS vs. V_{bias} @ fixed I_{Laser}
  - ⇒Gain
  - ⇒V_{break}
  - ⇒Response
  - ⇒Cross-talk & after-pulses
  - ⇒Dark-rate



New HCAL Base Unit (HBU2)

- 4 **new HBUs** in DESY lab

  → 70 channels equipped with scintillator tiles, LEDs, SiPM readout, 4 ASICs
- 1 HBU2 connected to DAQ modules for first tests

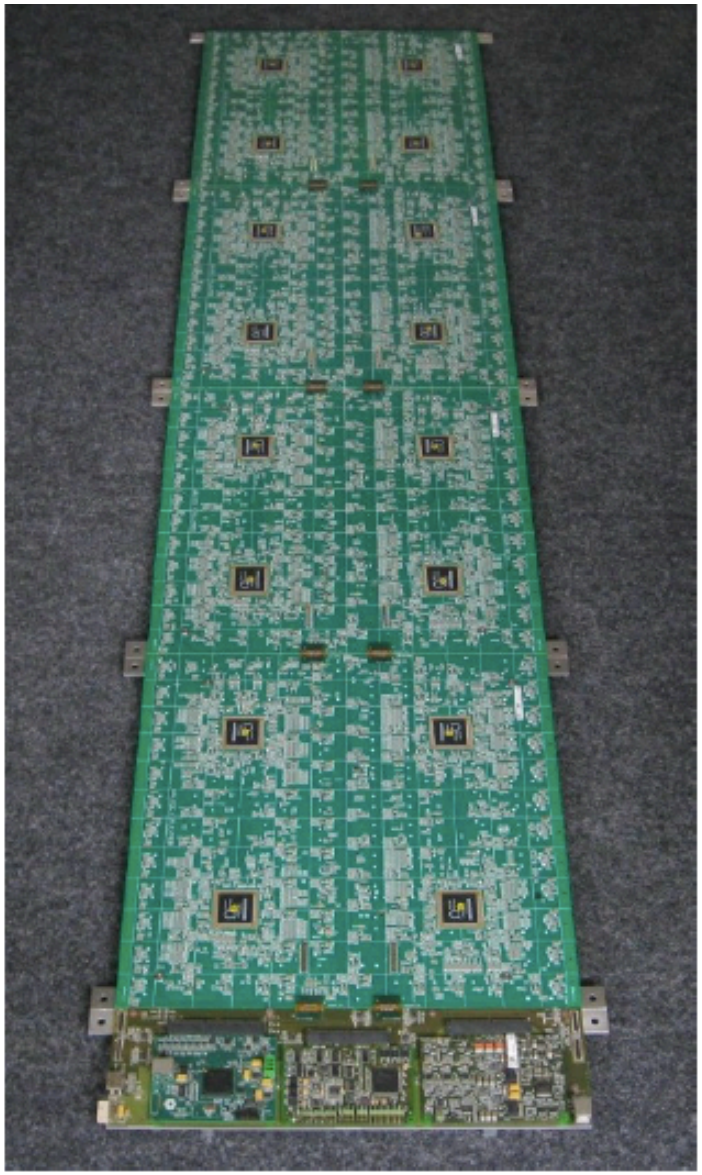
  → so far fully functioning!
- 1 HBU2 in **DESY test beam**
- We ordered 6 new HBU2s for **full slab test**:

  → Quality of electrical signals

  → Mechanics, temperature

  → DAQ

Build small stack with ~10 layers, 1 HBU each?



Power pulsing

DESY

- Concept of power pulsing already tested on ASIC test bench

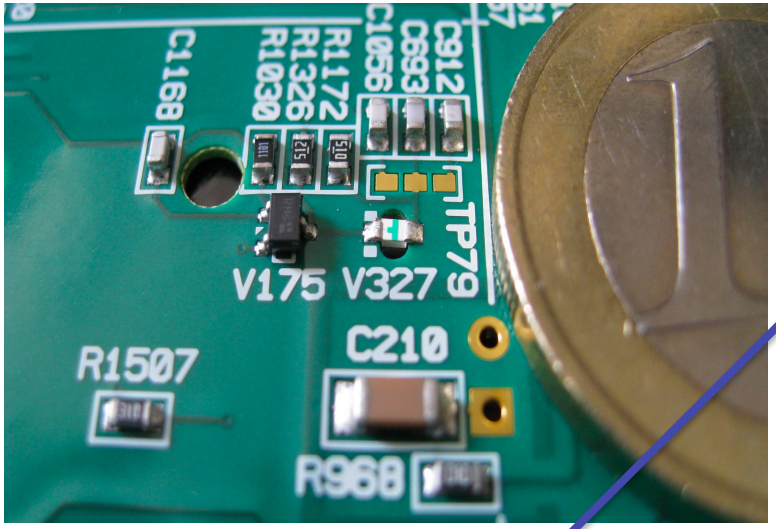
  → Working so far, but has to improve

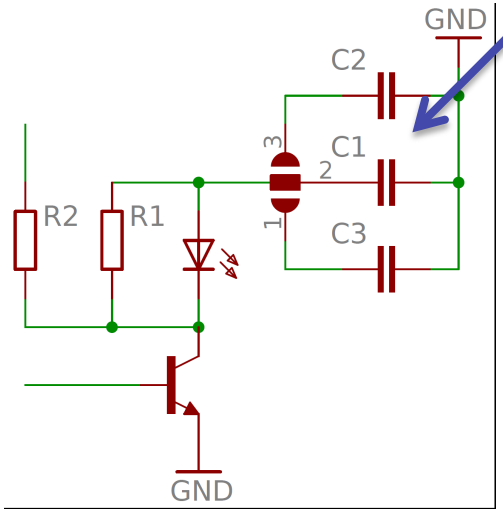
- Need to verify power distribution and signal integrity in larger system

  → **Use multi-HBU setup** (2012)

- **Validate heat dissipation calculations** with realistic steel plates (2012)

LED calibration system





Wuppertal solution:

Light directly coupled into tile by 1 integrated LED per channel

Light output equalization via C1 – C3 (default: 150pF, plus: 22pF, 82pF)

New design implemented in HBU2 and is currently tested extensively

Prague solution:

Light coupled into tile by notched fiber

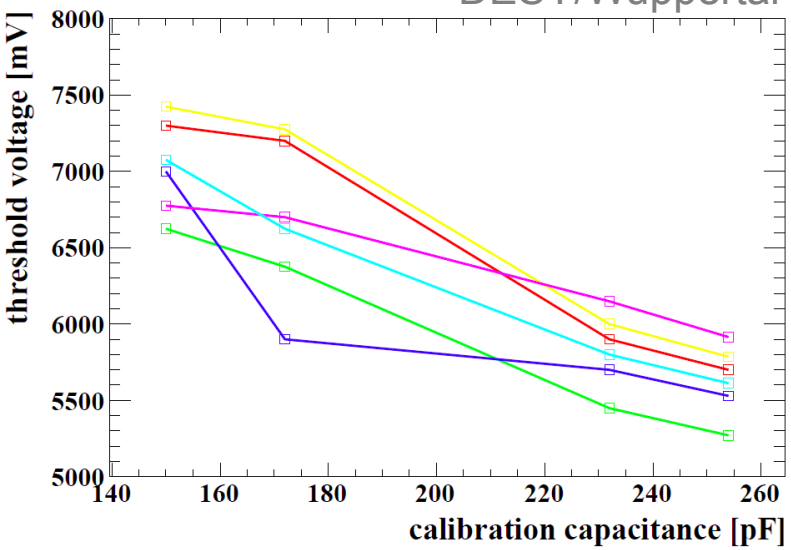
Mechanical integration difficult

→ First tests performed in DESY lab with new electronics and new tiles

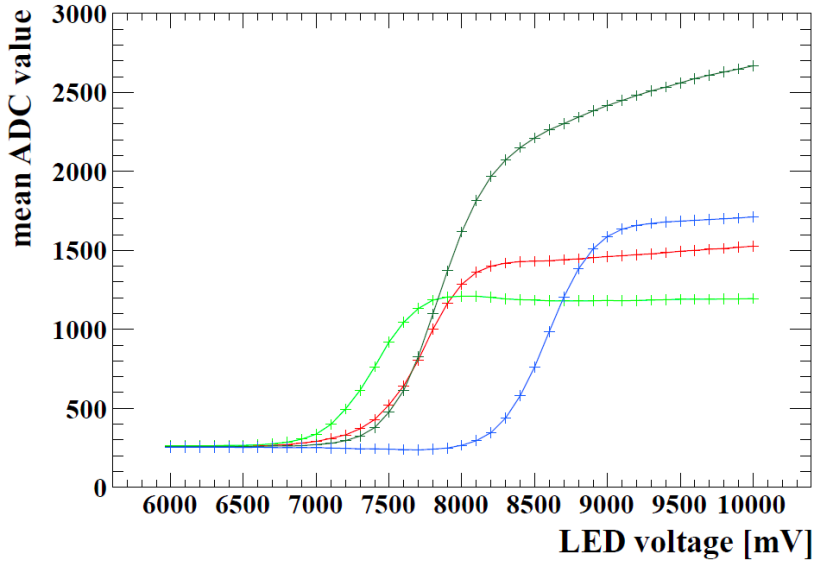
Embedded LED calibration system

DESY/Wuppertal

LED light output equalization:
4 bias capacitor combinations tested:
→ 150pF, 172pF, 252pF and 254pF
Measured minimum voltage to produce LED light
→ Improvement of LED uniformity possible!



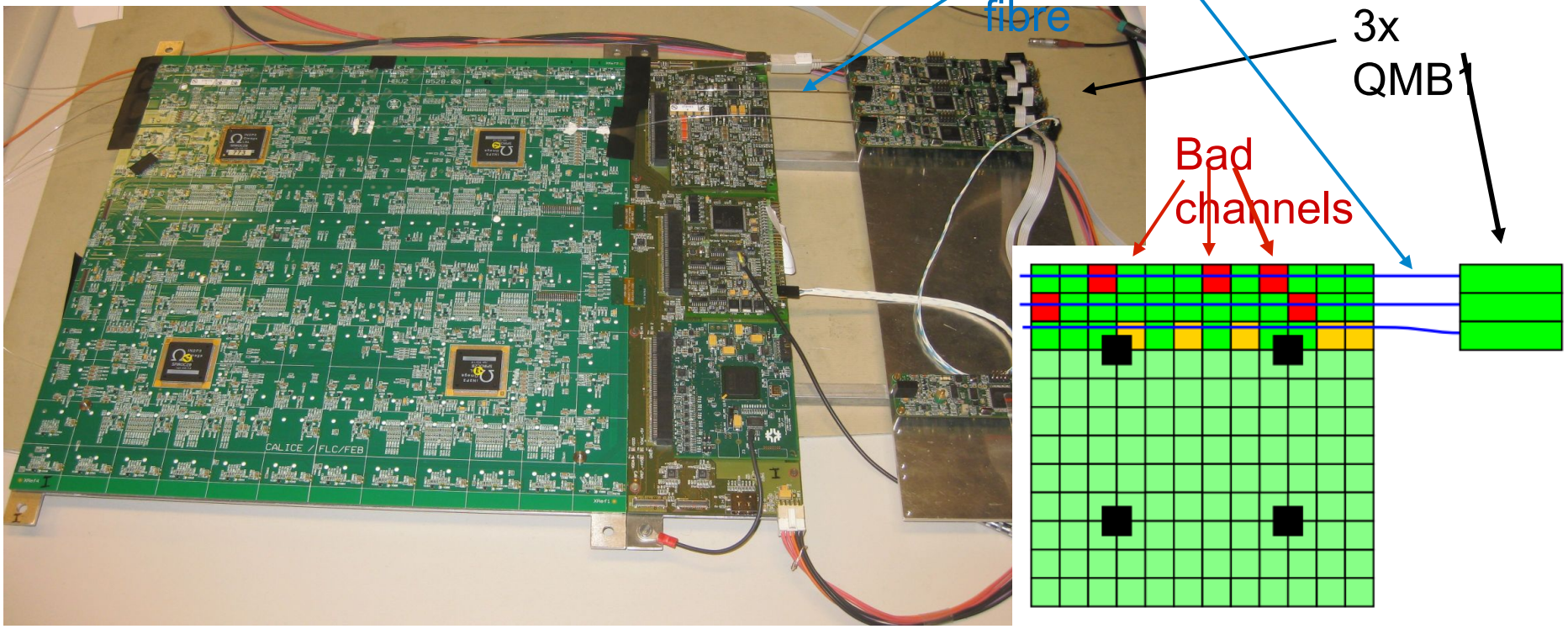
SiPM saturation:
SiPM saturation can be seen with the integrated LED system



Combined test with HBU2 and QMB1

Prague

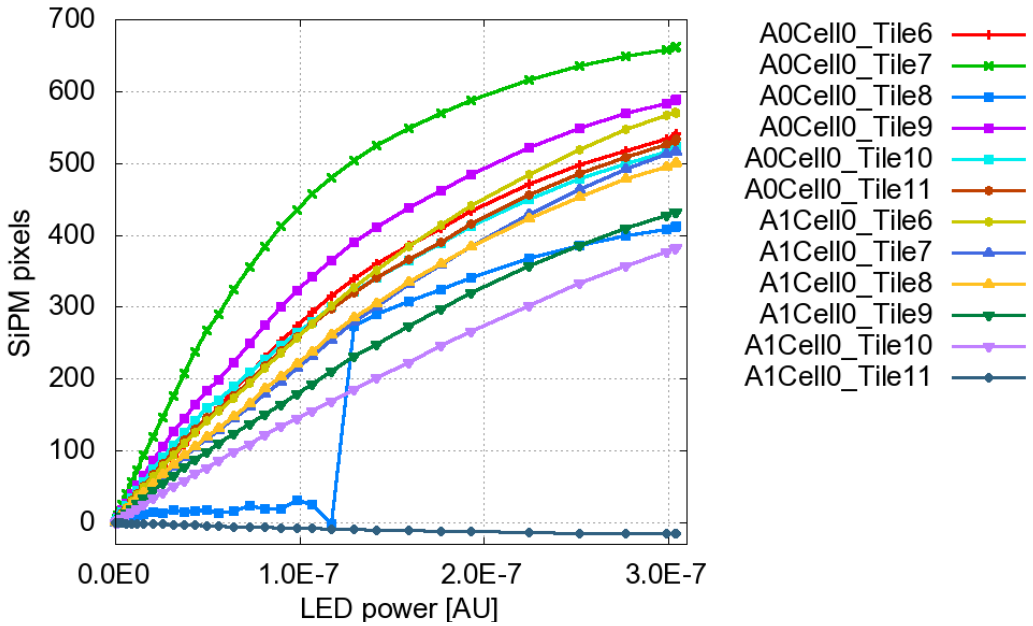
- HBU2 (two SPIRoc2b ASICs) equipped with 3 rows of scintillators with SiPMs (delivered in Nov2011)
- 3 active QMB1s 3mm UV LED (395nm)
- Tested with new notched-fibre prototypes (semi-automatic production)

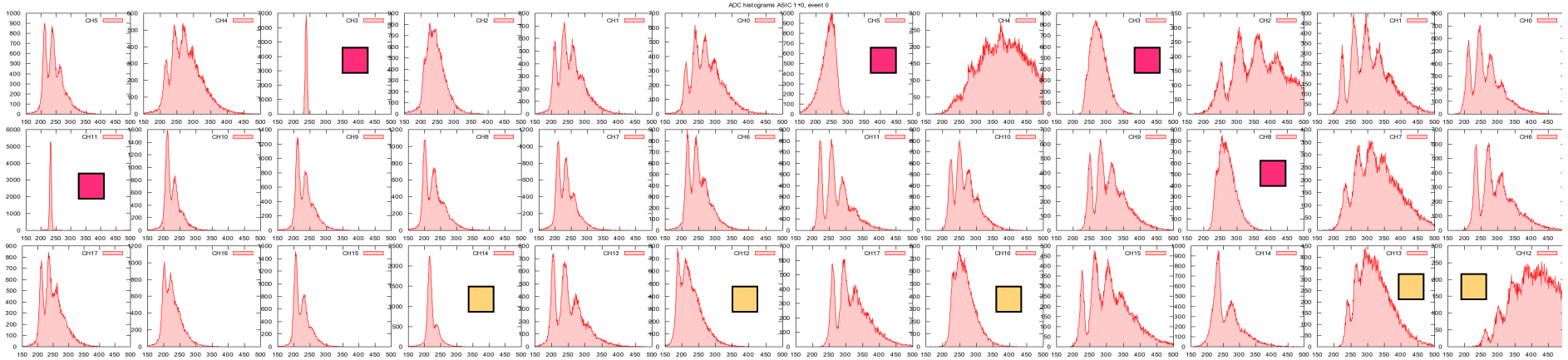


Results

Prague

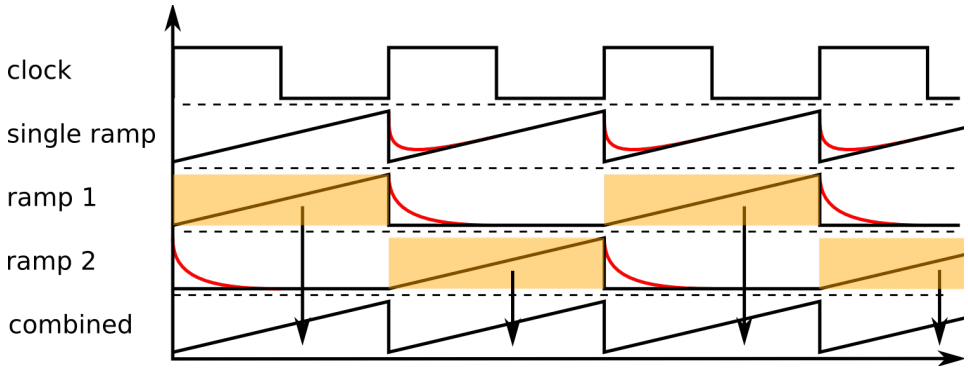
- **Single Photo-electron Spectrum** obtained for all channels by a single run
- **Saturation** of the SiPM observed

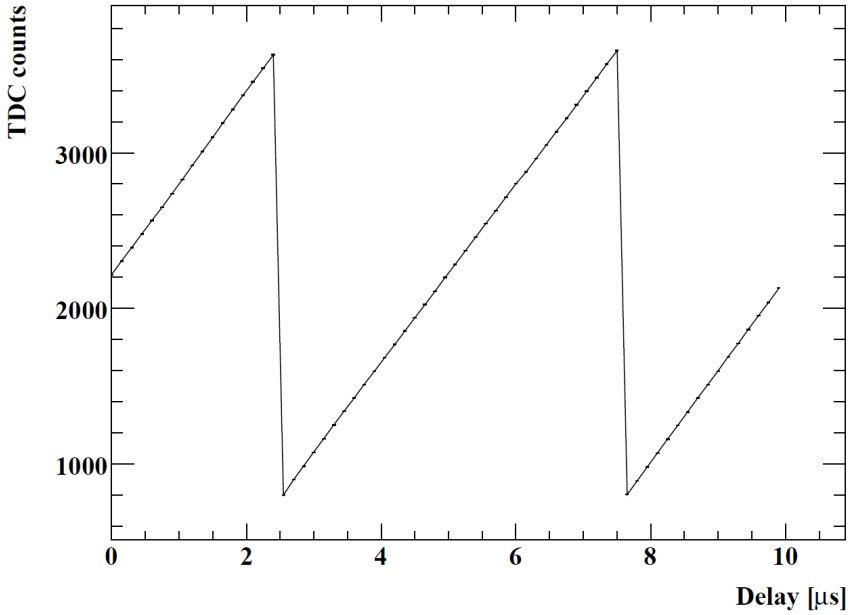




SPIROC 2 - time measurements

DESY/LAL





SPIROC2b measures time in auto-trigger mode relative to bunch clock

→ 2 ramps to reduce deadtime due to ramp reset
→ ILC mode = 200ns ramp, testbeam mode = 5µs ramp (less dead time)
→ Investigate time resolution to optimize ramp slopes (and lengths)

→ time resolution of ASIC tested:
ILC mode = 300ps,
testbeam mode = 1-2ns

Simulation

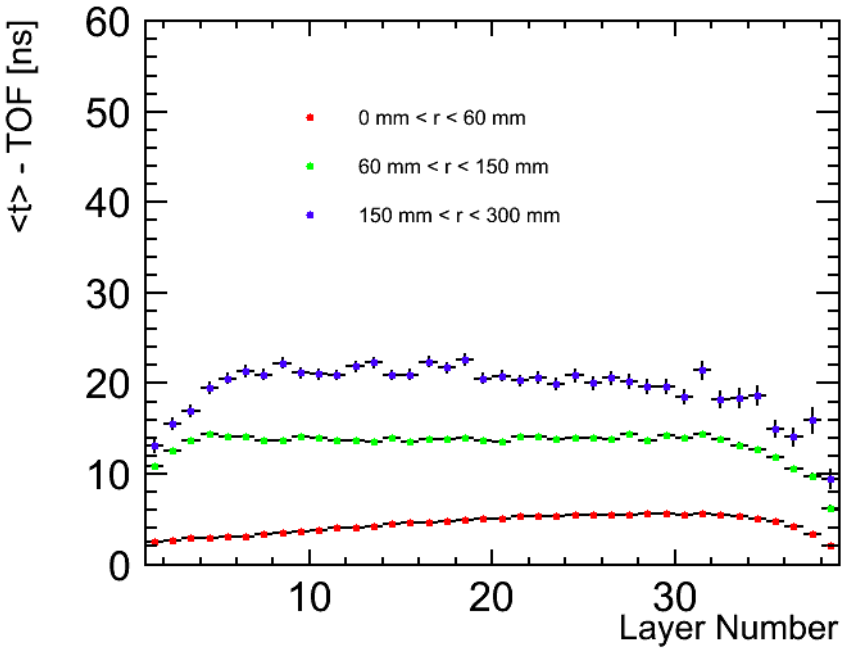
Implementation of time information in simulation done ✔

Digitization is currently under development

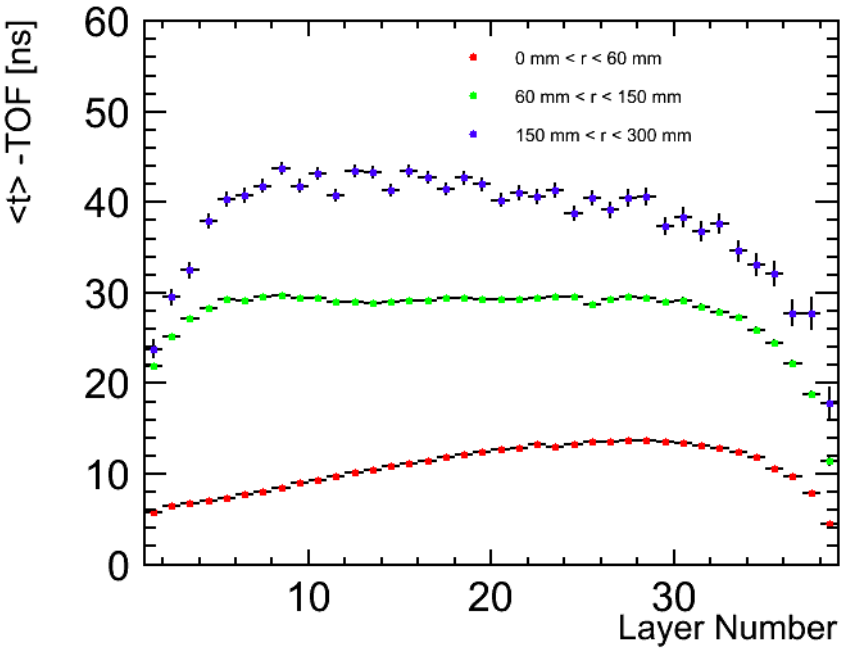
→ Realistic analyses of simulation data with timing information started

→ Prepare for future 4D testbeam measurements

10 GeV pions QGSP_BERT_HP

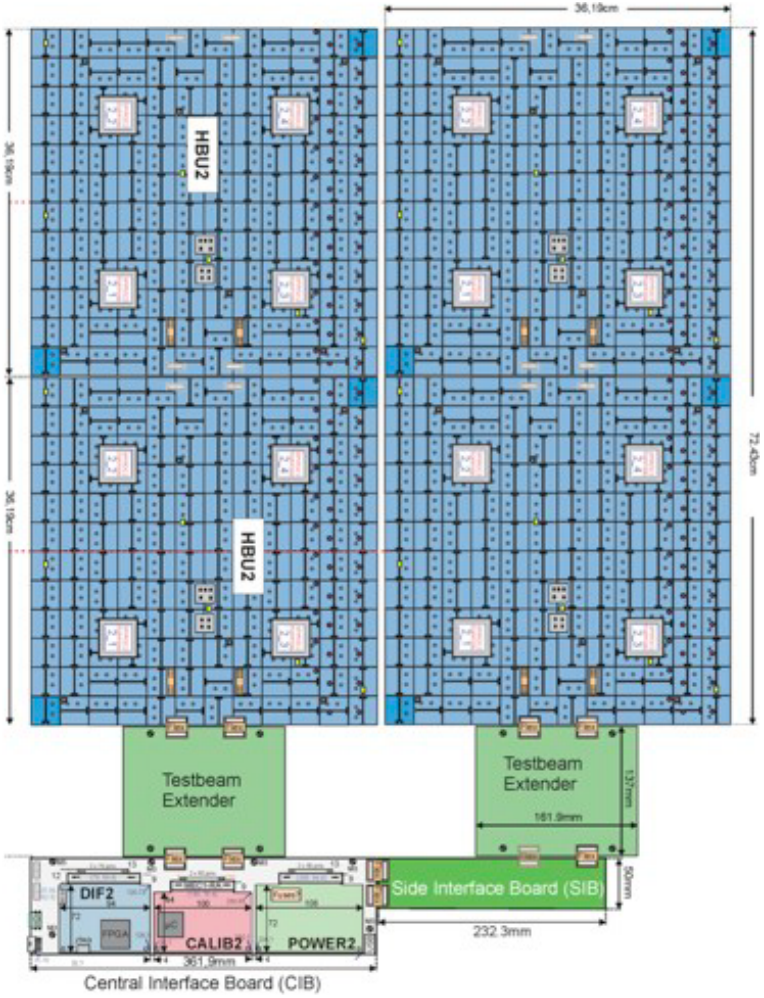


10 GeV pions QGSP_BERT



- difference between models > 1 ns (ASIC resolution) in every layer
- smaller difference in last layers

Preparing for test beam (SPS)



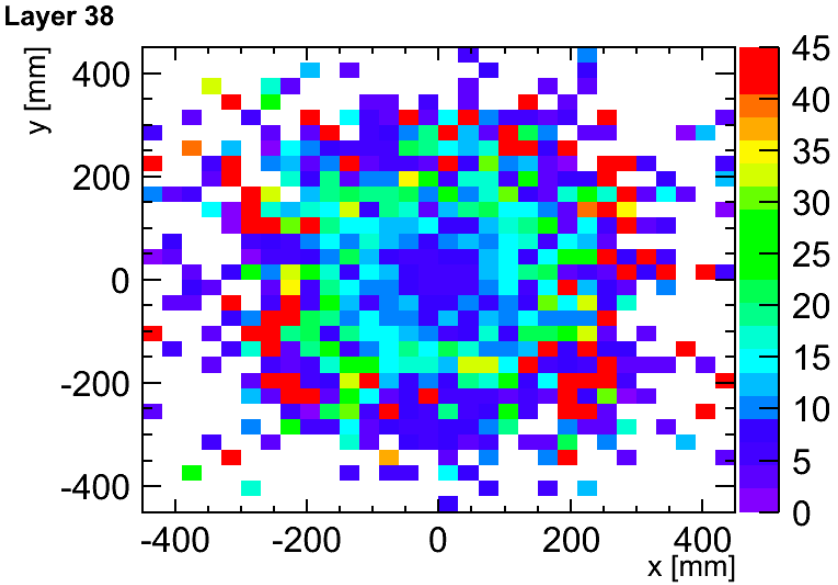
Planned test beam time at SPS in Nov. ’12

→ 4-HBU-Cassette in production

→ Side-Interface-Board in development

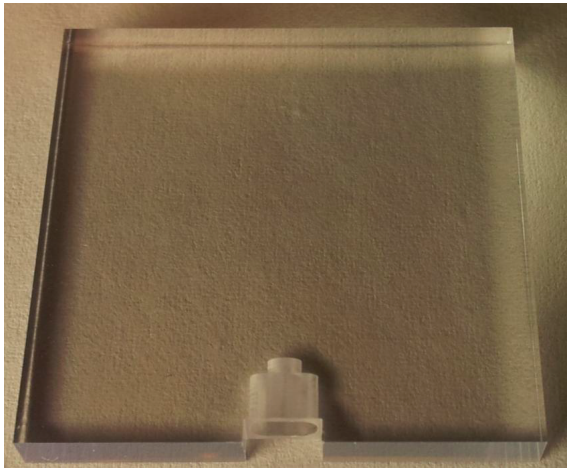
→ Extender board in development

→ DIF redesign ongoing

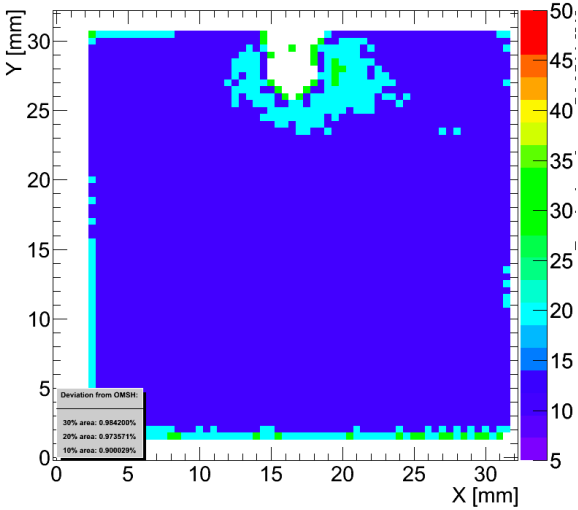


→ simulation studies ongoing

Towards direct coupling



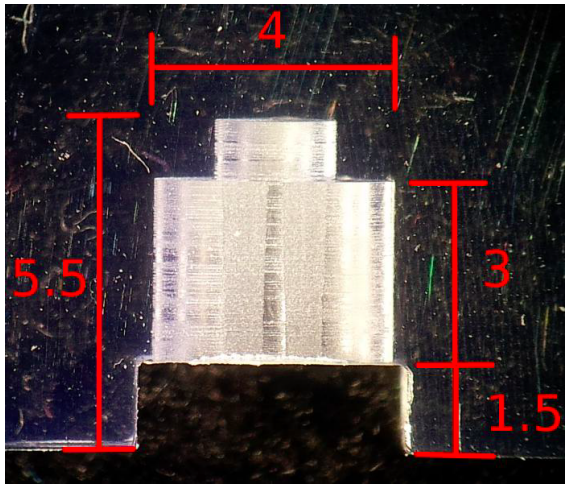
Tiles produced at UniHH using Munich direct coupling design
High uniformity
Simplified assembly procedure
sufficient LY with paper wrap



Reference:

SiPM	tile	borders	surface	LY (Pixel)
MPPC	BC-400	air	3M	10,4±0,4
MPPC	BC-400	3M	3M	28,8±0,4
MPPC	BC-400	paper	paper	19,7±0,4

SiPM	tile	borders	surface	LY (Pixel)
Ketek II	BC-400	3M	3M	33,7±0,4

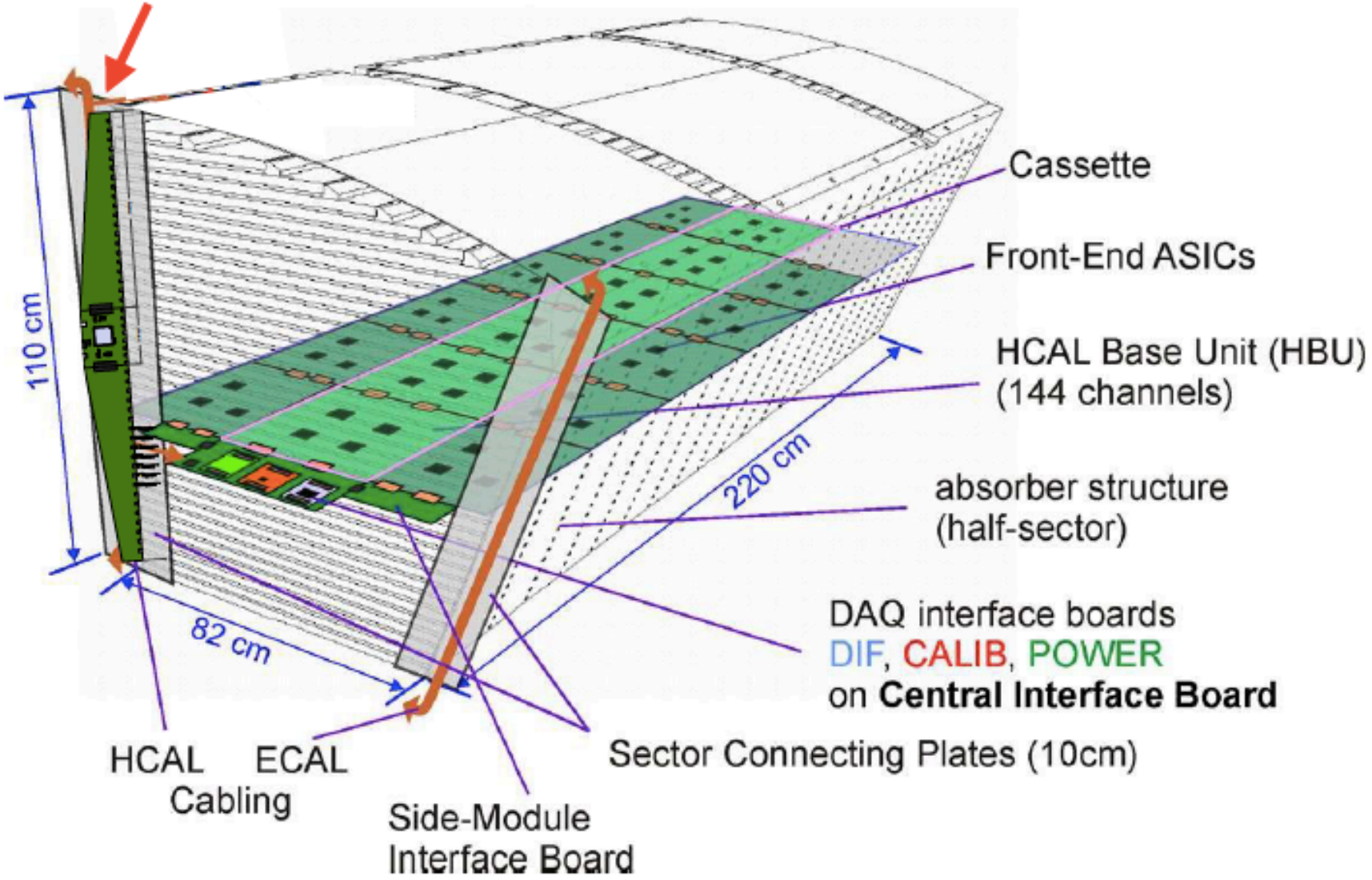


Ketek (Type II)
2.25 mm x 2.25 mm area (12000 cells, pitch 20 µm)

Towards a complete system

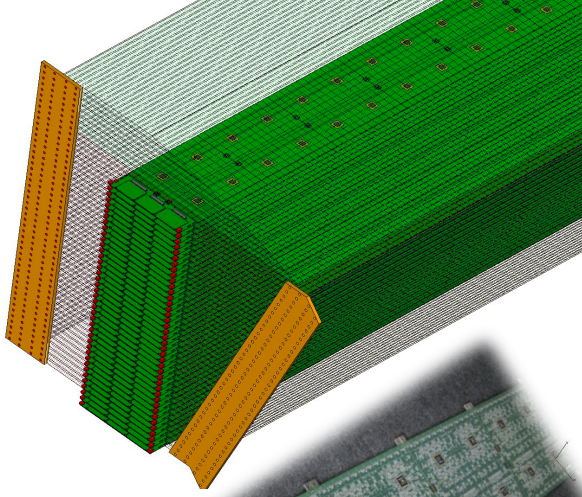
Put LDA board inside cable shaft!

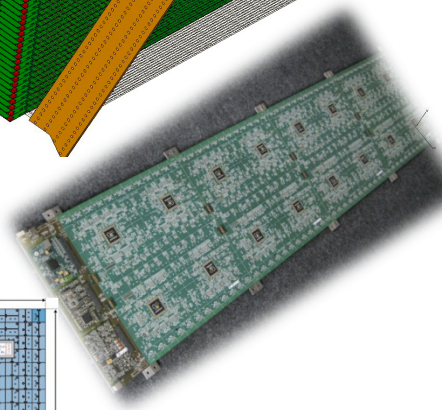
Uni Mainz

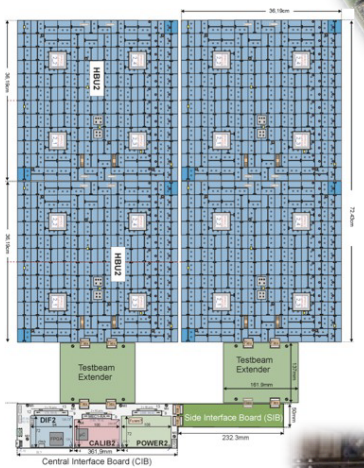


Conclusions / outlook

- AIDA work package 9.5 AHCAL is progressing according to schedule
- Test of power pulsing and electronics in a 2m long calorimeter layer in preparation at DESY
- Getting ready for first 4D hadronic shower measurements at SPS in fall this year
  - All critical components under development or test
  - Need to intensify activity on DAQ development/adaptation
- Progress towards a calorimeter stack







EUDET vertical test structure

Deviation from OMSH	Desy Tile	Itep Tile (fully 3M)	Itep Tile (matted sides)
30 %	98.4 %	99.3 %	98.5 %
20 %	97.4 %	96.0 %	94.4 %
10 %	90 %	82.8 %	75.9 %
OMSH	28.4 p.e.	14.2 p.e.	14.1 p.e.