Timepix1 readout

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Introduction

Subtask 9.2.3 (CEA, DESY, Bonn, NIKHEF): Common **readout systems** for gaseous detectors. Auxiliary electronics for the read-out of **pixellated front-end chips**, aimed at highly granular pixel read-out of **gas detectors**, are to be developed.

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Timepix 1 chip

Introduction

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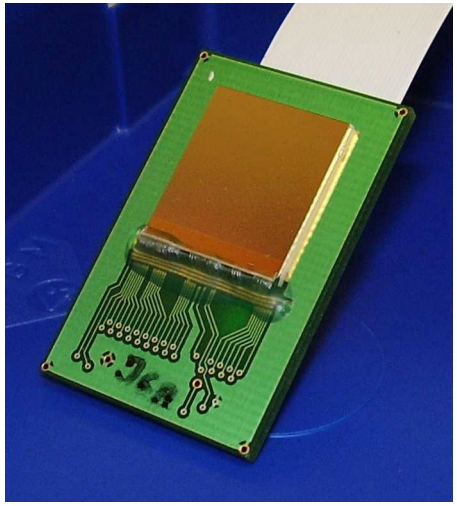
Scalable Readout System (SRS)

Outline

- Introduction
- Timepix 1
- Readout system
  - current system
  - new system
- Status one year ago
- Efforts of last year
- Outlook

Timepix 1

- Universal readout chip
- Properties:
  - active surface: 1.4 x 1.4 cm²
  - pixel size 55 x 55 µm²
  - 256 x 256 pixel array
  - 14 bit counter in each pixel (ToA or ToT)
  - Noise threshold ~500e^- (ENC ≈ 90e^-)



Timepix 1

Important for readout:

- 256 x 256 x 14 ≈ 1 Mbit of data
- Takes 9,2 ms @ 100 MHz to read out
- → theoretical limit of readout speed: 108 Hz

Requirements for new readout

- Reach the limit of readout speed
- Transmit data in efficient way to PC and control several chips

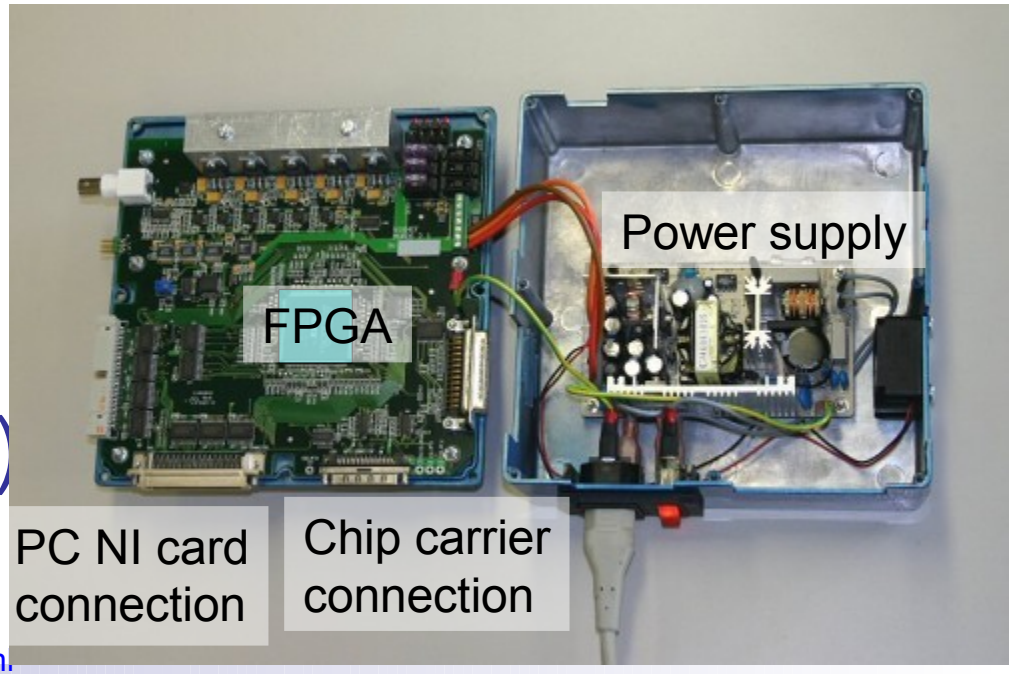
Readout system

Current system: MUROS 2.1

- Developed at NIKHEF orig. for Medipix2
- Readout speed in practice ≈ 3 Hz
- DAQsoft: Pixelman

Problems:

- Not available
- Old drivers(NI card)
- Only up to 8 chips



http://www.nikhef.nl/pub/experiments/medipix/muros.htm

Readout System

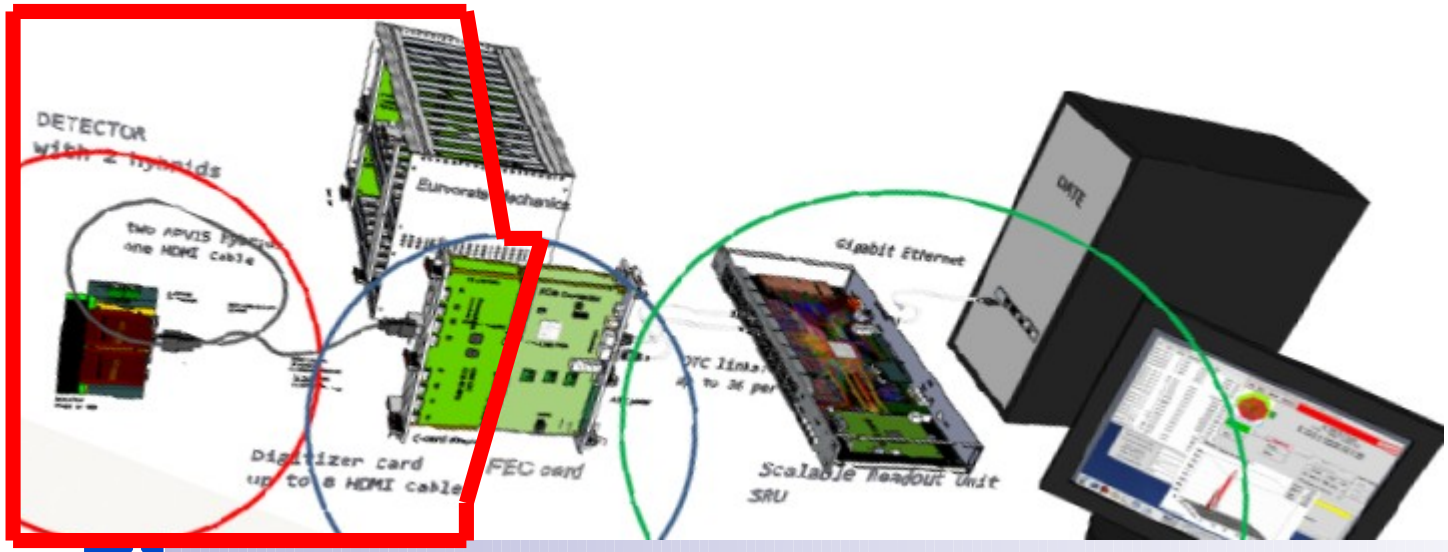
Aims for the new system:

- Read out ~100 chips → large area detector
- Modular system → use SRS
- Develop firmware for Virtex6 FPGA
- Use Gbit ethernet
- On FPGA zero suppression
- Triggerable
- Integrated control and calibration

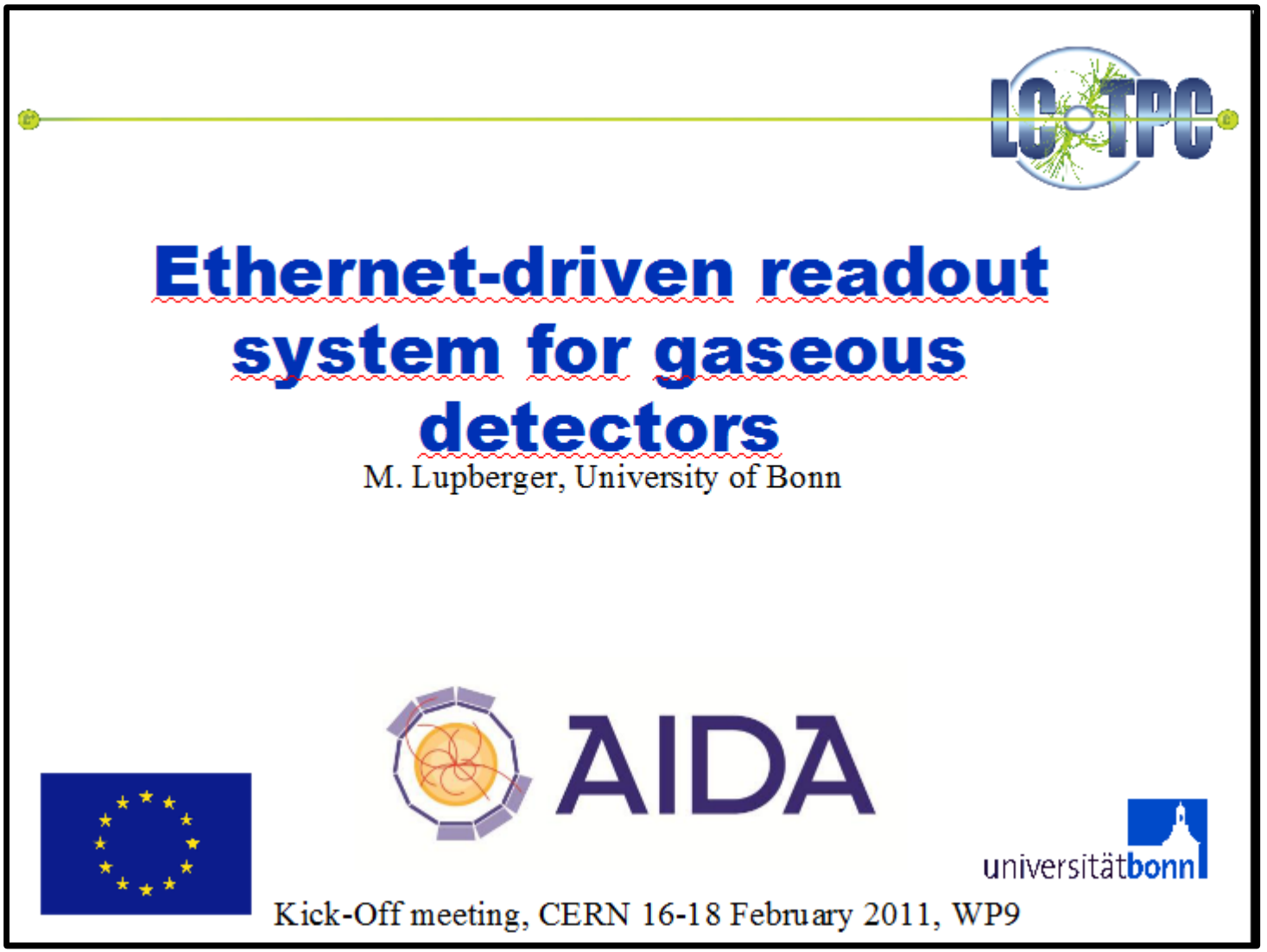
Readout system

The Scalable Readout System (SRS)

- Developed within RD51 (OpenSource)
- Provides common hard- and firmware
- User part: chip carrier & adapter card

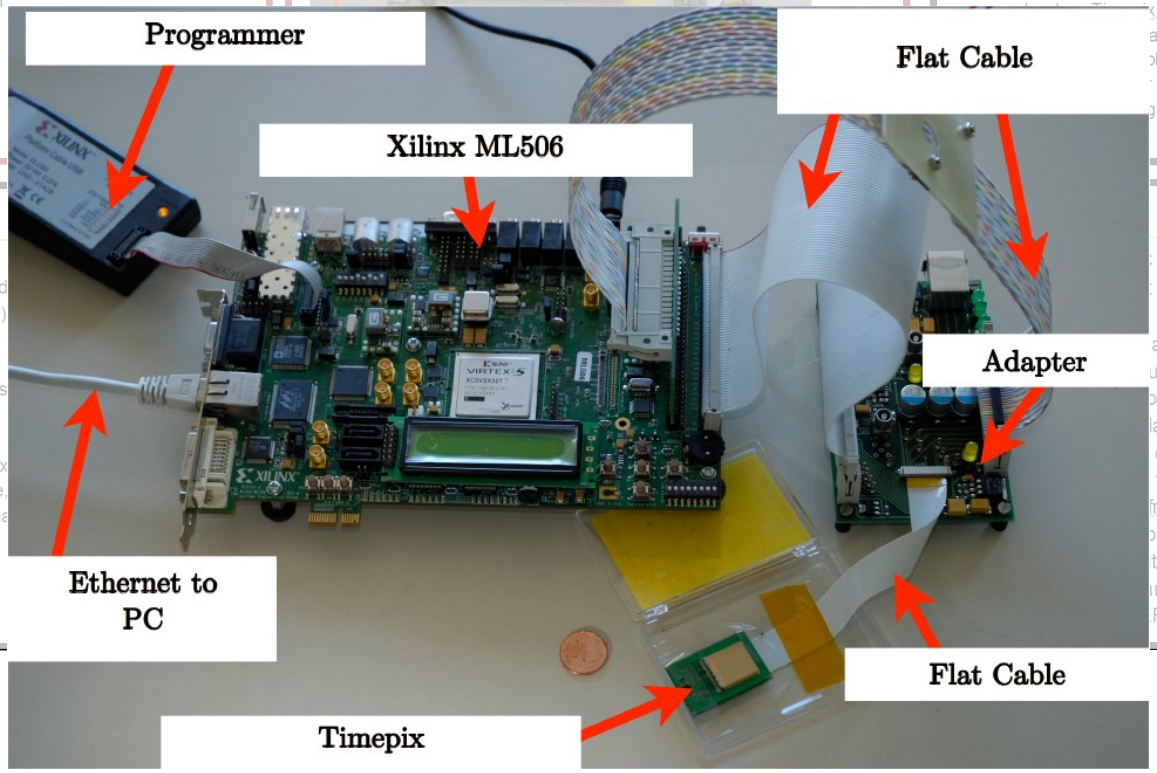


Status one year ago



Status one year ago

- First step: copy of Mainz prototype system
- Xilinx Virtex5 evaluation board

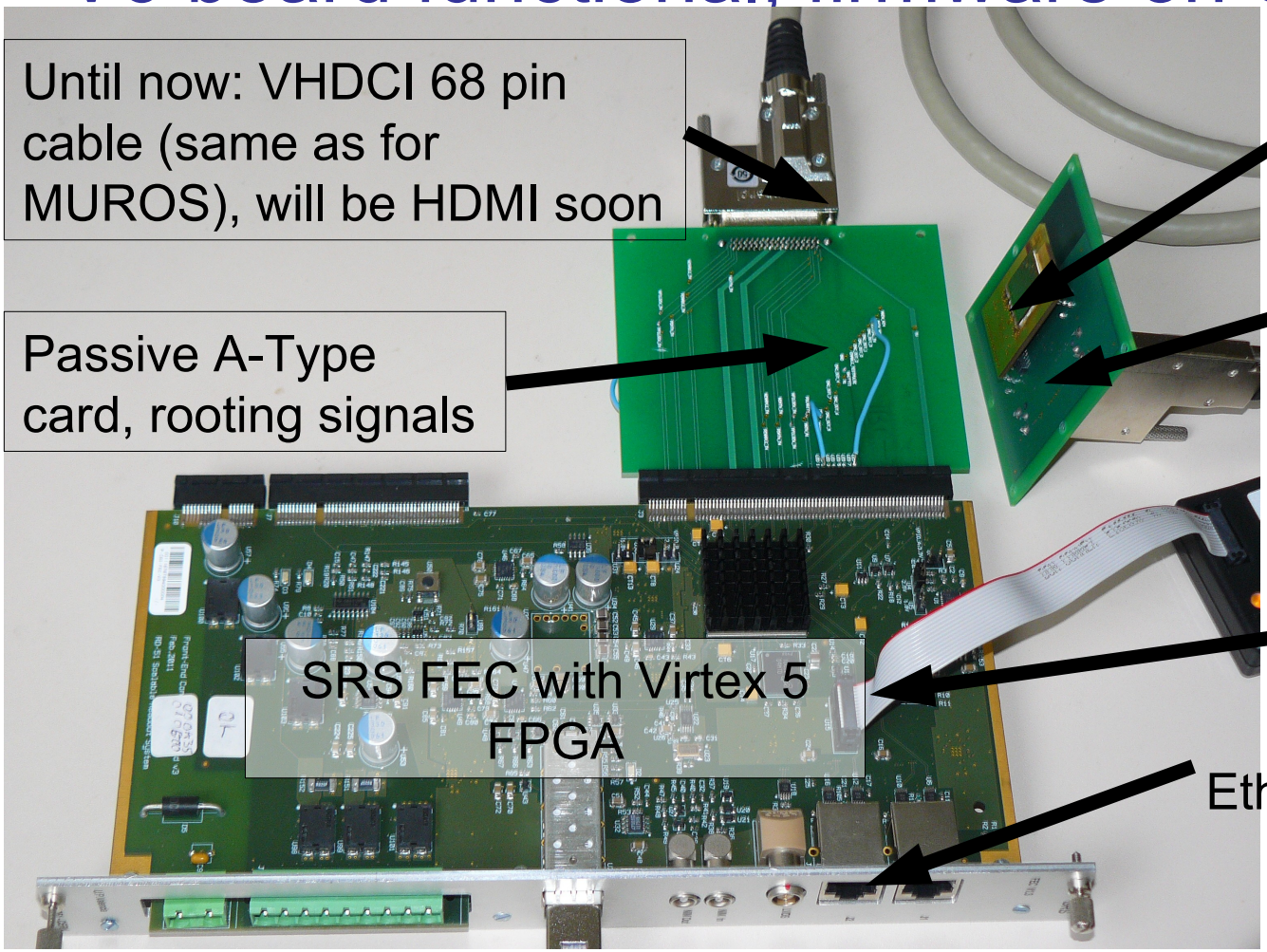


Status one year ago

- Data piped through FPGA
- Readout speed up to 27 Hz
- Firmware modifications for Virtex6 FPGA
  → timing problems
  → adapter card for V6 board to be designed

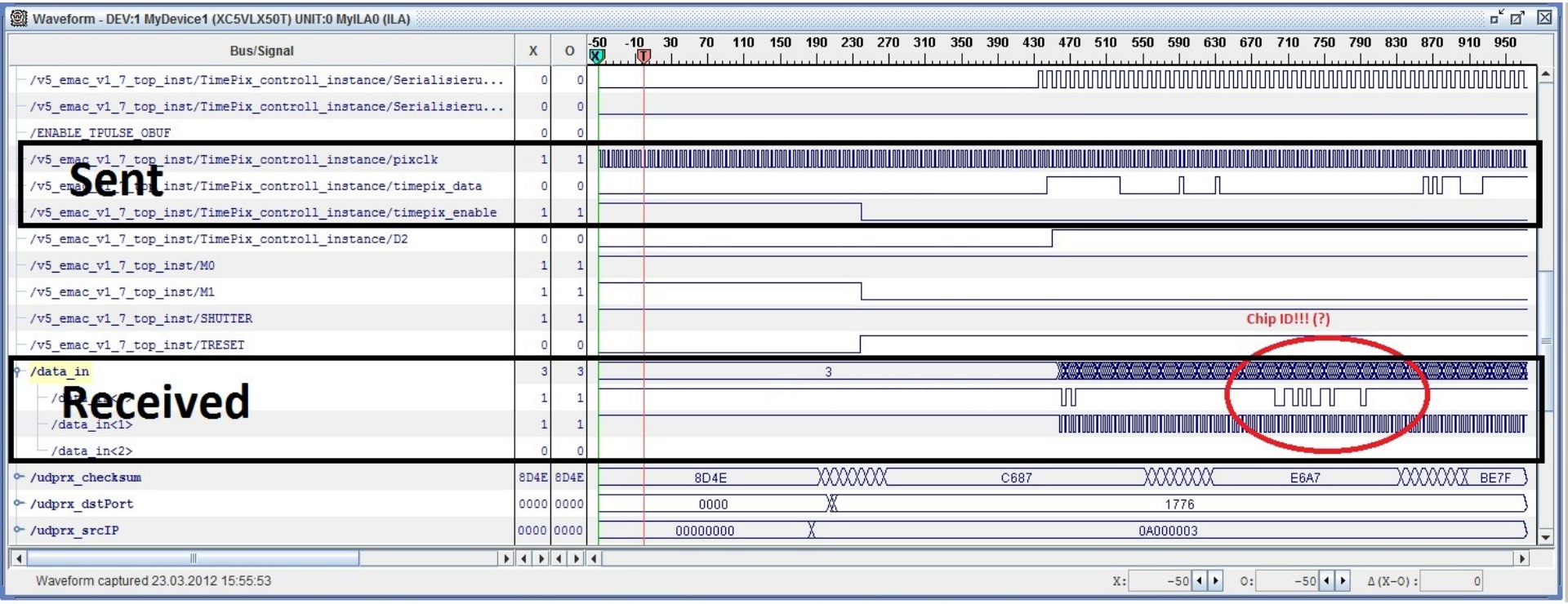
Efforts last year

- V6 board functional, firmware on SRS



Efforts last year

- SRS can read chip ID



Communication with SRS (no simulation)

Efforts last year

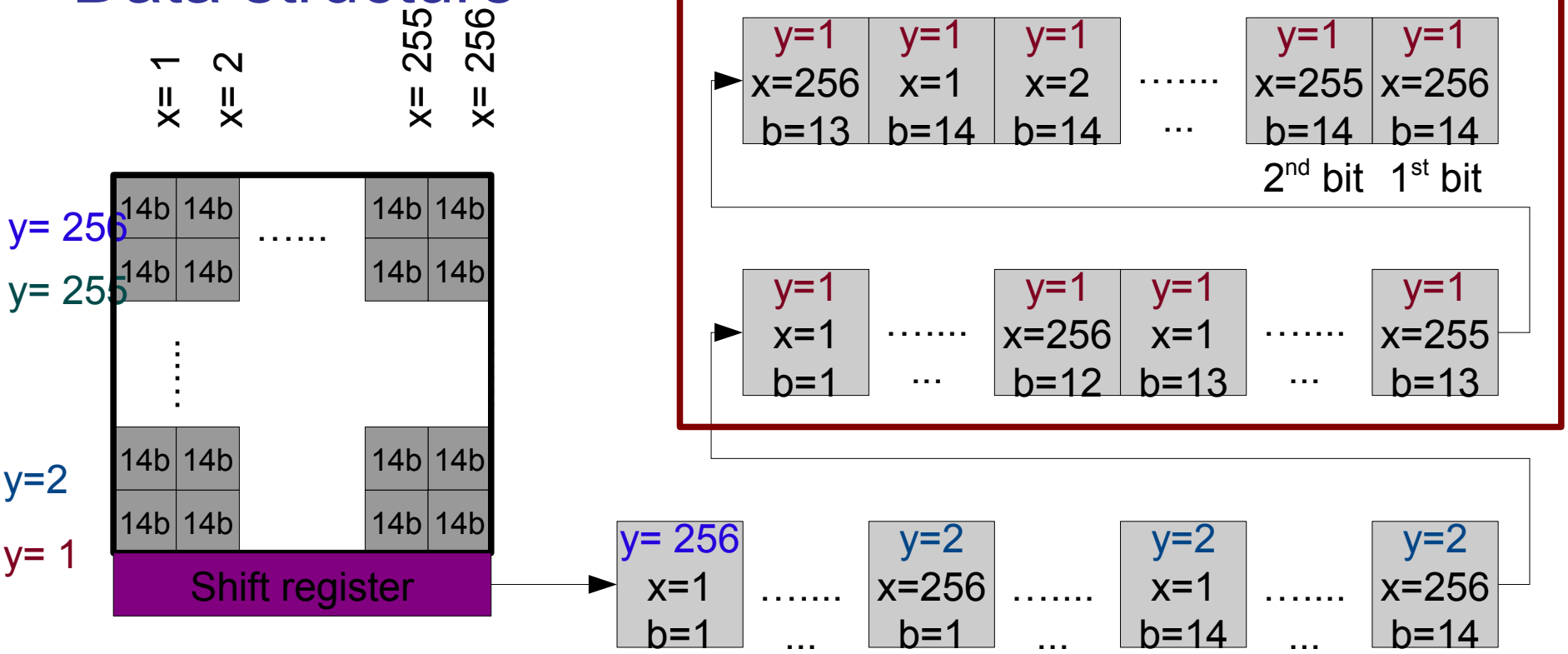
Firmware modifications:

Smarter readout / more effective

- Zero suppression in FPGA
- Multi threading in FPGA
- Clock domain crossing for better sampling

Efforts last year

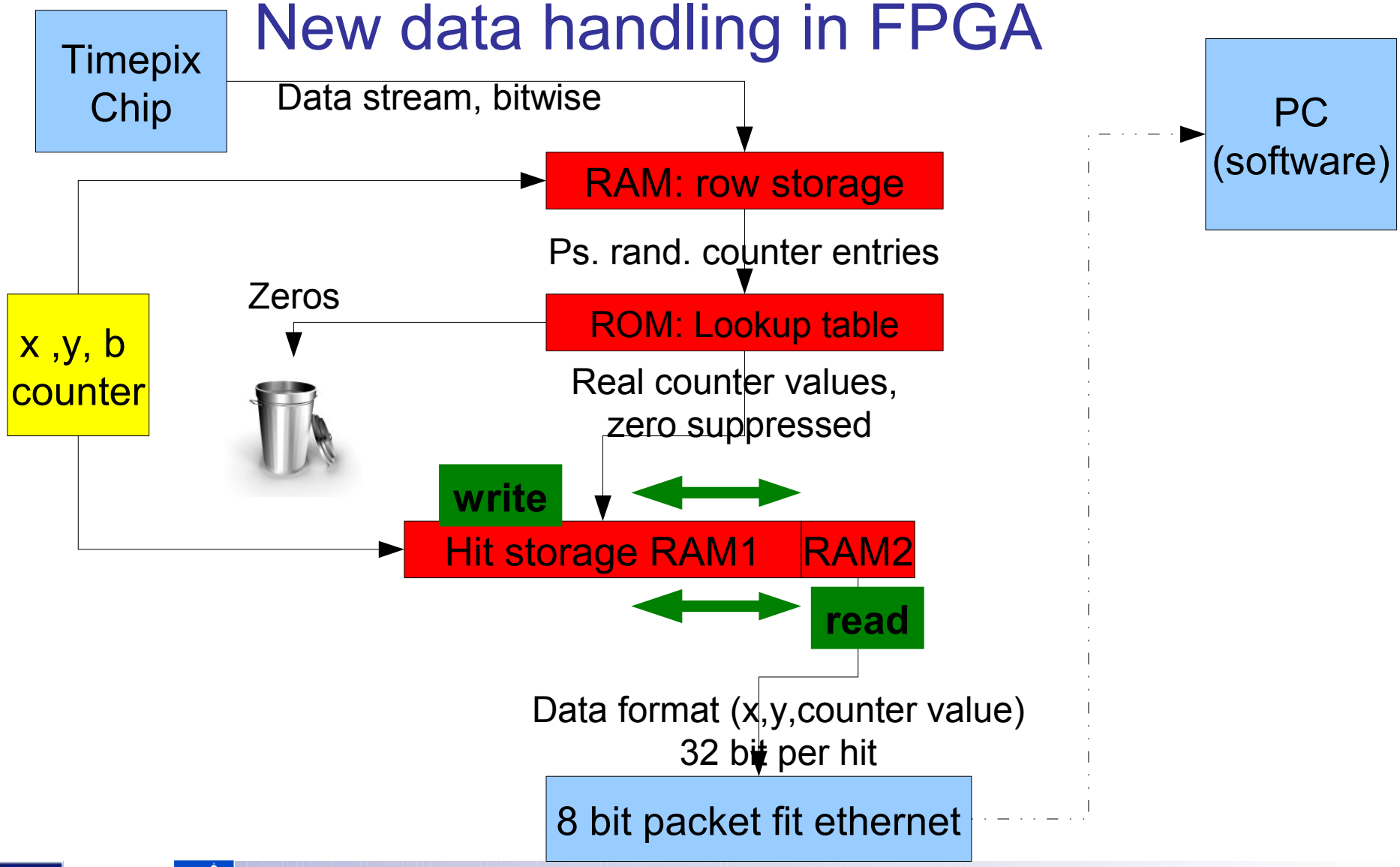
- Data structure



- Data in each pixel: not real number but pseudo random counter

Efforts last year

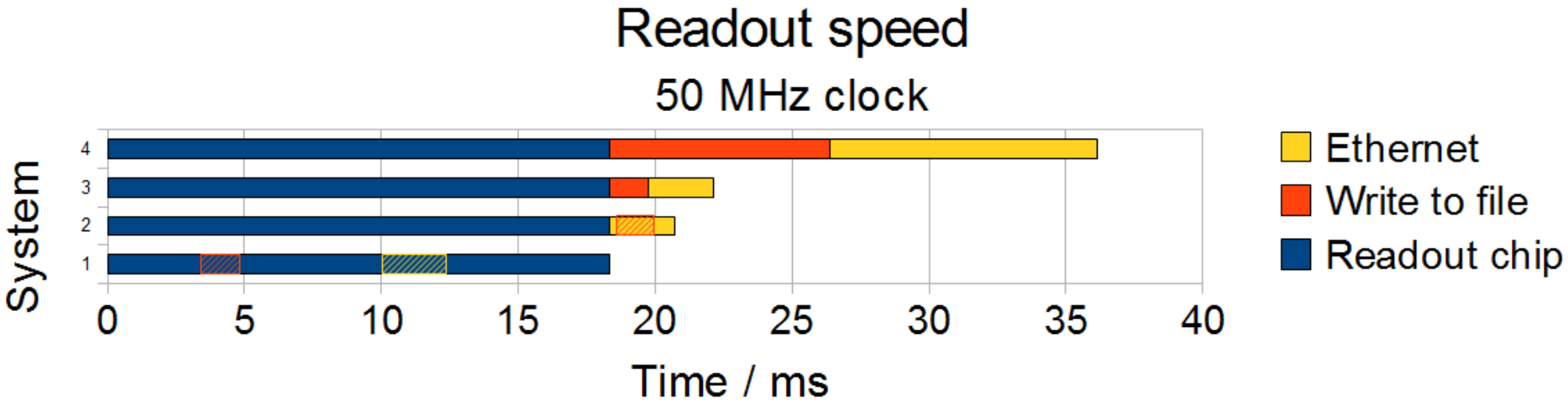
New data handling in FPGA



Efforts last year

Software modifications:

- Write zero suppressed files
- Multi threading in PC

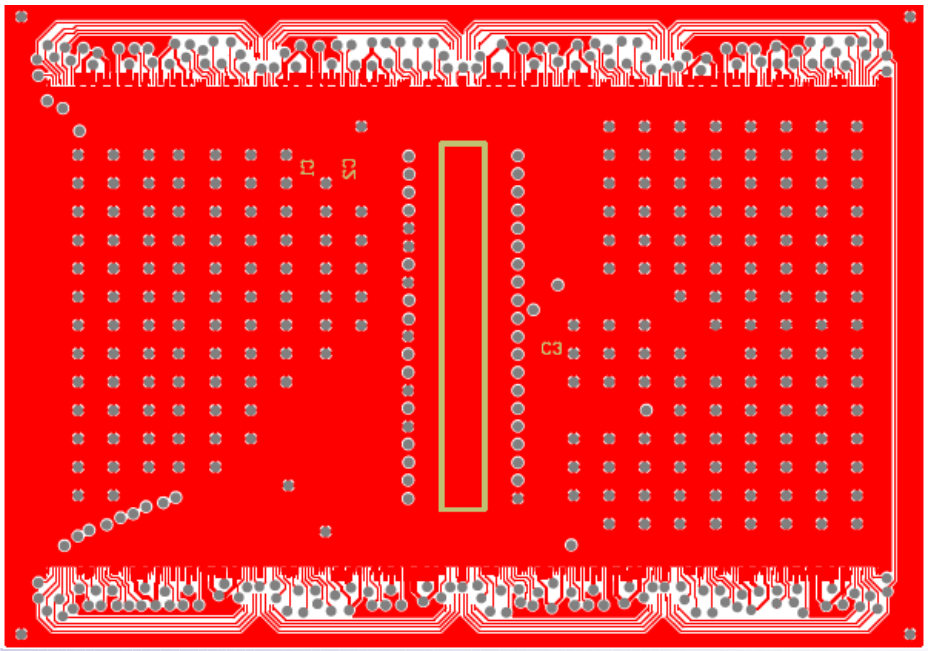


- Speed after all improvements @ 50 MHz:

  27 Hz → 53 Hz (53,7 Hz theoretical limit)

Outlook

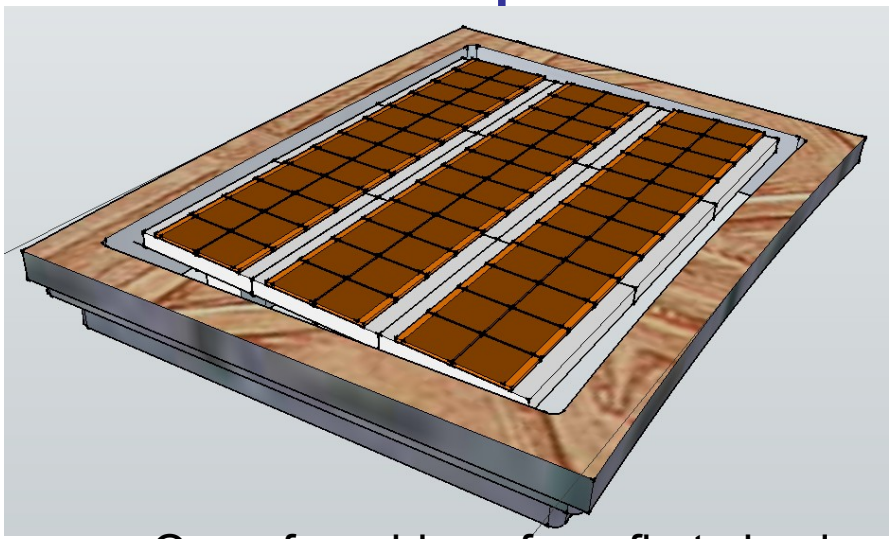
- Software improvements (calibation, threshold equalisation, …)
- Data taking with SRS + single Timepix
- SRS + 8 chips

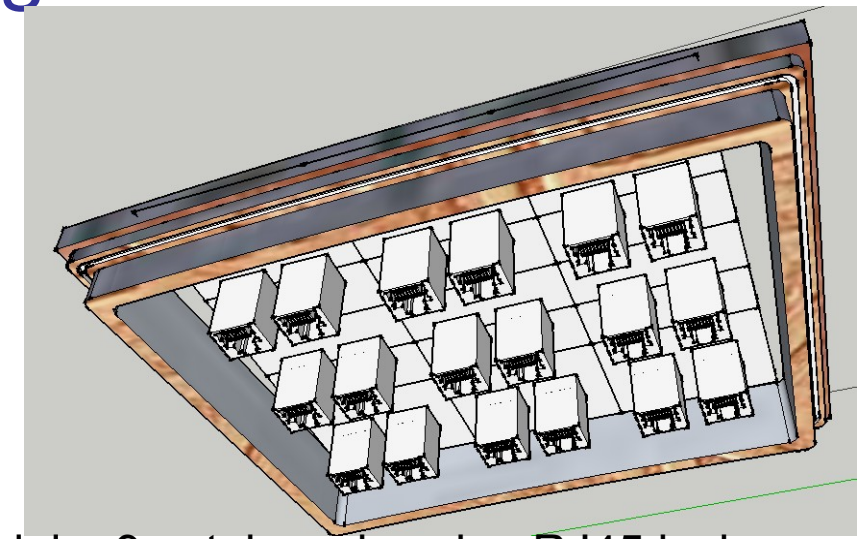


Outlook

- New type of cables between chip carrier and SRS (serialise slow control signals)
- Large (LCTPC endplate) module

  ~100 chips → cooling? Power distribution?





One of our ideas for a first simple module: 9 octoboards using RJ45 jacks

Summary

- Development of new readout for Timepix1
- Prototypes on V5 and V6 boards
- SRS single chip readout almost there
- Data taking after software improvements

- 8 chip module to come
- Go towards full module by using modularity
- Still a lot of work to do :)