Pixelated readout at Nikhef

1st AIDA Annual Meeting

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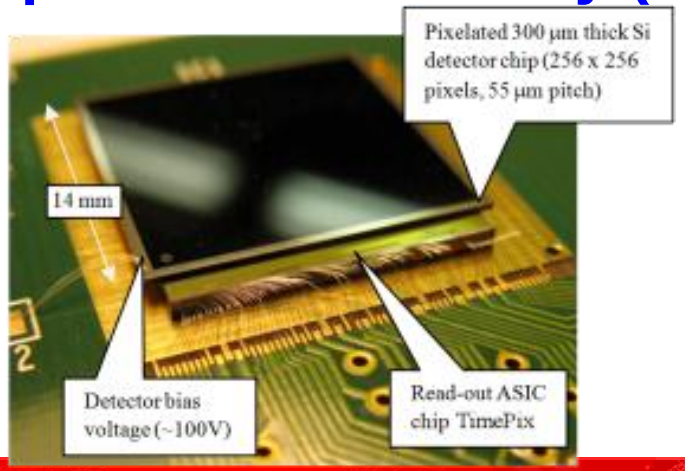
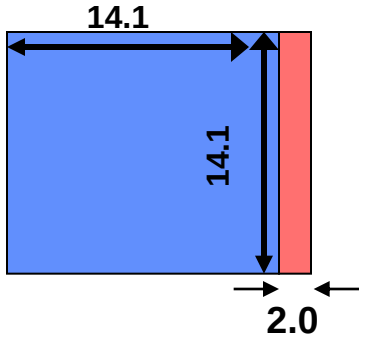
- Timepix chip
- Relaxd for Timepix
- Timepix3 chip
- Timepix3 readout with SPIDR
- Few words on CO_2 cooling

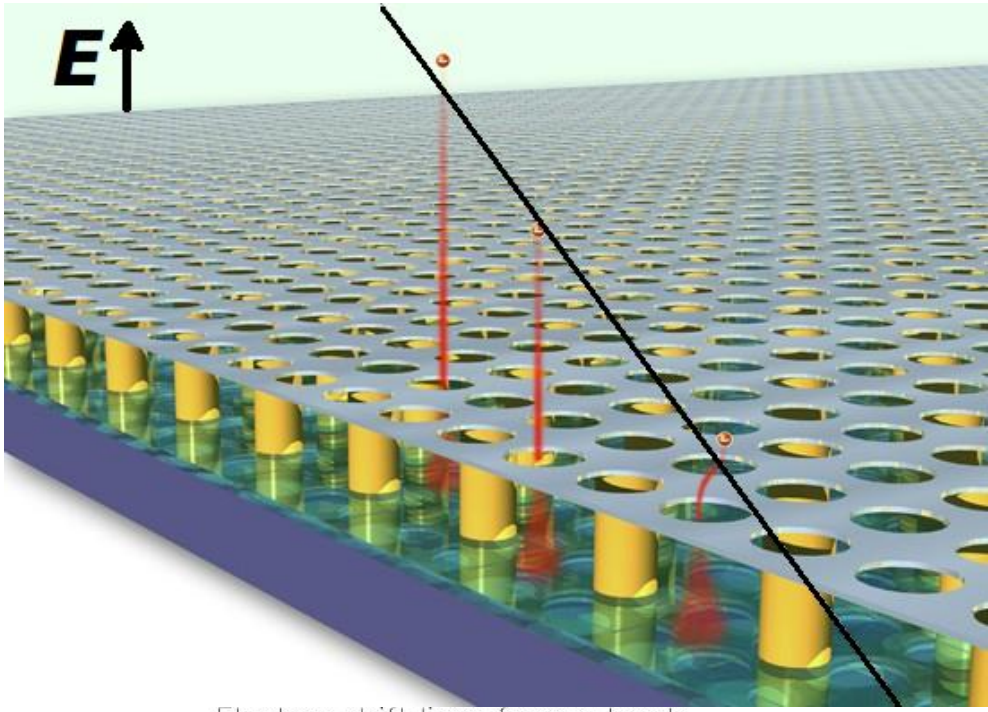
Timepix

- **Timepix existing chip in 0.25 μm technology**
  - General purpose chip developed by Medipix collaboration in 2006
  - Matrix of 256x256 pixels of 55x55 um^2
  - Either Time-of-Arrival or Time-Over-Threshold (charge) measurement
    - Or 'counting' for imaging
  - Frame based readout: readout the whole matrix, no zero suppression
    - Simple readout, but slow (~120 Hz using 1 serial link)
    - Higher speeds possible with parallel readout
  - Chip size 14x14 mm, 3 side buttable
  - Moderate radiation hardness
- **Timepix is used in many (non HEP) applications**





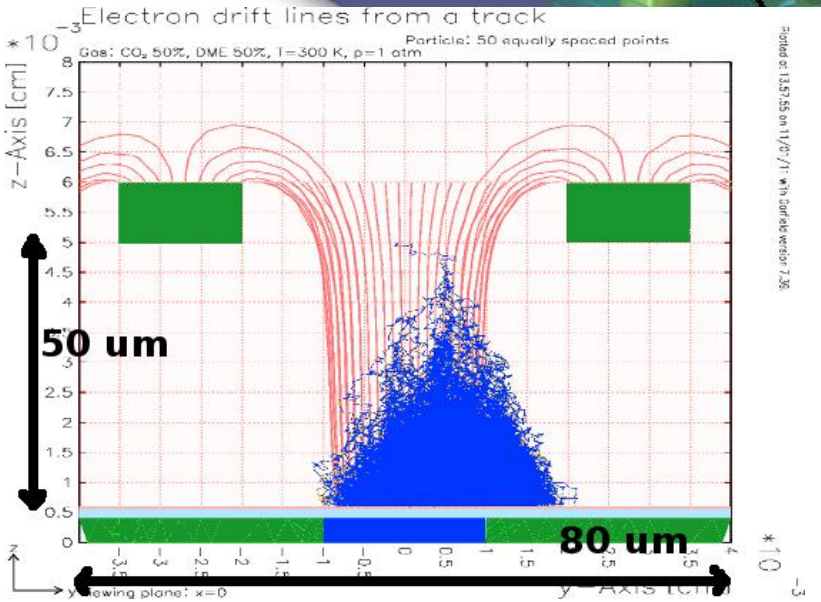
Ingrid / Gridpix



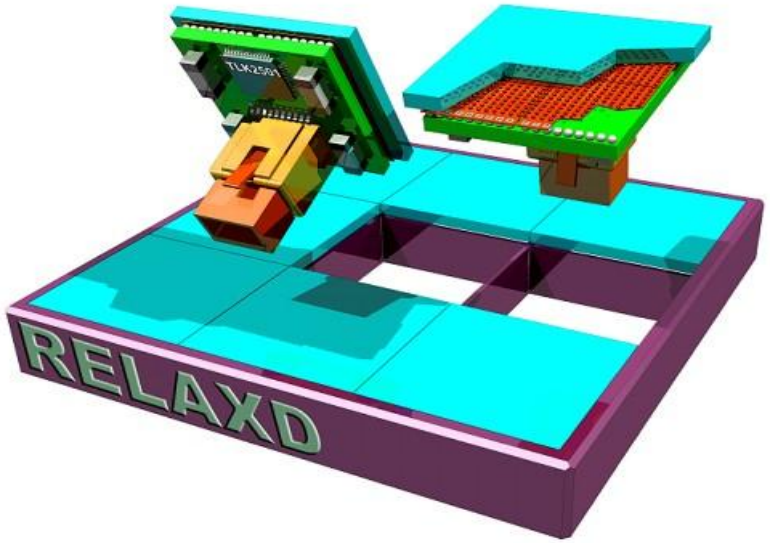
- Integrated grid on top of Timepix
- Grid provides gas gain
- Thanks to Bonn University for their efforts to produce high quality devices

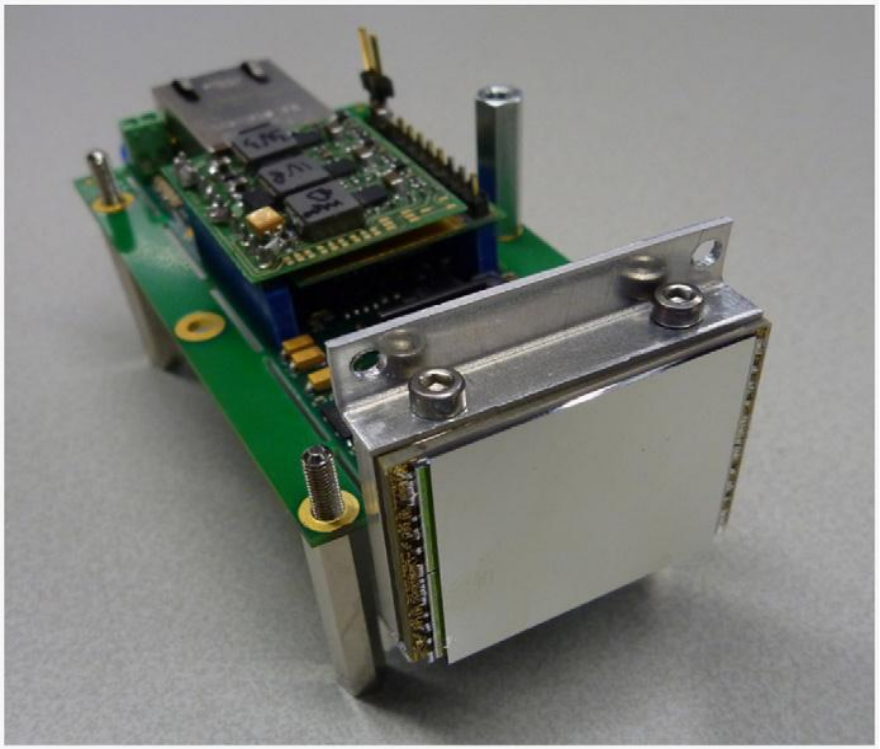
- Z-coordinate from drift time measurement
- Timepix: 10 ns time resolution

- Drift length depends on application
- from mm to meter



Readout with Relaxd

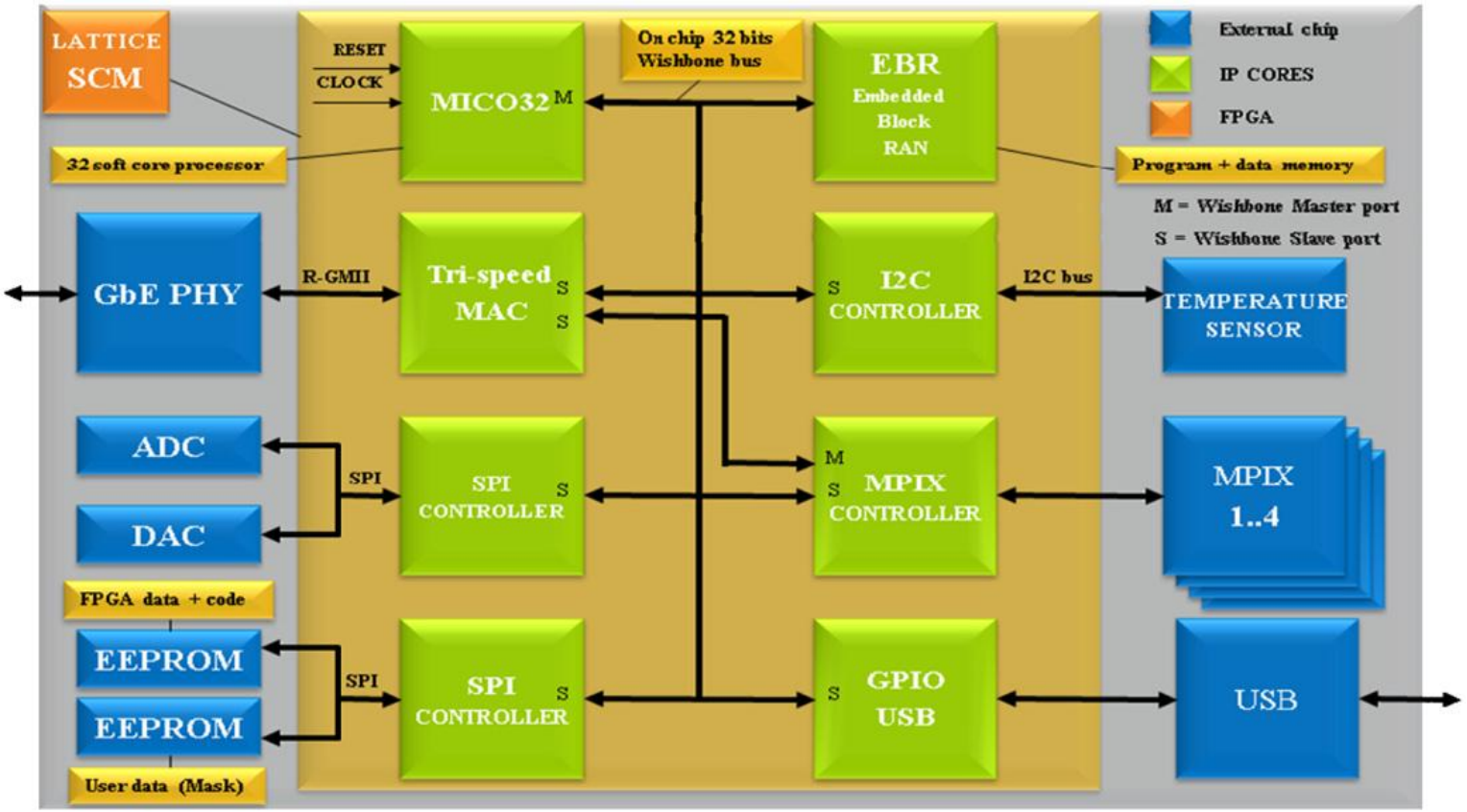




- Readout of large area Xray Detectors
- Originally designed for imaging (MPX2)
- T-shaped module
- Fits behind quad chip module
- Small board with FPGA and gigabit Ethernet interface
- Firmware adapted to readout Timepix chips
- Matching DAQ software: RelaxDAQ
  - Windows & Linux
- Works also with Pixelman SW

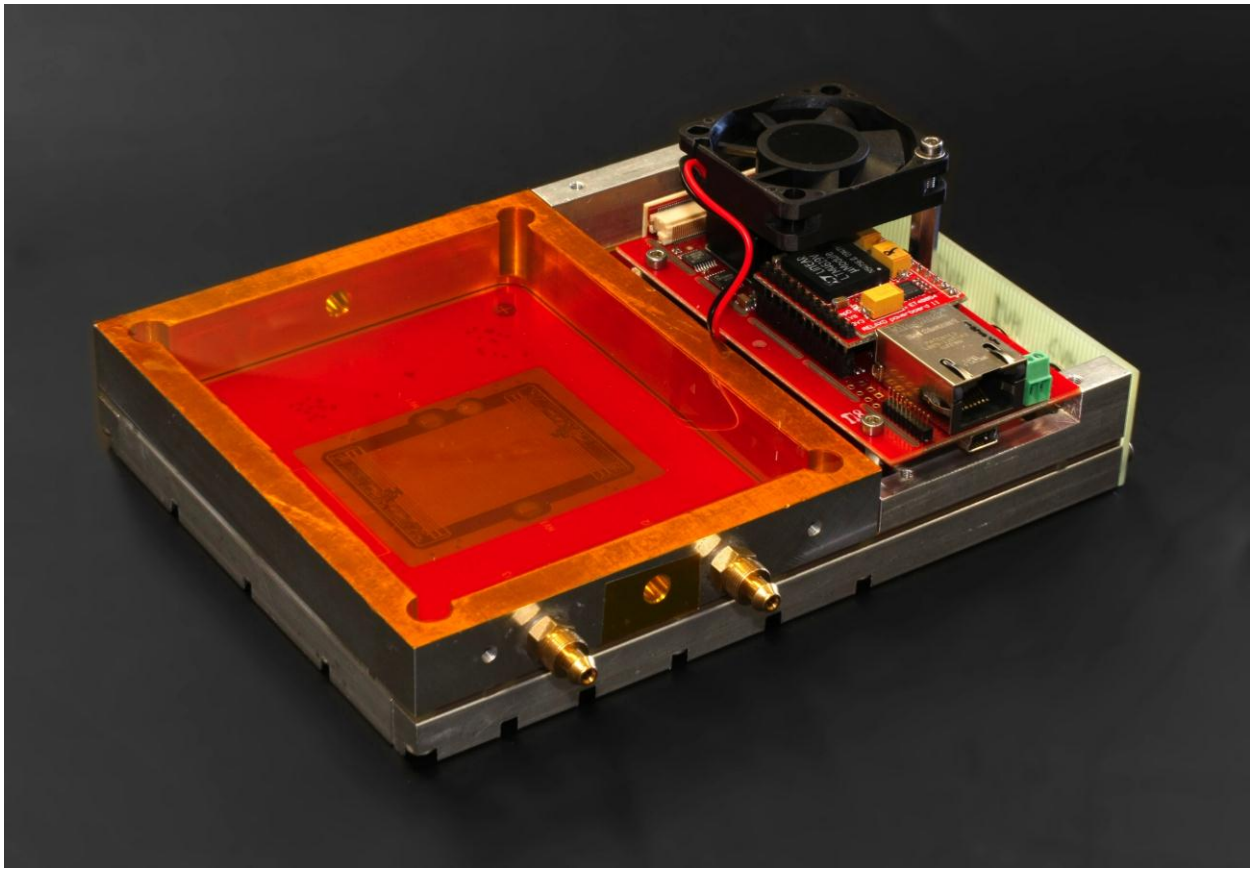
Relaxd

- Readout of 4 Timepix (or medipix2) chips via Gigabit Ethernet
- Up to 120 frames/ second (Timepix limit)
- No zero-suppression -> 50% occupancy of 1 Gbit/s Ethernet
- Our work horse for Timepix readout



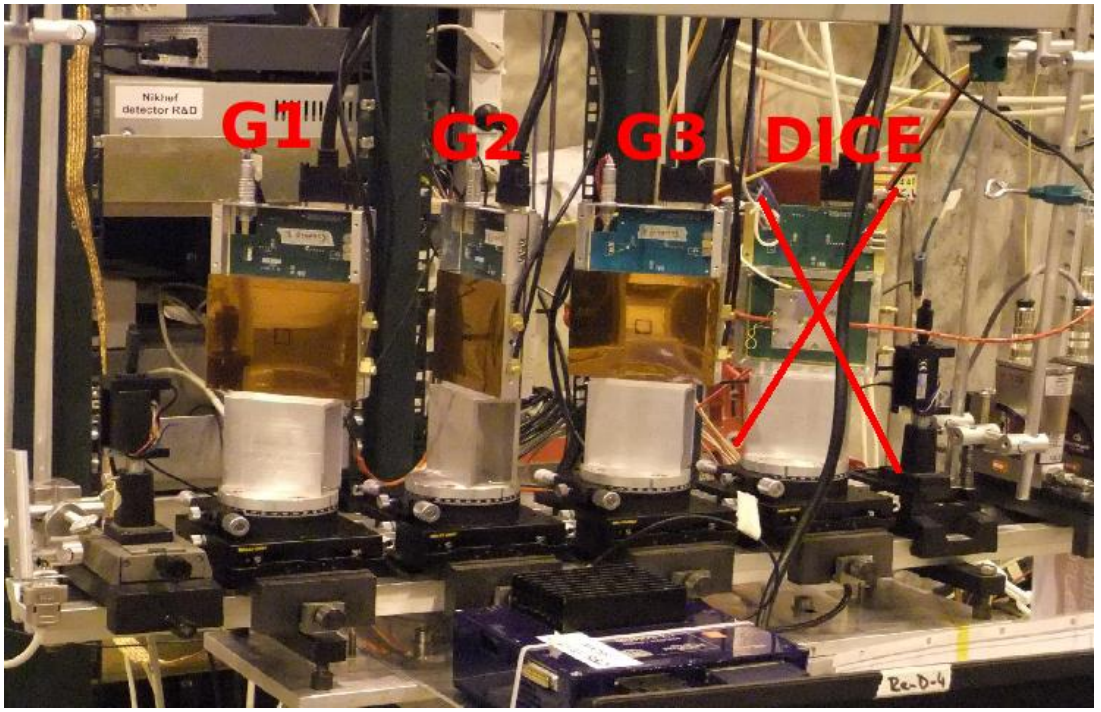
Renext: relaxd for gaseous detectors

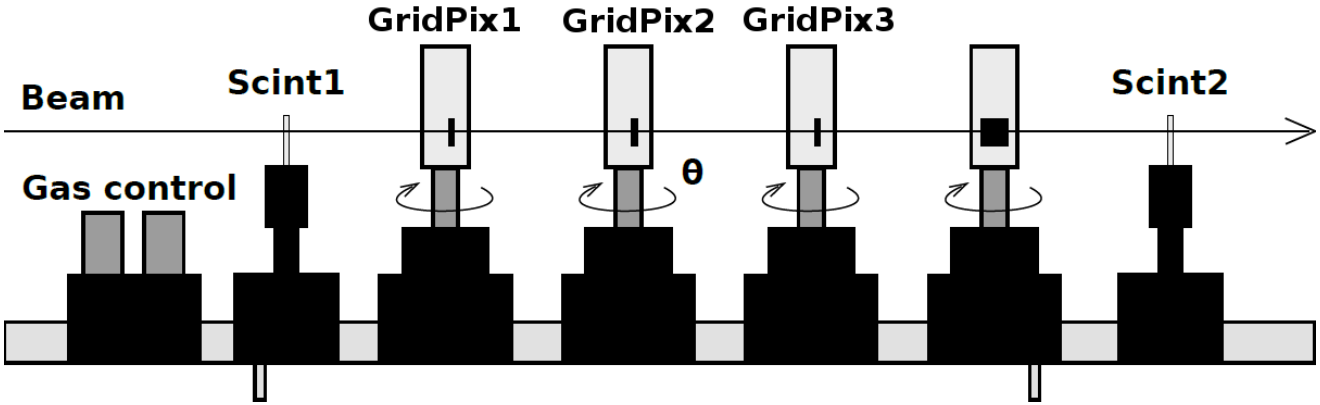
- Quad timepix carrier board for gaseous detectors
- Provides gas enclosure
- Relaxd readout board as mezzanine



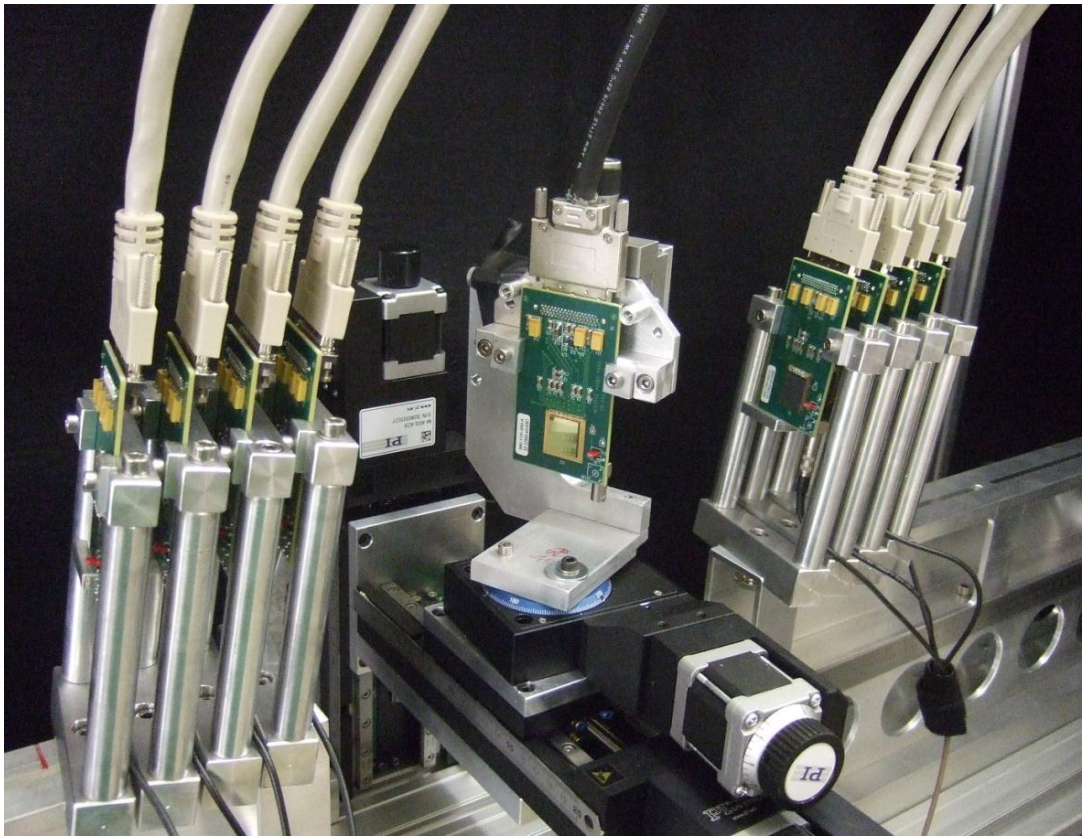
GridPix beamtests

- GridPix as tracking detector
- Used for telescope planes
- And as Device Under Test
- Relaxd readout





But not only used for Gaseous detectors …

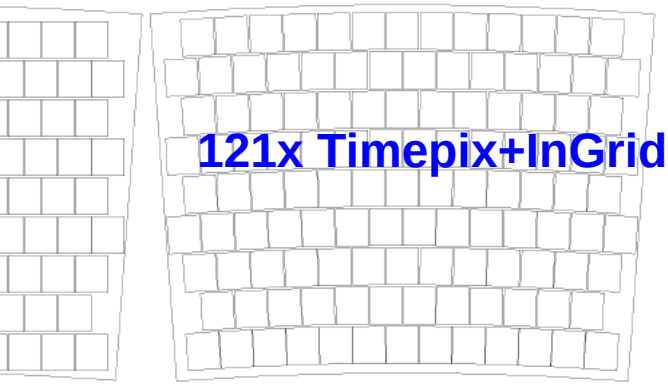


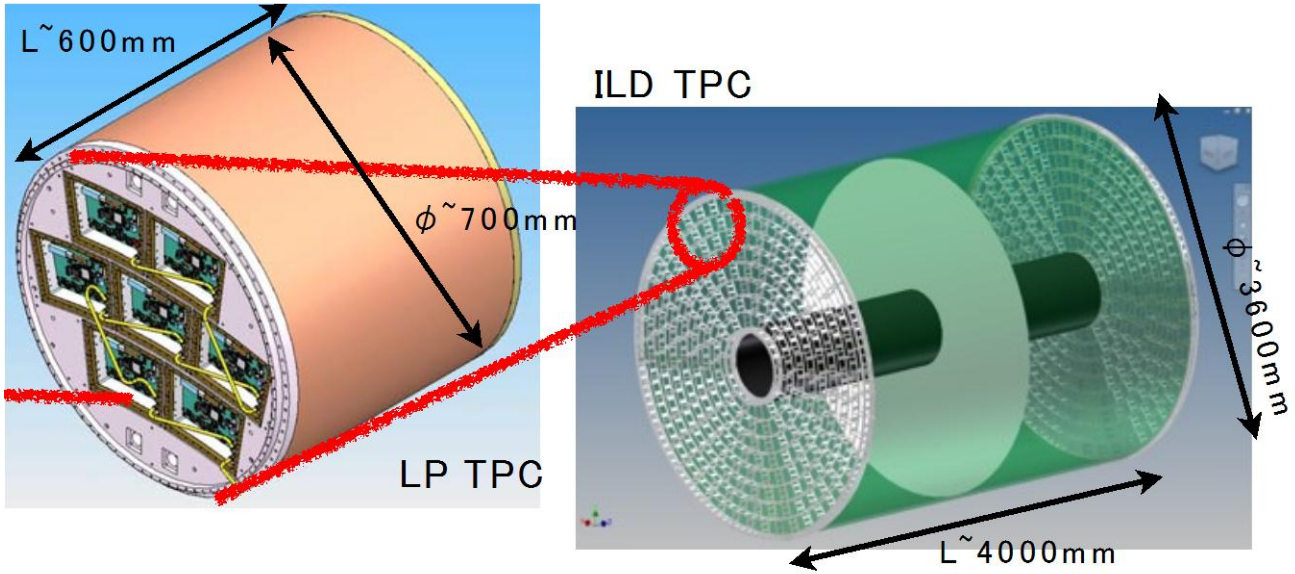
- “LHCb” Timepix telescope
- CERN chip carriers, 4 single chips into 1 Relaxd readout via breakout cable
- One of the AIDA telescope arms

Large Prototype TPC

- **Building a LPTPC tile with Timepix is under consideration**

- **Scope of project to be defined**
  - One big module or multiple smaller ones?
  - Relaxd readout on backside?
  - Dedicated PCB for 8? / 16? or more chips
  - Current relaxd can readout 4 chips
    - limited resources in FPGA
  - Migrate to larger FPGA?





Limitations of Timepix

- **Z-resolution limited due to 10 ns time resolution**
  - Factor 5 more required for thin tracking devices
  - Development of high resolution TDC: 1.7 ns bin width
  - Prototype chips Gossipo3 and G4 (G4 with University of Bonn)
  - Gossipo will not be developed to full scale chip: TDC integrated in timepix3
- **Maximum frame rate of ~120 Hz**
  - Full frame readout is OK for imaging, but too slow for tracking detectors
  - -> zero suppressed readout
  - new development: Timepix3

Next generation: Timepix3

- **TPX3 is a general purpose chip**
  - **Some compromises coming from the need to accommodate many different applications, the technology choice, and the schedule.**
- **Developed and paid by the Medipix3 collaboration**
- **Chip designed by CERN with contributions from Nikhef and Bonn university**
- **Main changes w.r.t. Timepix1**
  - **Fast front-end -> Timewalk < 25 ns**
  - **Simultaneous ToA and ToT measurements**
  - **TDC resolution 1.7 ns**
  - **Data driven readout: Each hit is time-stamped, labeled and sent off chip immediately**
- **Timepix3 is a precursor for VELOpix (LHCb), ClicPix, etc.**

More Timepix3 info

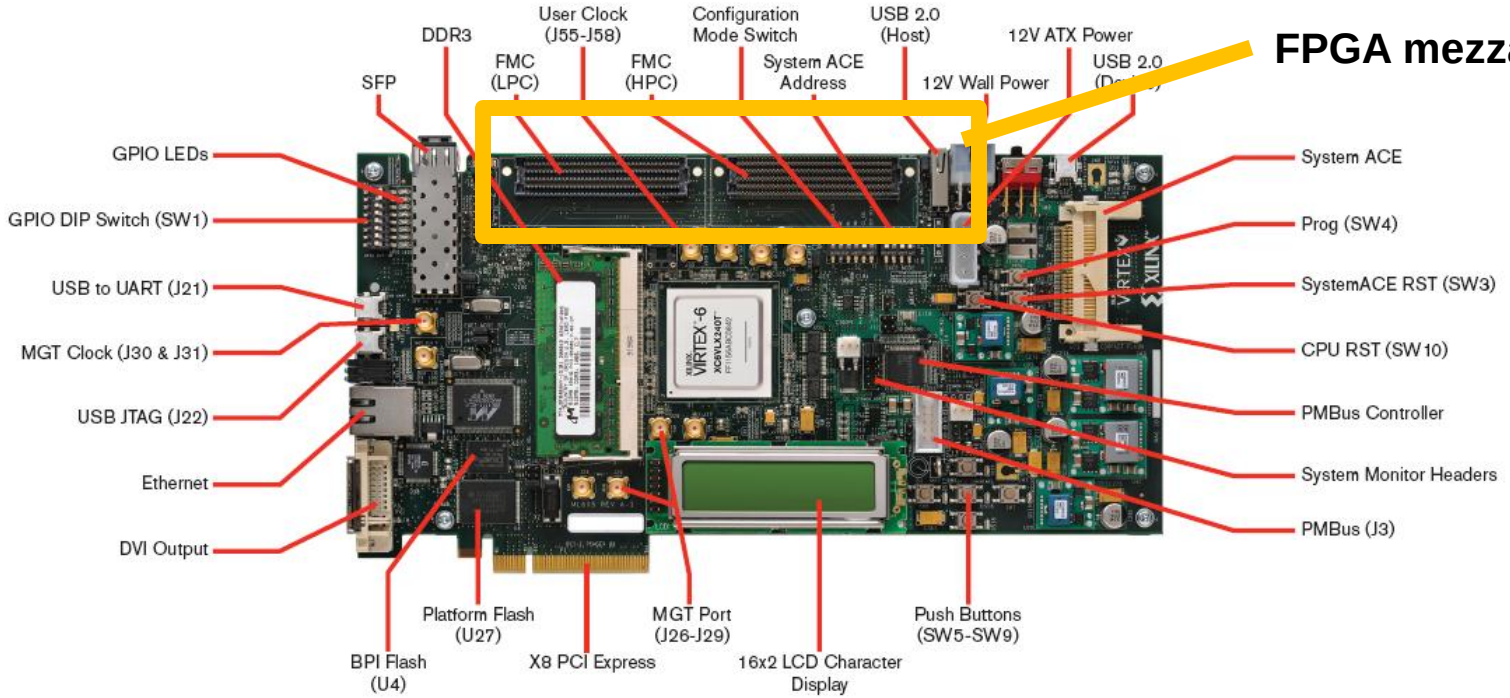
- Designed in 130 nm IBM technology
- Radiation hard, TID > 500 MRad (SiO_2)
- Hit-rate per chip, up to 40 Mhits/s
- 4 serial output links @ 640 Mbit/s
  - Clock-data encoded signals (8B/10B) -> standard in FPGAs
- Uses CERN custom designed HD digital library
  - Low power, smaller size: hence more functionality

Status:

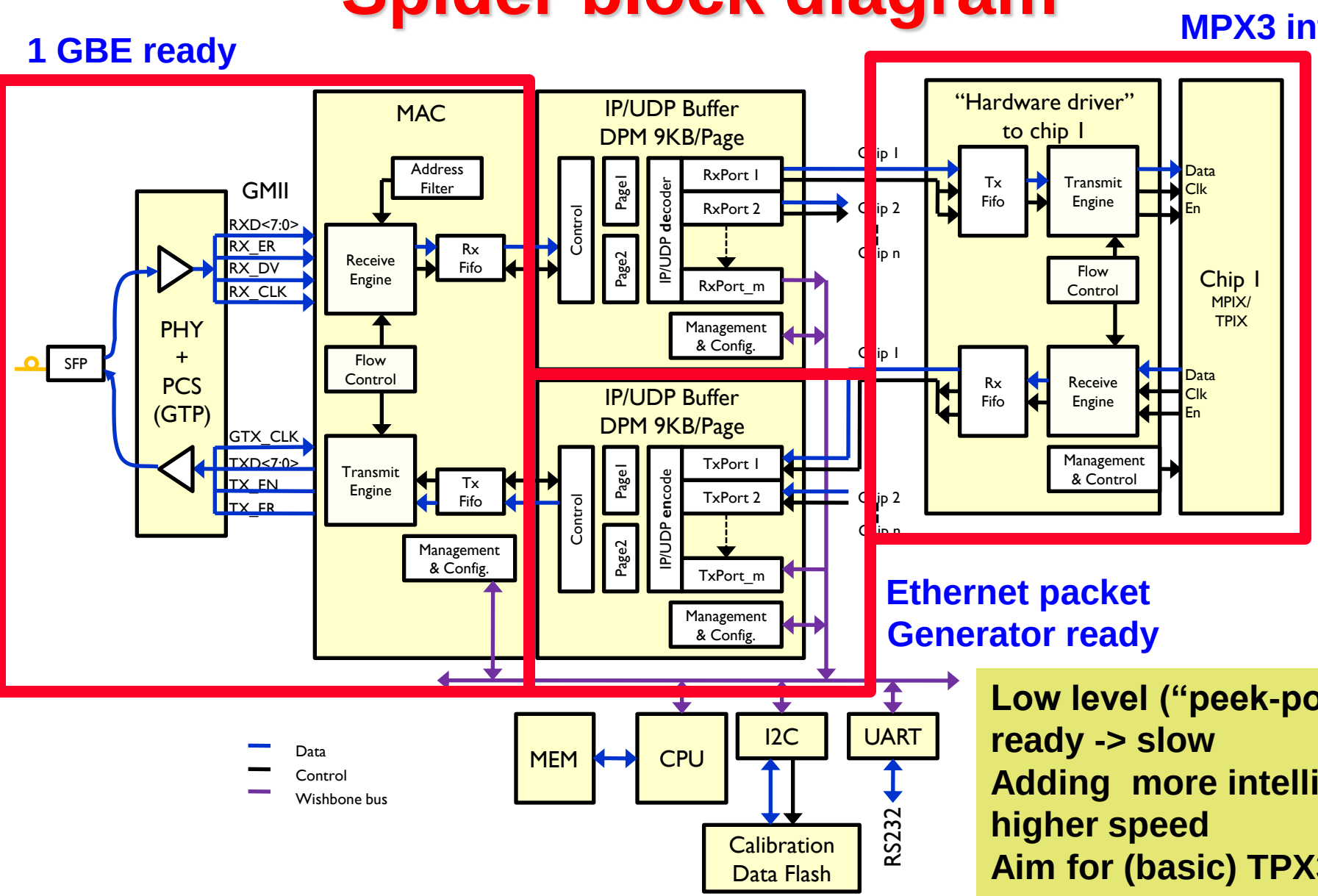
- Design is well advanced
- Chip submission expected late 2012
- A readout for TPX3 being designed by Nikhef: SPIDR

SPIDR development @ Nikhef

- Speedy PIxel Detector Readout
- Readout for Medipix3 and (later) Timepix3
- Initially 1 Gbit/s Ethernet, then migrate to 10 GBE
- Develop firmware on FPGA development boards
  - At a later stage design a compact readout module like Relaxd

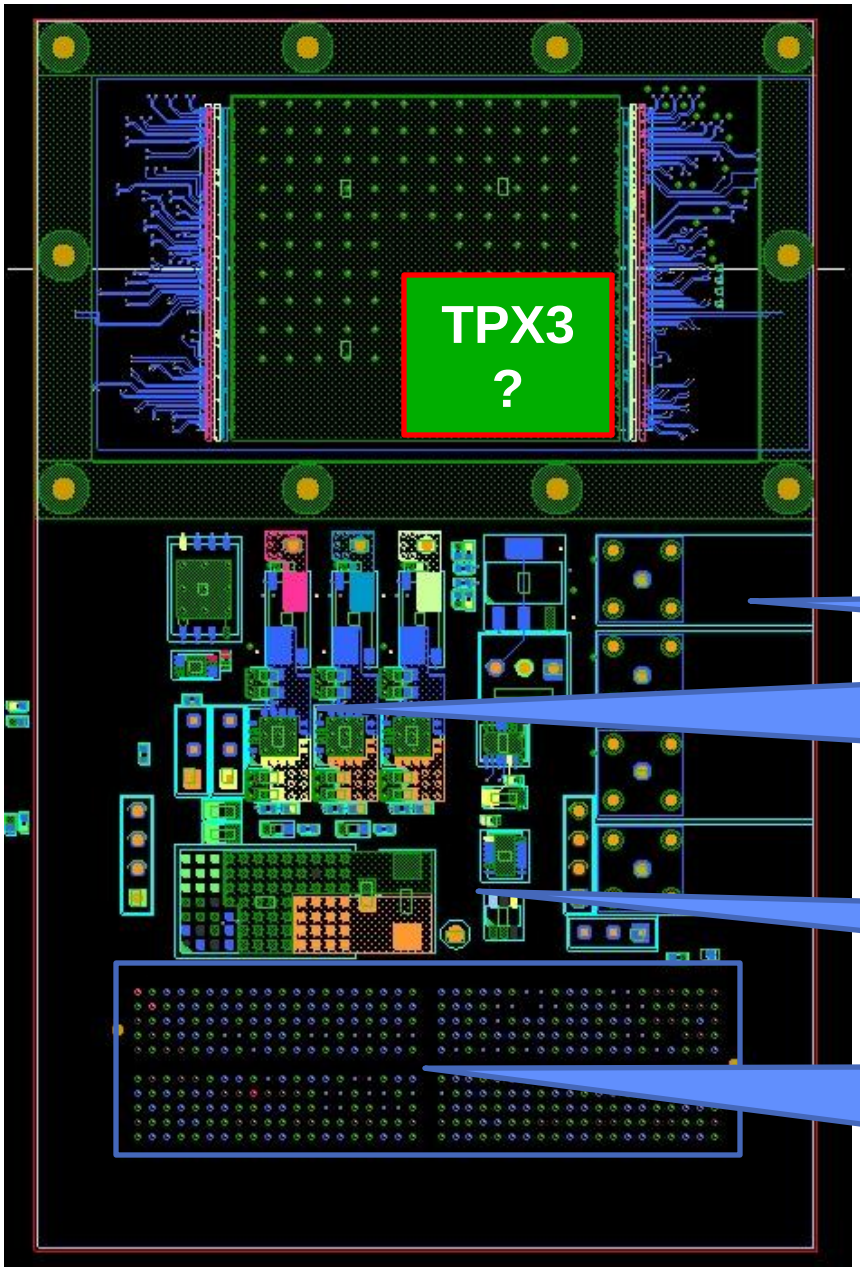


Spider block diagram



Low level ("peek-poke") system ready -> slow
Adding more intelligence for higher speed
Aim for (basic) TPX3 readout by end of 2012

FMC Mezzanine for MPX3



- Quad MPX3 chip carrier board
- Boards are in production
- In time for MPX3 V2
- Can we also use it for TPX3?
  - Depends on TPX3 bondpad layout
  - If not, redesign required

Lemo connectors to FPGA (clock, trigger, etc) + external bias

Power supply's
With I/V sense
VDD(1V5)
DVDD(2V5)
VDDA(1V5)

4 DAC channels
8 ADC channels
32Mbit flash memory
Fan controller

Vita57 FMC connector (compatible with FPGA development boards)

Readout summary

- **Nikhef uses the relaxd readout system for a Timepix based gaseous detectors**
  - non zero suppressed data to gigabit Ethernet
  - up to 120 frames / second
  - existing system, number of users growing
- **Next generation pixel chip: Timepix3**
  - Design by CERN, Bonn, Nikhef
  - 1.7 ns TDC for improved z-resolution
  - up to 40 Mhits/s, zero-suppressed readout
- **Readout/DAQ for TPX3 under development: SPIDR**
  - data to (10) Gigabit Ethernet

And something completely different

- CO_2 cooling for WP9.3
- TRACI: Transportable Refrigeration Apparatus for Co_2 Investigation
- Several system are being built (CERN/Nikhef)
- Tests / characterization ongoing

Traci-2 expectations
Chiller=1.5x capacity, Insulation 40% better