GEMs for CMS : Electronics System

Basic System

VFAT3 / GdSP

On Detector to Off Detector Electronics

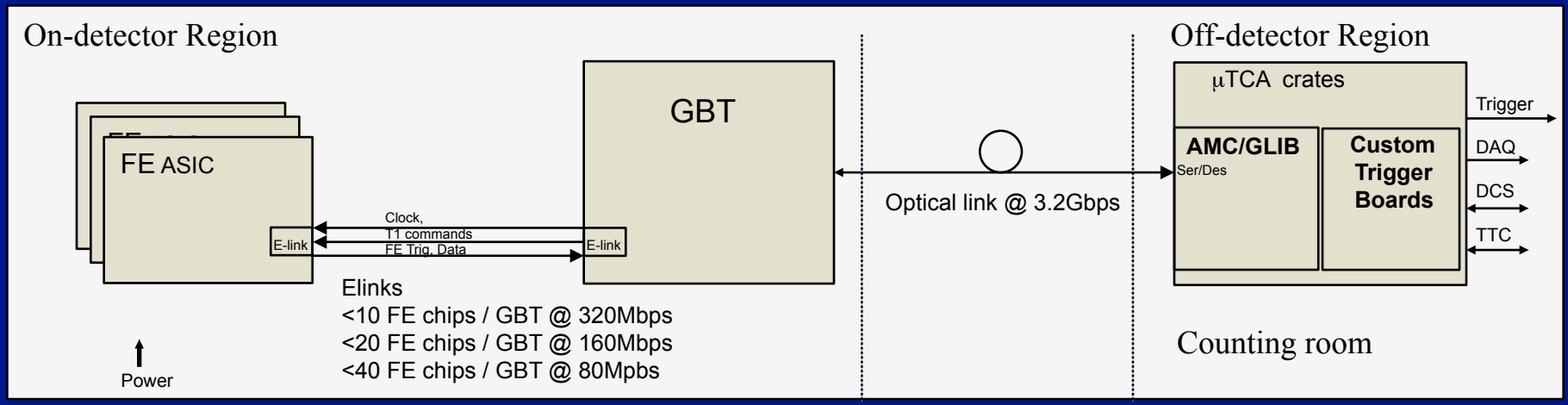
Off Detector Electronics & Interface to Trigger

Prototype development readout systems

LHC Planning

Differences between LHC and LC

LHC-Upgrade style readout system



Benefit as much as possible from generic projects in CERN for :

GBT

[The GBT is currently foreseen for many LHC upgrades :
CMS tracker, HCAL, Atlas tracker, LHCb (all upgrades)]

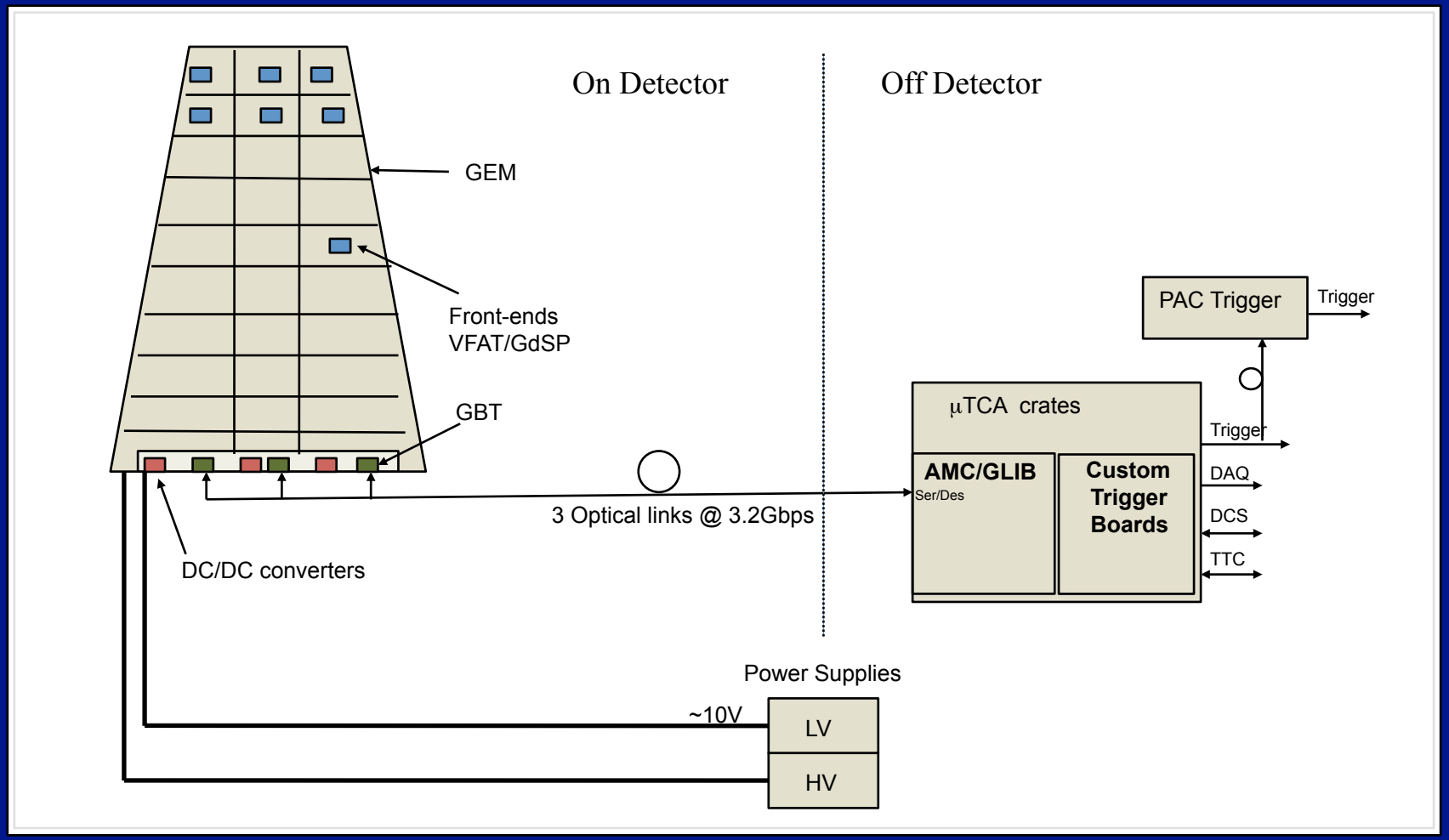
Versatile Link

DC/DC Powering

uTCA / AMC : GLIB

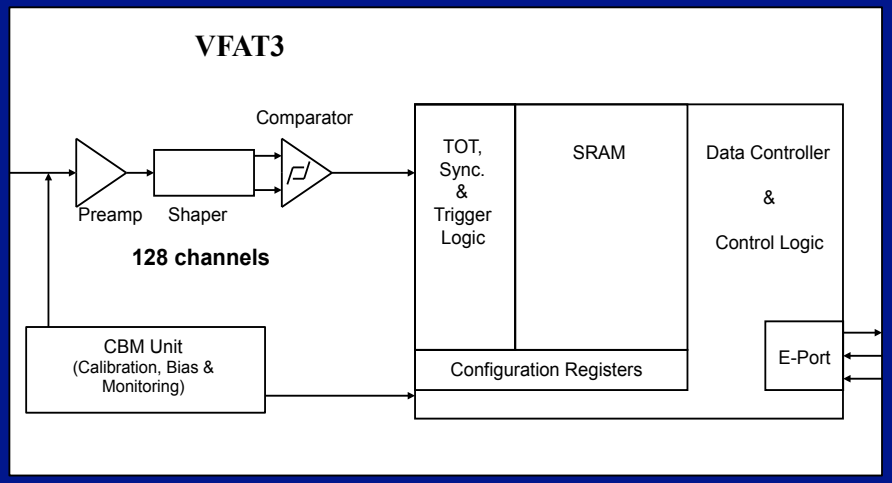
(Giga-Bit Link Interface Board)

GEMs for CMS System Architecture
VFAT3/GdSP ASIC design + uTCA design

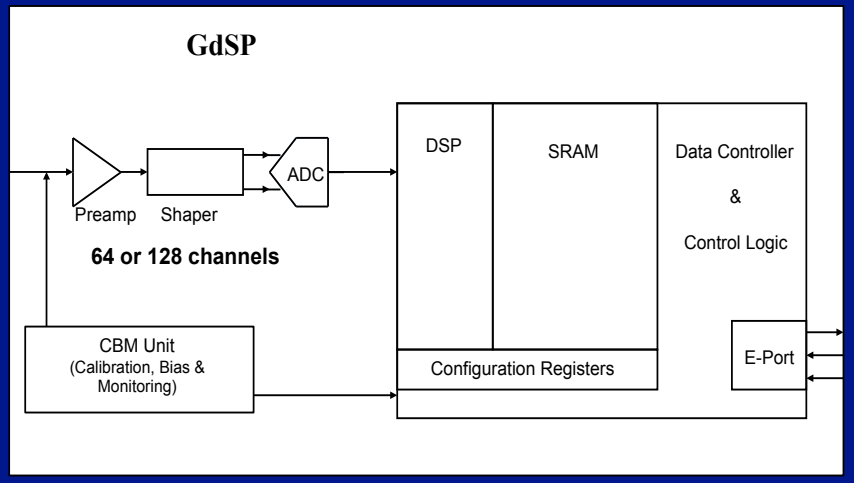


Front-end Microelectronics Design 2012-2015
VFAT3/GdSP ASIC design

2 Trigger & Tracking Front-end architectures considered.



OR



VFAT3 :

Front-end with programmable shaping time.

Internal calibration.

Binary memory

Interface directly to GBT @ 320Mbps.

Designed for high rate (10kHz/cm^2 depending on segmentation)

Design groups involved so far :
CERN
ULB (Brussels)
CEA Saclay
University of Bari

Approx. 8-10 man years of design work expected .

GdSP :

Similar to VFAT3 except has an ADC / channel instead of a comparator.

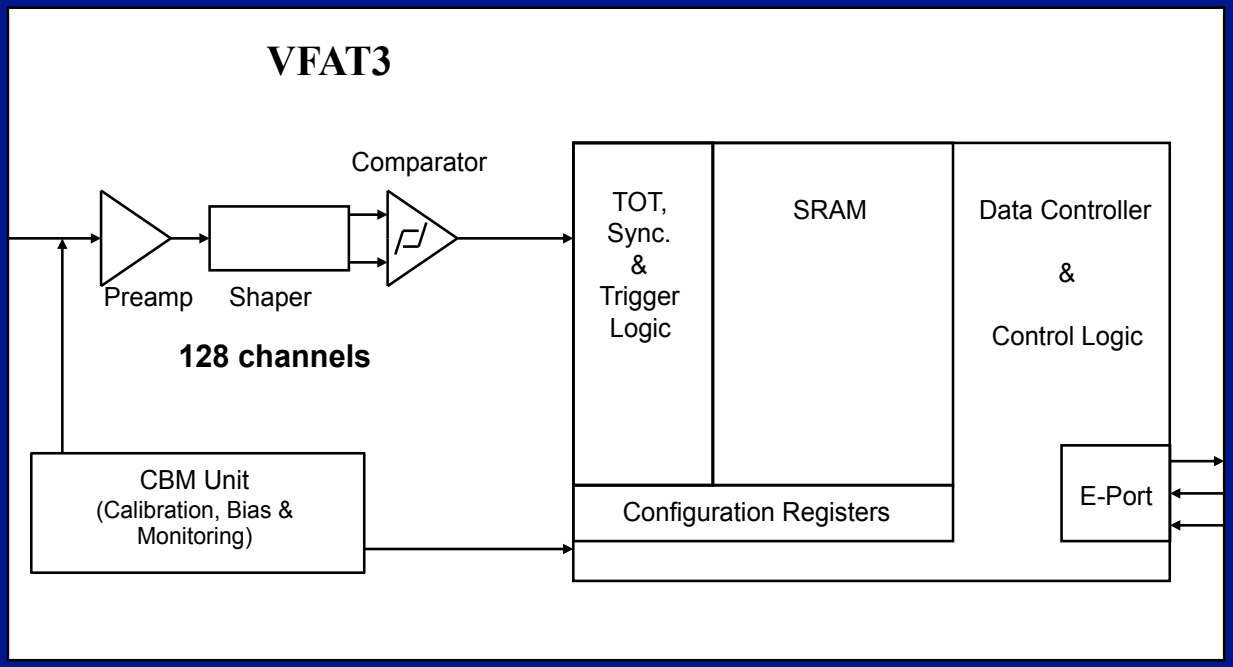
Internal DSP allows subtraction of background artifacts enabling a clean signal discrimination.

Centre of gravity a possibility to achieve a finer pitch resolution (if needed).

VFAT3

Main differences compared to VFAT 2

Programmable gain & shaping time.



Data packet structure for trigger/data at high rate.

Previous DCU functions for slow control integrated within the CBM unit.

Memory depth to be determined

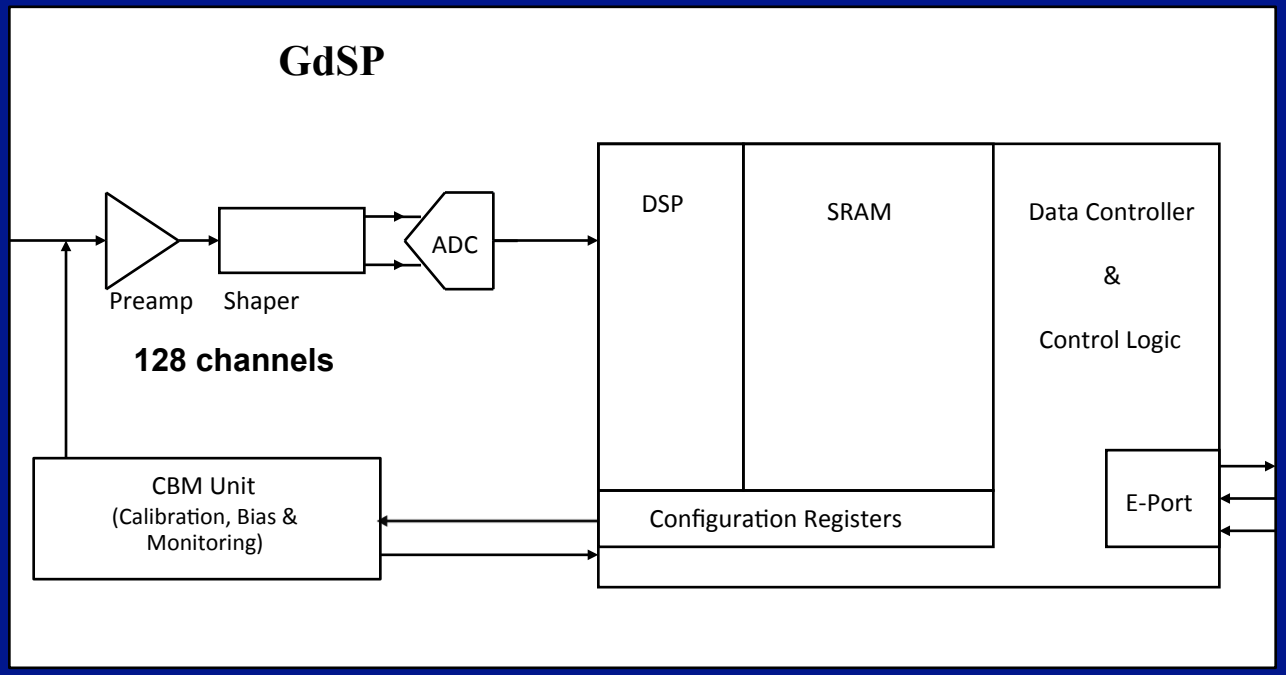
E-port Interface compatible with the GBT

0.13um CMOS

The GdSP (a possibility)

(Gas Detector Signal Processor)

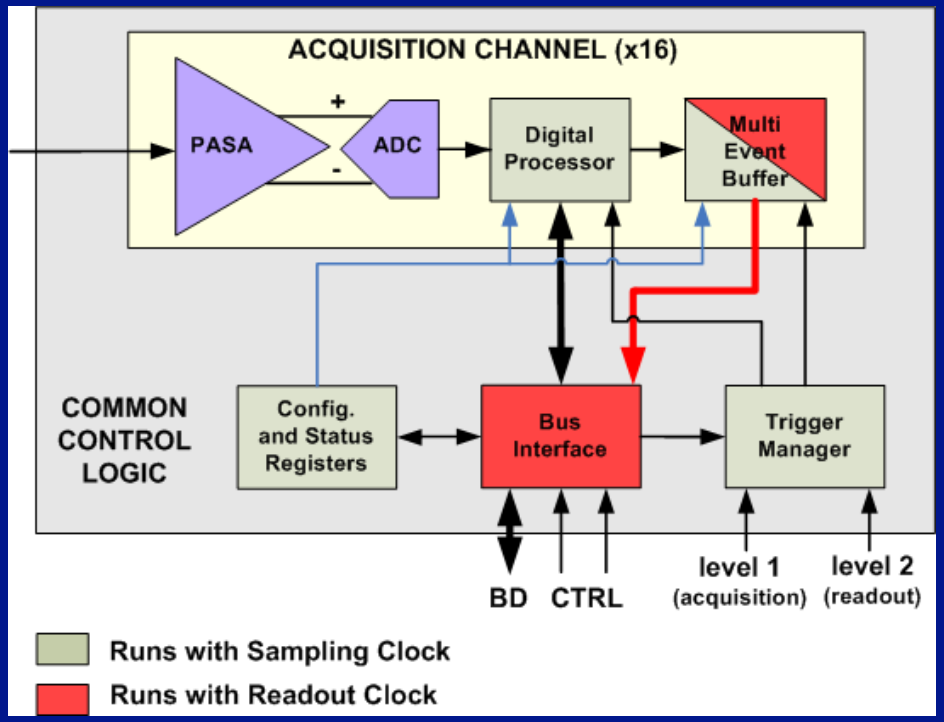
The GdSP, a 128 channel front-end ASIC designed specifically to tackle the needs of MPGD readout in the next decade.
A natural evolution of the SAltro architecture.



The GdSP is a possibility due to :

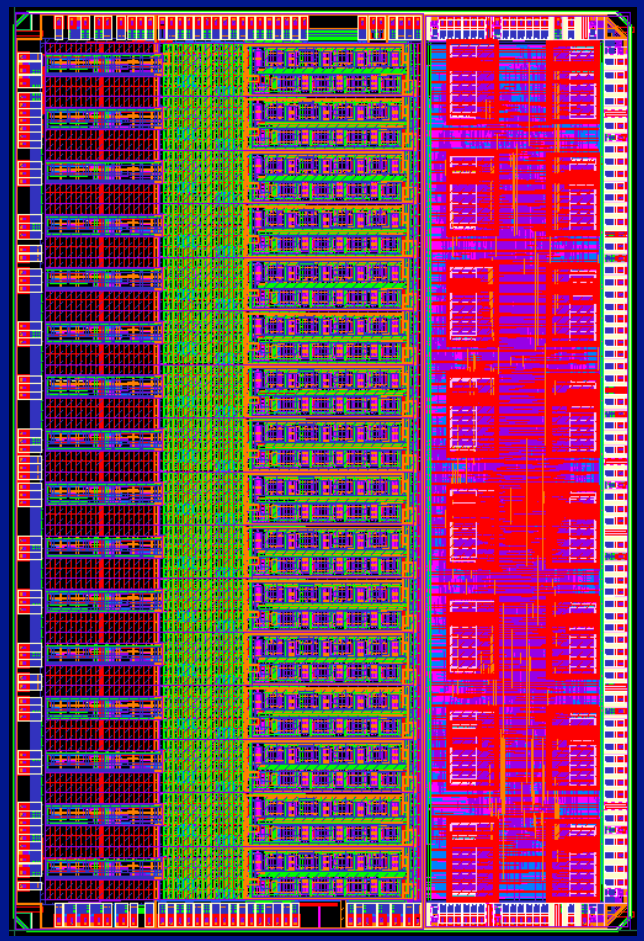
Very rapid IC trends in ADC power efficiency and Power Management techniques.

SAltro16



16 channel demonstrator chip designed in 2009-2010, Tested and working beautifully.

Technology : IBM 130nm CMOS



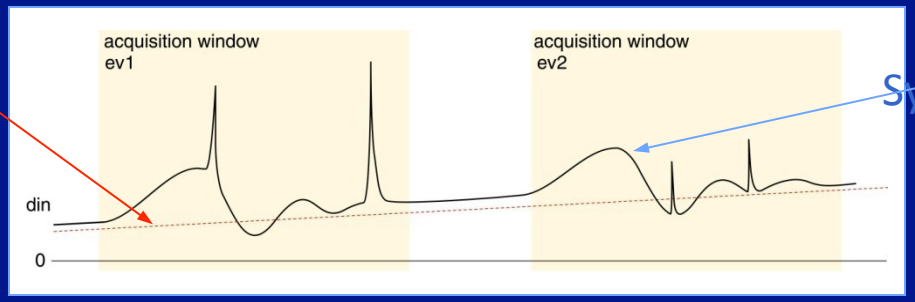
Luciano Musa …… S-Altro Specs. & Architecture
Paul Aspell …… Coordinator of design
Designers :
Massimiliano De Gaspari ……. Front-end + ADC
Hugo França-Santos ……... ADC core
Eduardo Garcia …… Data Processing & Control

Saltro Digital processing

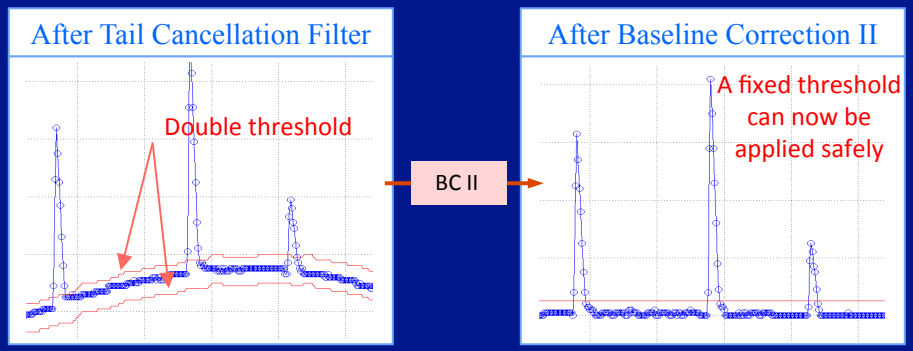
Baseline correction 1	Removes systematic offsets that may have been introduced due to clock noise pickup etc. The SRAM is used for storage of baseline constants which can then be used a look-up table and subtracted from the signal.
Tail cancellation	Compensates the distortion of the signal shape due to undershoot.
Baseline correction 2	Reduces low frequency baseline movements based on a moving average filter.
Zero suppression	Removes samples that fall below a programmable threshold.

Digital processing

Baseline drift



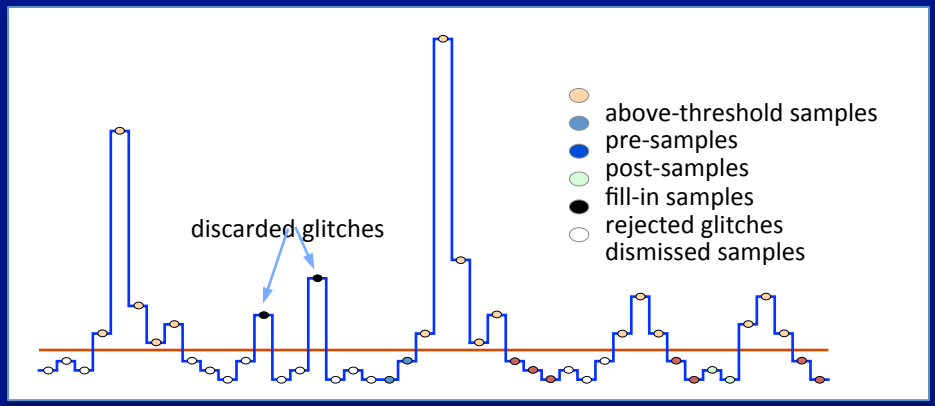
Systematic perturbation



Corrects on-chip for :

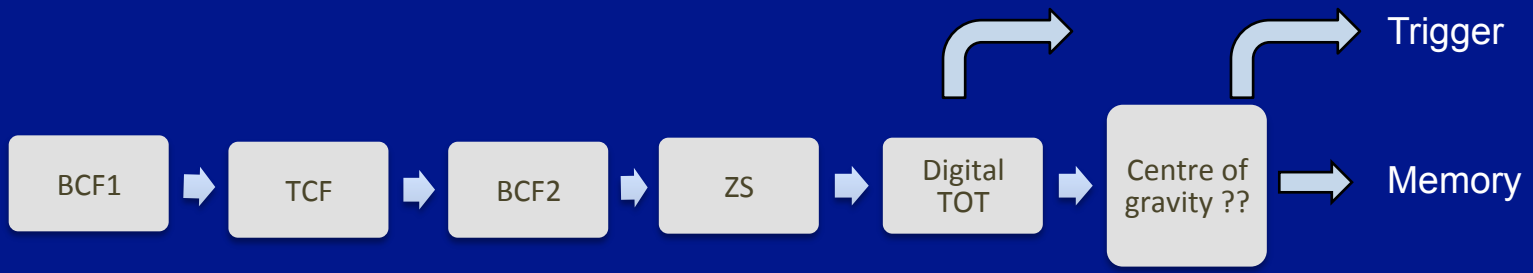
Systematic offsets,
Baseline movements
Ion tails
Removal of glitches

Zero-suppressed output



DP Design and simulations : Eduardo Garcia

GdSP Digital Processing



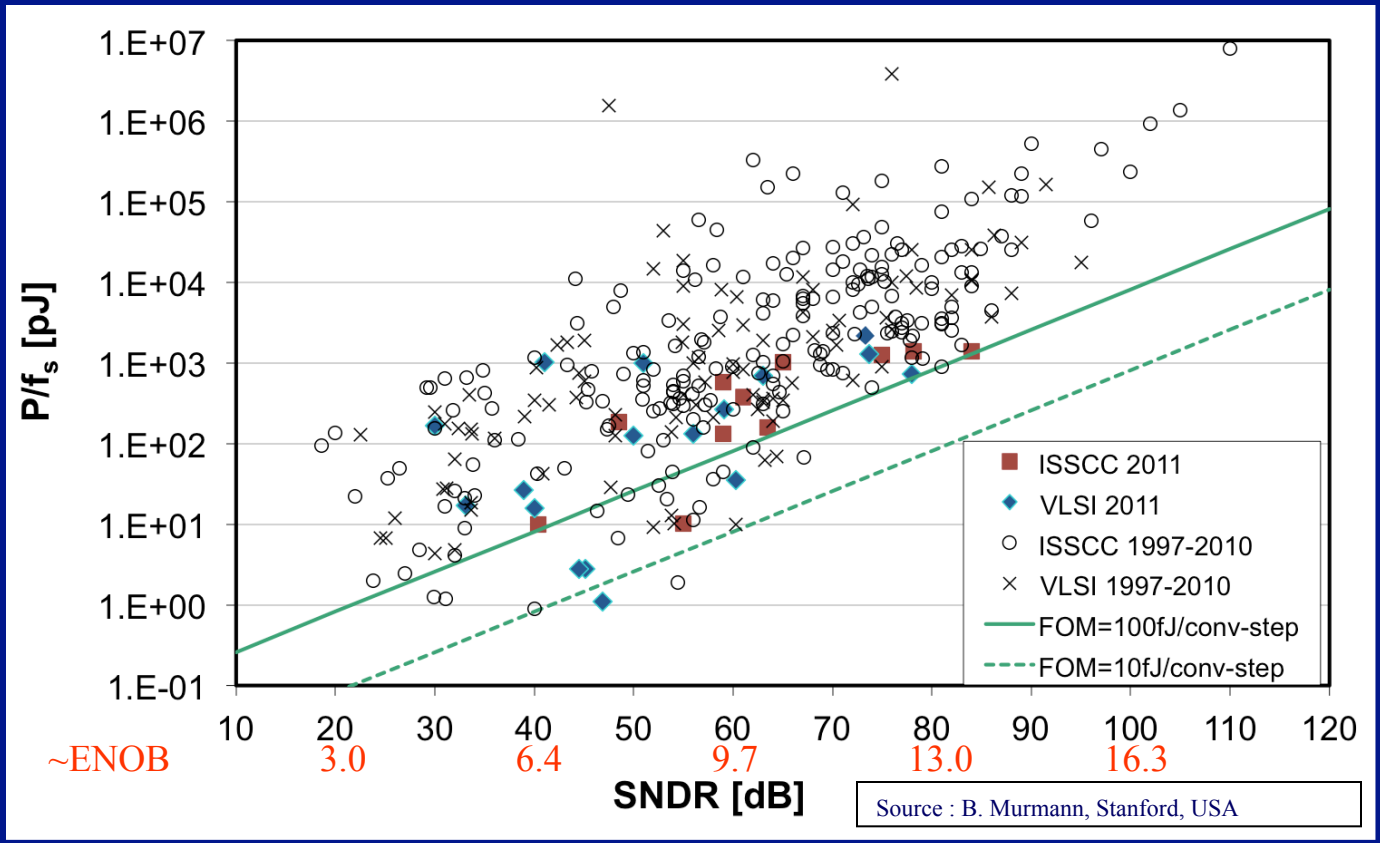
Not all stages are necessarily needed for all detectors.

Baseline correction 1	Removes systematic offsets that may have been introduced due to clock noise pickup etc. The SRAM is used for storage of baseline constants which can then be used a look-up table and subtracted from the signal.
Tail cancellation	Compensates the distortion of the signal shape due to undershoot.
Baseline correction 2	Reduces low frequency baseline movements based on a moving average filter.
Zero suppression	Removes samples that fall below a programmable threshold.
Digital TOT	To maintain accurate time resolution
Centre of gravity ??	Could be used to obtain a finer binary granularity. ?????

ADC Trends

- FOM ~ P / (2^{ENOB}. 2BW)

- 1pJ is high
- (~40mW @ ENOB 9, 40MS/s)
- 100fJ is good
- (~4mW @ ENOB 9, 40MS/s)
- 50fJ excellent
- (~2mW @ ENOB 9, 40MS/s)

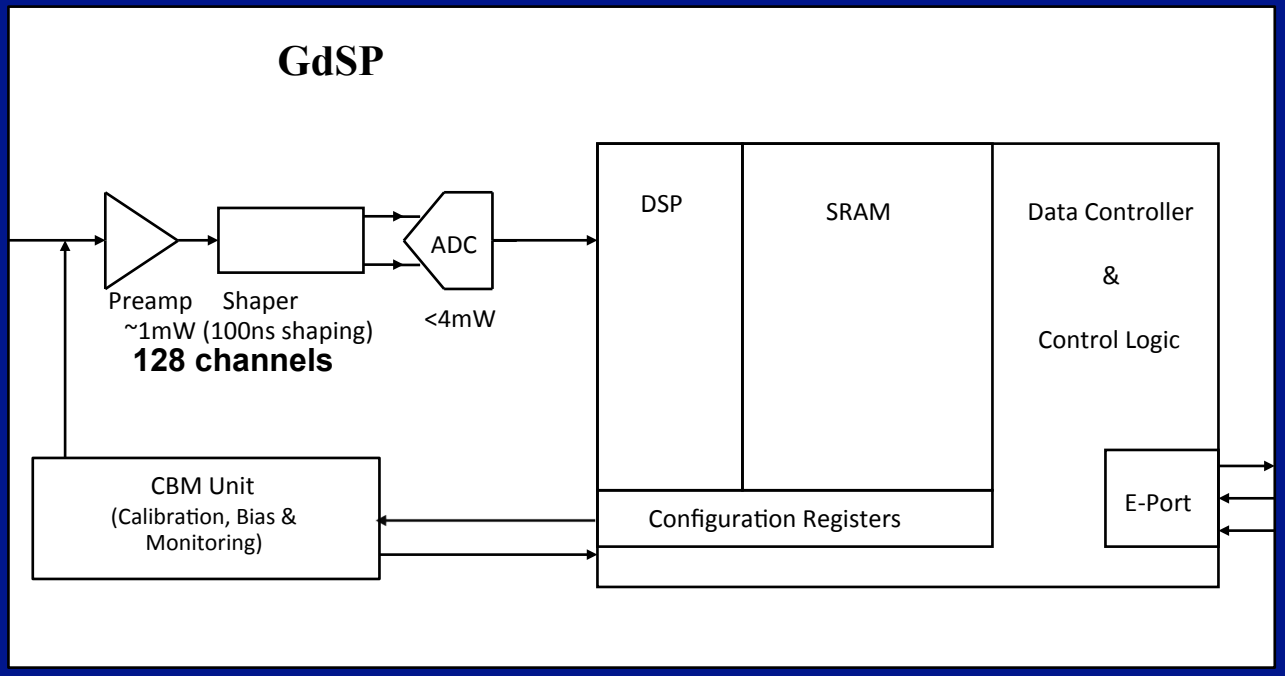


State of the art :

A 30fJ/conversion 8b 0 to 10MS/s Asynchronous SAR ADC in 90nm CMOS. P. Harp et. al. IMEC ISSCC 2010
[They measured 69uW at 10MS/s,]

A 550uW 10b 40MS/s SAR ADC with Multistep Addition-only Digital Error Correction, *Sang-Hyun Cho et al.*
CICC 2010 *(FOM = 42fJ/conversion)* designed in 0.13um CMOS

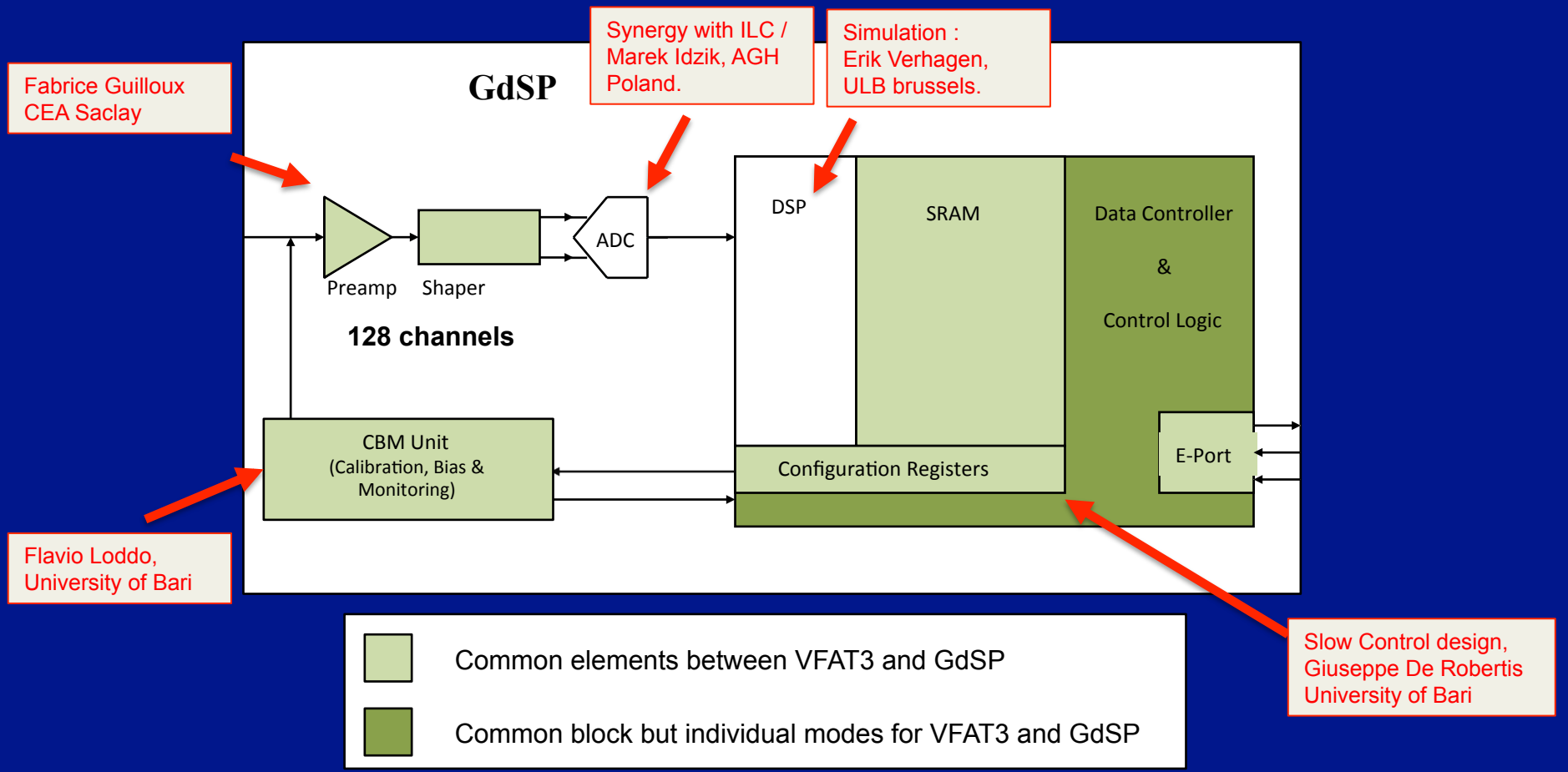
Estimate GdSP power consumption



128 channels = Analog power 640mW + Digital power ~ some hundreds mW.
Approx. ~900mW / chip.

Should be possible to get 7-8 mW/ch for everything on a 128 ch chip.

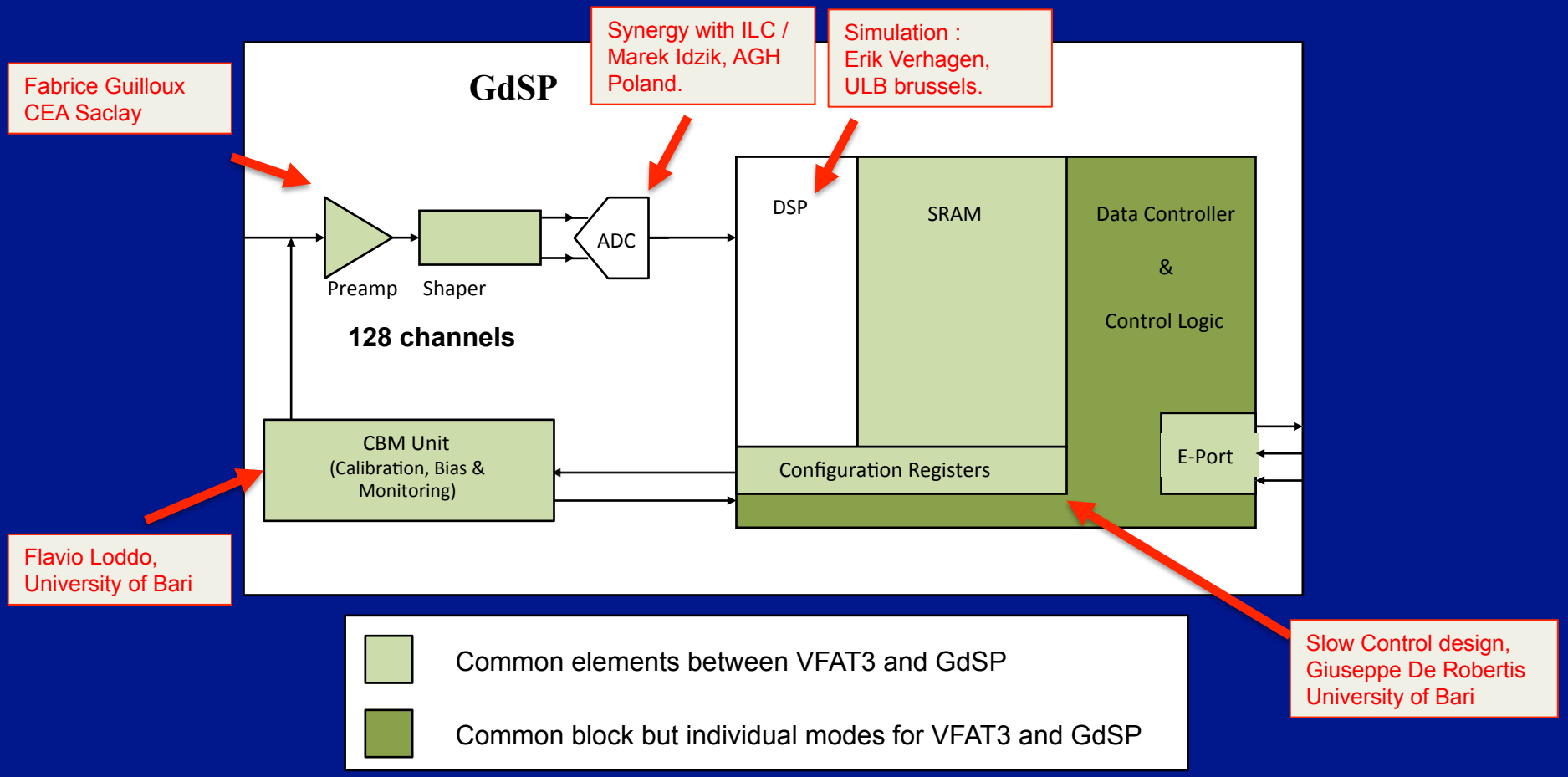
Microelectronics design



2011 : Define global architecture and design team (approx. 8-10 man years needed).
2012 : Initial focus on VFAT3/GdSP elements needed for architecture choice and common architecture building blocks.
Aim to complete design by 2015.
Design team not yet complete .

Coordination :
Paul Aspell, CERN

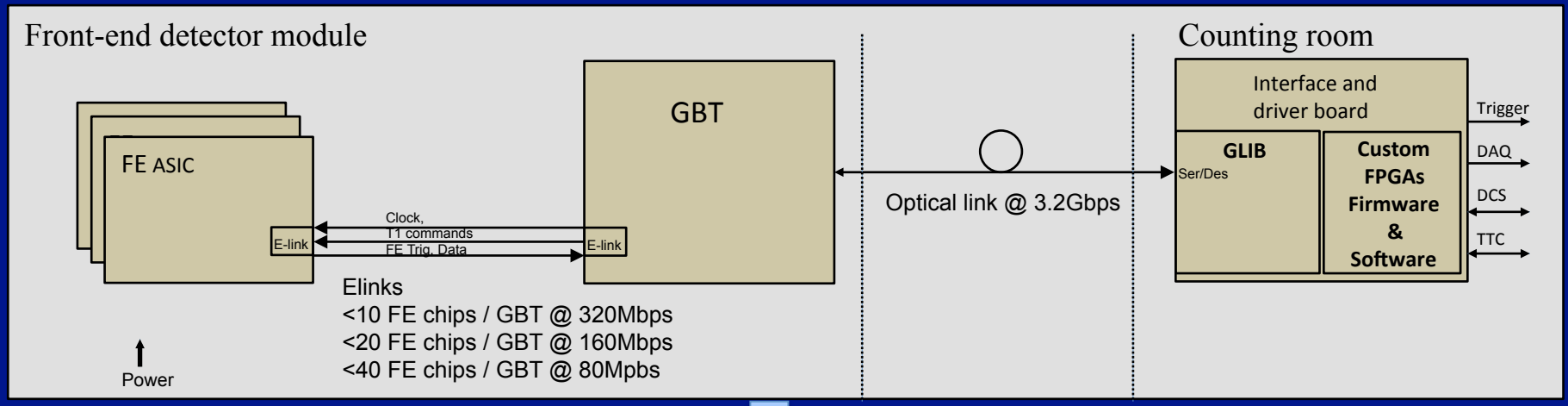
Microelectronics design



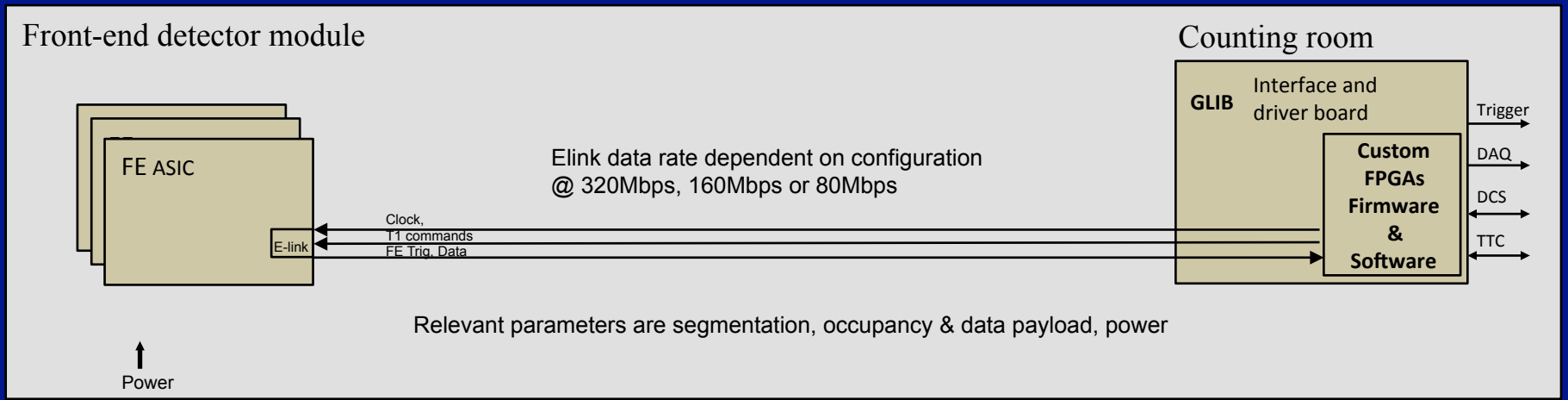
Groups from Aida or LCTPC please contact me if interested in joining the design team !

Coordination :
Paul Aspell, CERN

Equivalent point to point communication from FE ASIC to counting room

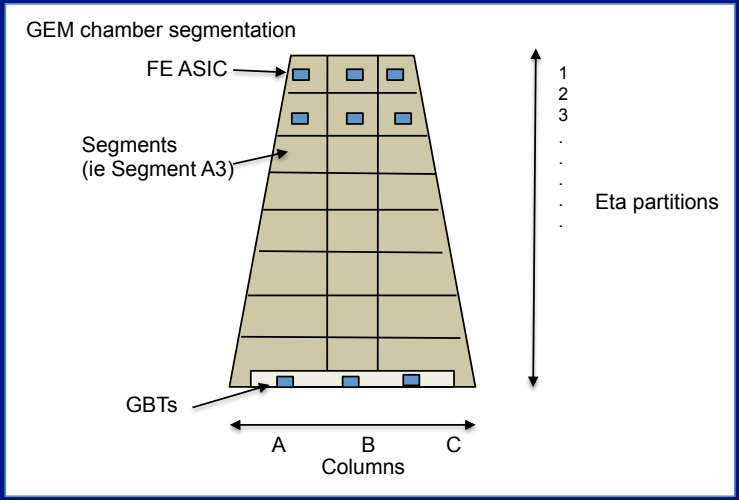


The GBT and optical links are transparent ie. the 2 diagrams are equivalent



Considered as a continuous data stream output from the FE to counting room.
We are free to choose our data packet structure.

GEM segmentation.



	Increasing Eta Partitions	Increasing columns
Area cover by one chip	↓	↓
Strip area and capacitance	↓	↓
Noise	↓	↓
Strip pitch	–	↓
Rate capability	↑	? ↓
Power	↑	↑
Cooling needs	↑	↑
Cost	↑	↑

Increasing eta partitions: increases particle rate capability and also increases power/cost.

Natural design for the electronics would be 3 columns and 10 eta partitions per chamber.

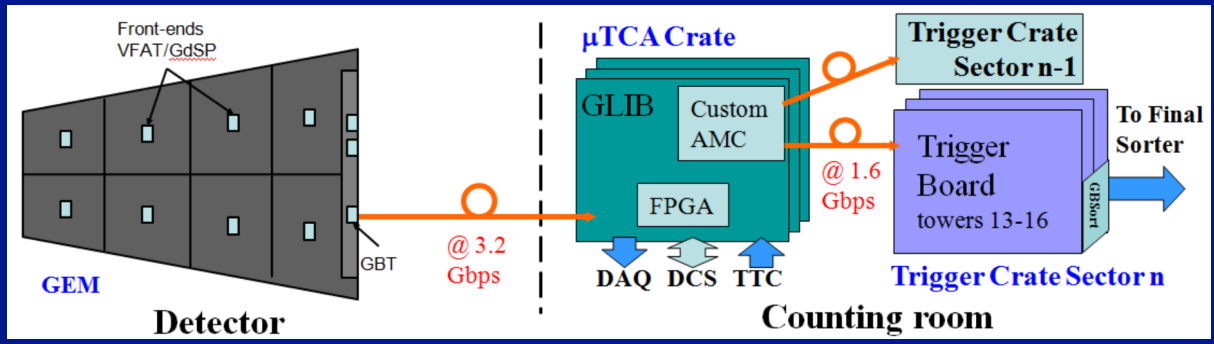
Studies by Karol and myself conclude that a GE1/1 GEM segmented in a 3x10 format would be able to run at rates of 10kHz/cm^2 with minimal losses.

Chart for 3x8.

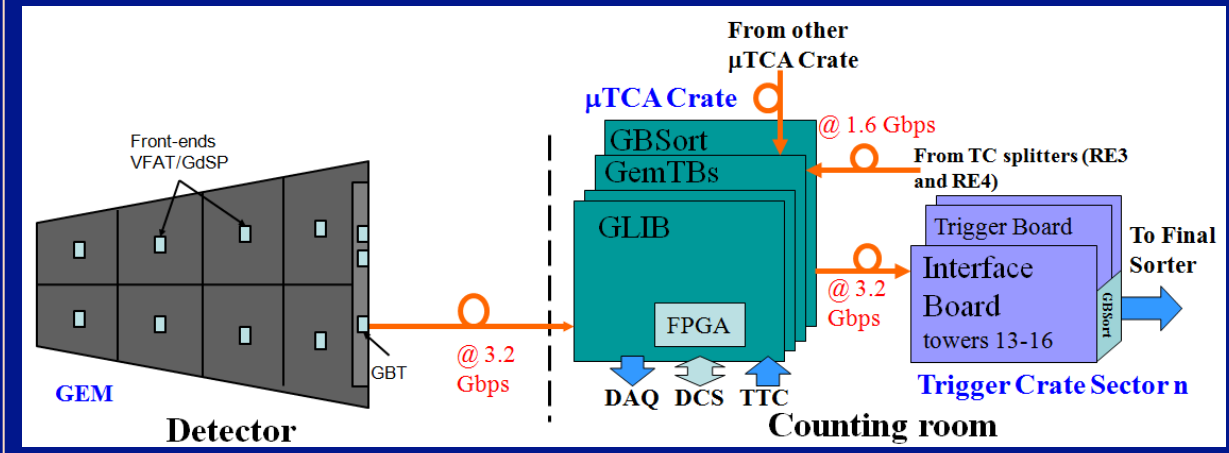
Rate Hz/cm^2	Rate Hits/chip/BX	Lost frame fraction			
		Cluster size 1 = 1 frame/hit	Cluster size 2 = 1.25 frames/hit	Cluster size 3 = 1.5 frames/hit	Cluster size 4= 1.75 frames/hit
2 339	0.01	$<10^{-8}$	8×10^{-6}	4×10^{-5}	5.2×10^{-5}
4 679	0.02	$<10^{-8}$	4×10^{-5}	1.4×10^{-4}	3.1×10^{-4}
11 697	0.05	$<10^{-7}$	2.6×10^{-4}	0.001	0.0027
23 393	0.1	1.4×10^{-5}	0.0015	0.007	0.014
46 787	0.2	7×10^{-4}	0.015	0.04	0.08

Interfacing to and from the RPC trigger

Option A:
- uTCA crate converts GEM data to RPC PAC data format.
- RPC TB for the trigger algorithms.
- GEM data ORed to RPC granularity and sent @ 1.6Gbps.



Option B:
- Integrated GemTB in uTCA crate.
- Allows full granularity in trigger algorithm.
- Receive data from RPC RE3/1, RE3/2, R4/1 and RE4/2.
- Local sorting & ghost busting of muon trigger candidates.
- Candidates transmitted to Trigger crate.
- If super chambers (double layer) then Δphi for muon pT measurement.

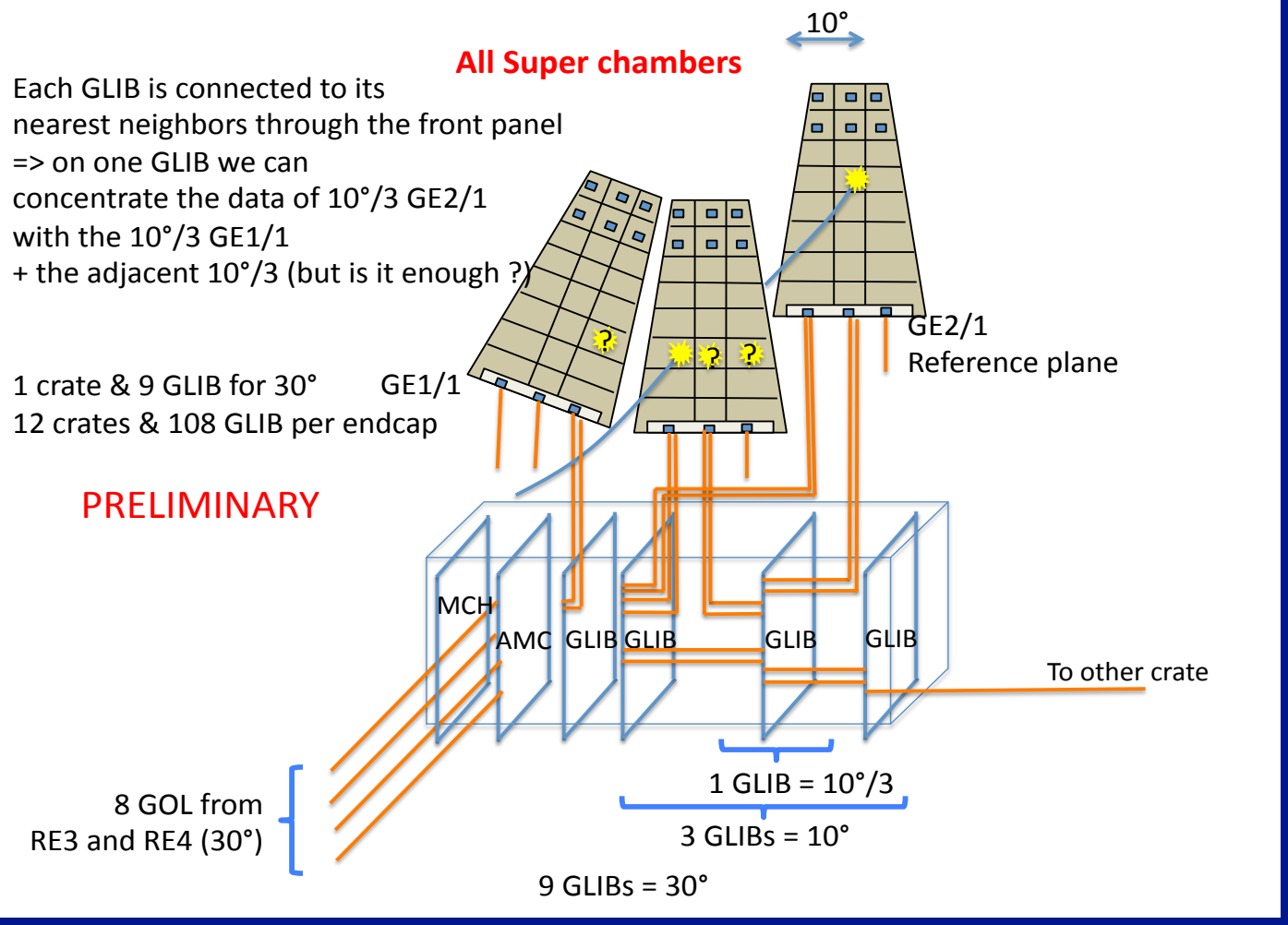


Options B & C are currently the preferred options.

Option C:
- Option B including compatibility with any future RPC trigger upgrade.

Figures from :
K. Bunkowski

Off Detecor uTCA Electronics



Source : G. De Lentdecker (ULB)

A possible off detector partition

1 AMC/GLIB = one phi column ie. 10°/3 GE21 (2links), GE11 (2 links + 4 neighbours)

1uTCA crate = 30° degrees in phi (1 or 2 AMC boards to receive RE3 and 4 data.

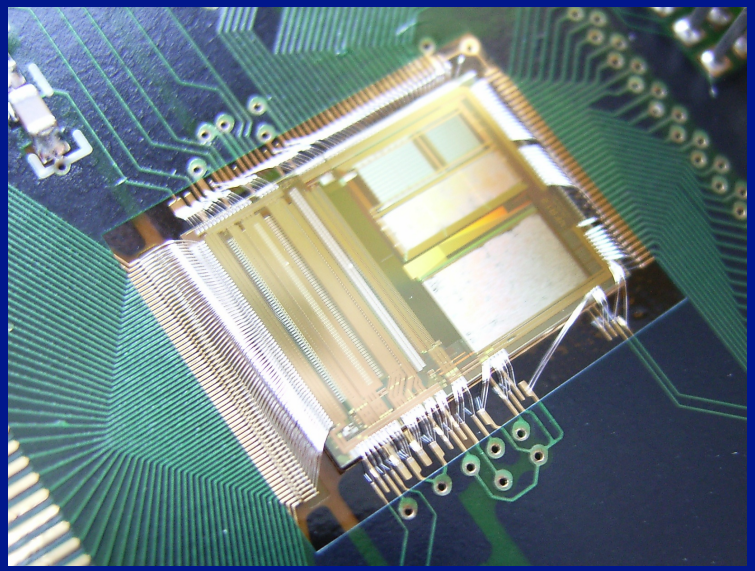
12 uTCA crates = 360°

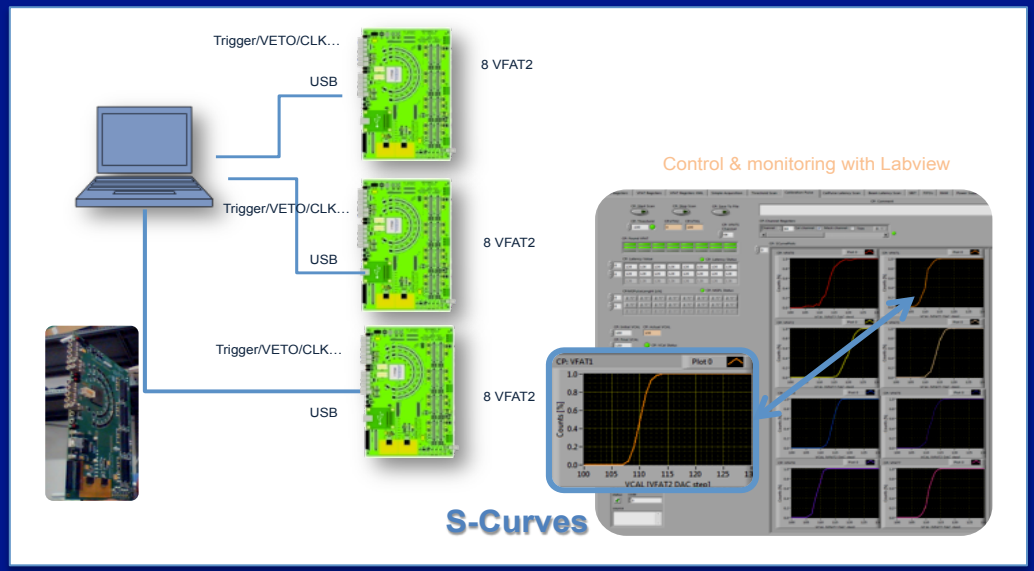
24 uTCA crates for both endcaps

Scheme currently under investigation.
Not yet fixed.

"Short Term" : Electronics Prototype System 2011-2012
VFAT2 + Turbo readout system

VFAT2 "Tracking and Triggering" front-end ASIC design at CERN.
Originally designed for the TOTEM project, GEM and Si detectors.

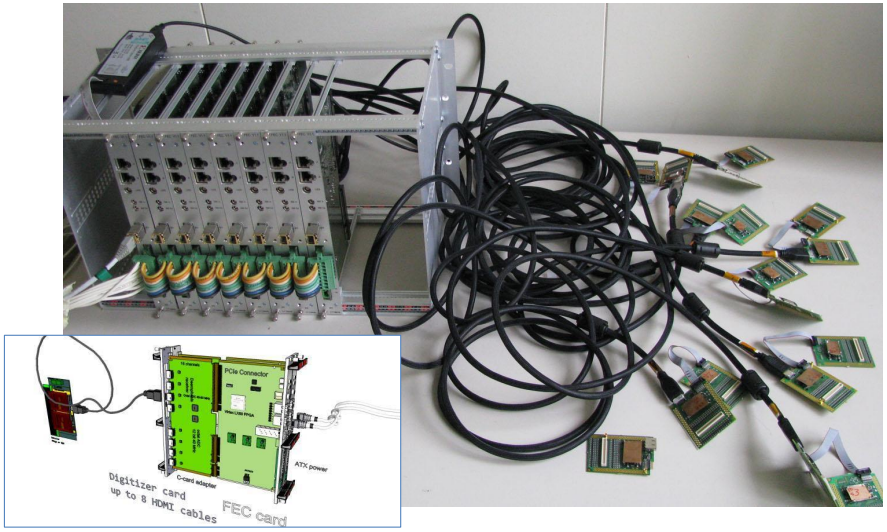




Used together with the Turbo readout system developed in Sienna.

"Medium Term": Electronics readout system for 2012-2014
Prototypes: VFAT2 + Turbo & SRS readout system

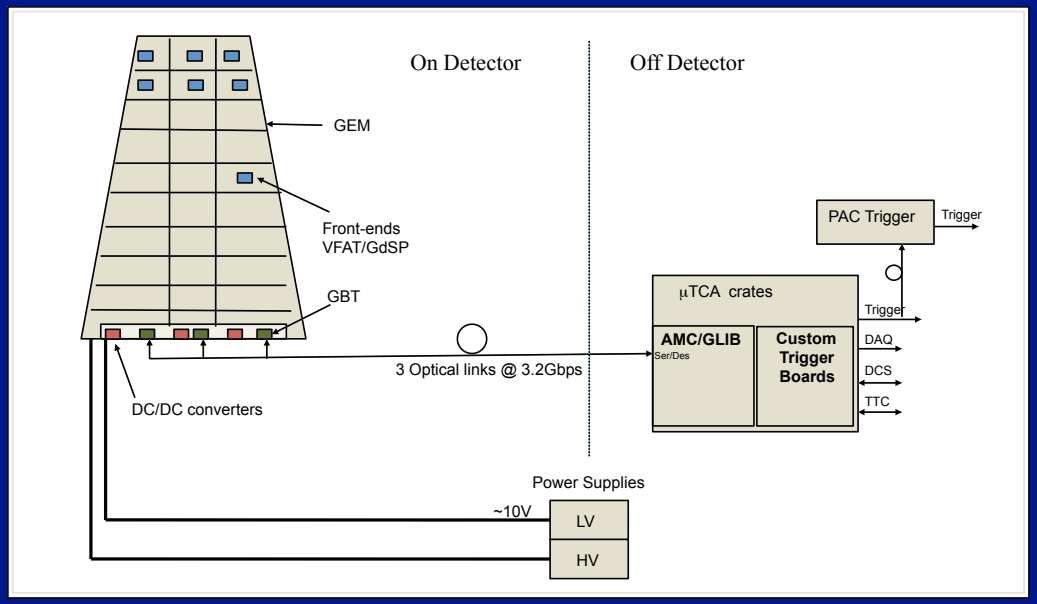
Scalable Readout System



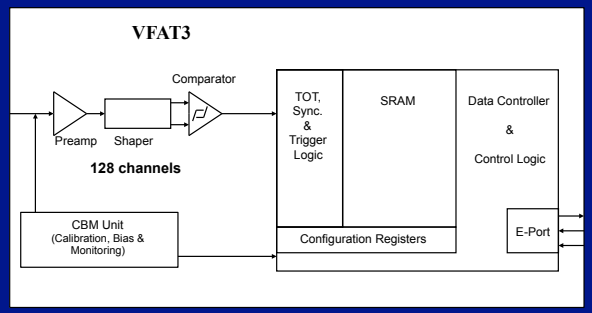
New VFAT2 hybrid and SRS interface

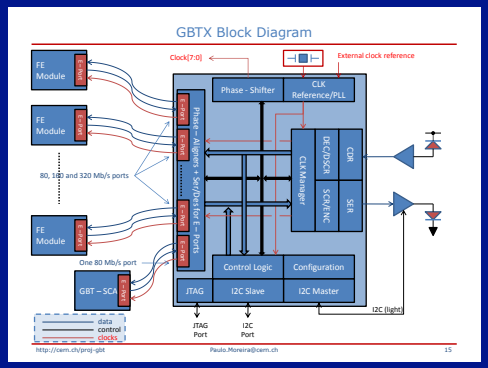
Currently being designed by Sorin Martoiu (CERN)

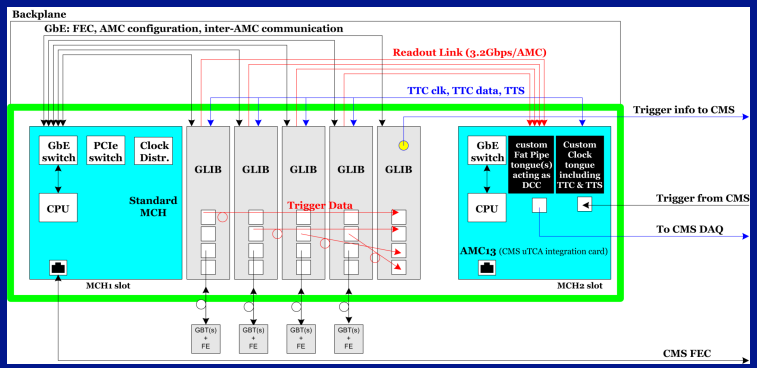
Electronics 2015->
Prototypes : VFAT3/GdSP + GBT + uTCA

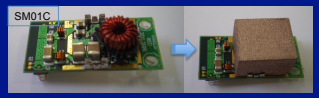


Designs currently involving :
CERN
Brussels
Bari
Saclay (in conjunction with the ILC)









Electronics Planning

FE ASIC

Define electronics system for TP,
Formation of design teams.

ASIC design starts

FE ASIC design team
Approx. 8 man years
of design time
needed.

Submission of FE AISC (VFAT3/GdSP)

Readout systems

2011

Short Term :

VFAT2 , Turbo hardware and Labview DAQ software

2012

We are here.

Medium Term :

VFAT2 + SRS

Off Detector
uTCA development

2014

Long Term :

2015

Full and final system
On & Off detector electronics.
VFAT3/GdSP + GBT + uTCA system

GdSP for LC operation

The GdSP could be an option for the LC

The LC can benefit from the fact that CMS needs it first.

However, design is similar but different.

LHC needs trigger
LCTPC doesn't

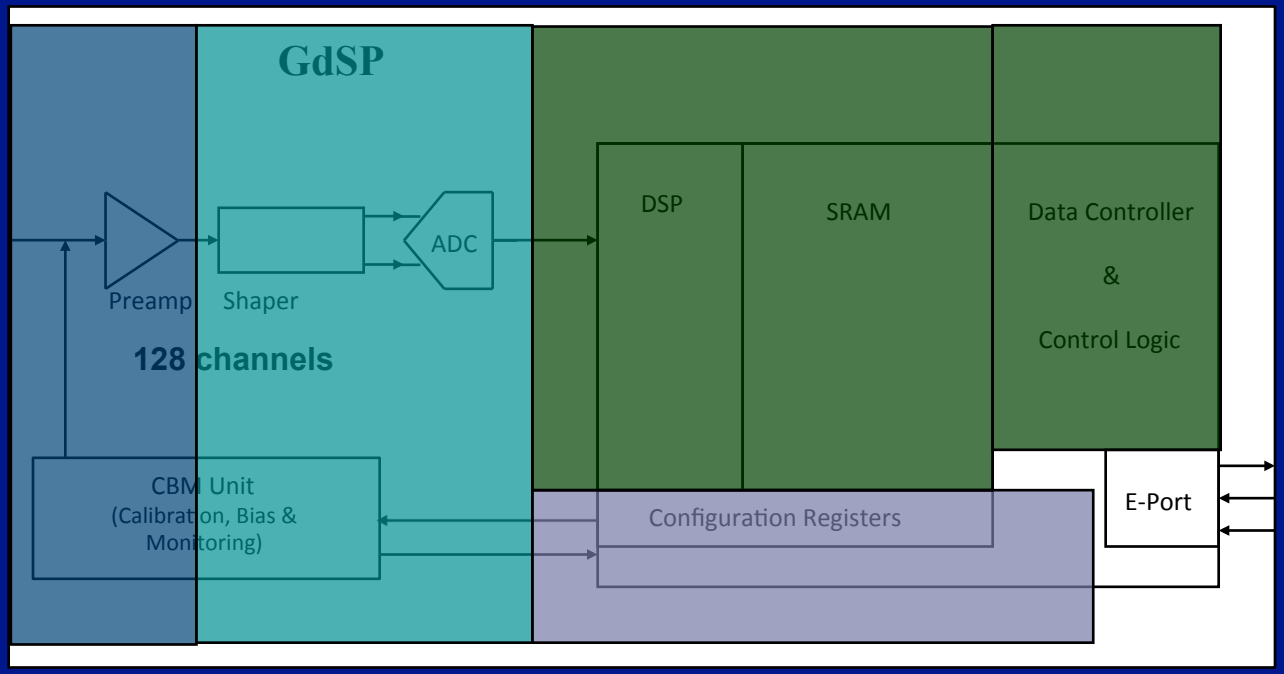
LHC needs continuous operation
LC needs burst mode.

LC needs power pulsing / power management

LC requires different memory capacity and different data packet

An institute interested in studying/simulating these points would be very welcome, as would a microelectronics digital designer, please contact me.

Power Pulsing : Power Management with multiple power domains



Preamp > Reduce current via bias control, important to maintain a low impedance on the electrode.

Shaper > Reduce current to approx. zero via bias control. Vdd could be maintained.

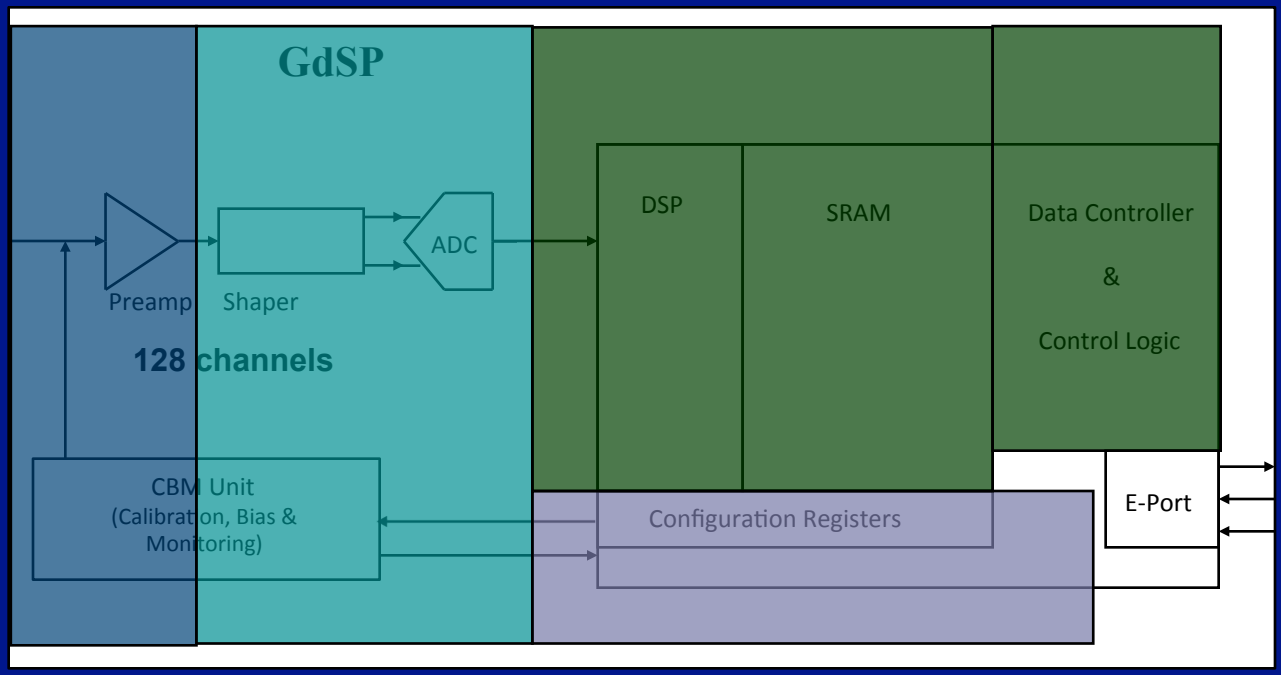
ADC > Stop clock and reduce current to approx. zero via bias control. Vdd could be maintained.

Configuration reg.s > Reduce Vdd to minimum voltage necessary to hold data.
Current consumption limited to leakage currents.

Digital logic > Switched off by reducing Vdd to 0V.

Power Pulsing Phases

"Sampling", "Read" and "Sleep" phases controlled by synchronous commands.



"Sampling" Phase = All modules "Up".

"Non Sampling" Phase = Preamp, Shaper and ADC "Down",

"Read" Phase = Preamp, Shaper and ADC "Down", DSP RAM Configuration Reg.s and E-ports "Up"
"Sleep" Phase = Preamp, Shaper, ADC, DSP, RAM "Down", Configuration Registers and E-port "Up".