Status of the Medipix3 TSV project

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Outline

- Medipix3 TSV project description
- Status reports
  - Phase 1
  - Phase 2
  - Phase 3
- Conclusions & outlook

Medipix TSV project description

Phase 1: TSV processing of Medipix 3 wafers

- Adapt the CEA-LETI TSV process to Medipix 3 wafers
- Process 10 Medipix3 wafers with TSVs
- CEA-LETI contract participants: Medipix3, ALICE, CLIC, ACEOLE and AIDA

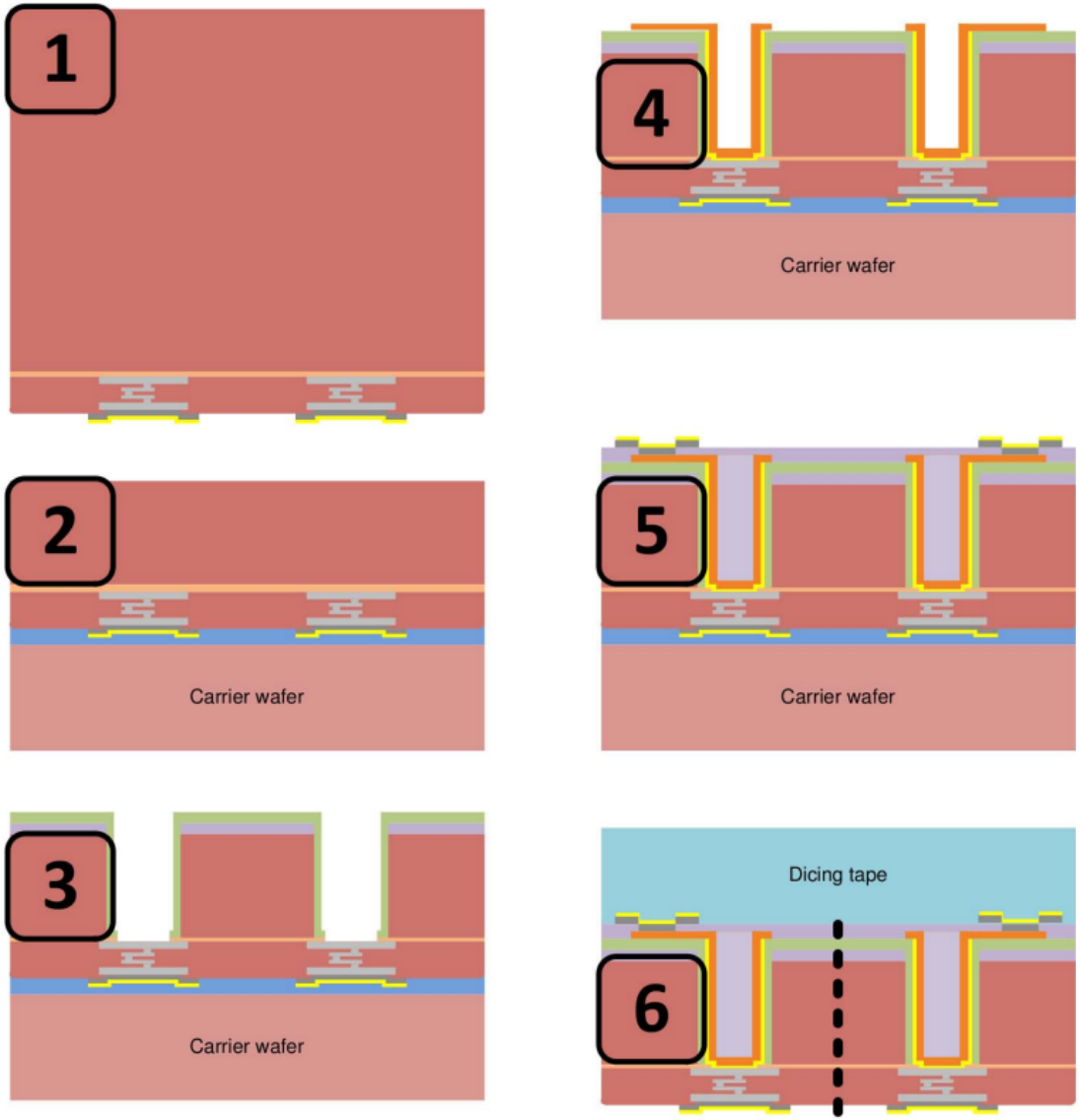
Phase 2: Hybridization of the TSV processed read out chips

- Dicing the wafers
- Develop handling and FC bonding procedures for thin chips
- Prepare a number of functional assemblies
  - Edgeless or traditional sensors, depending on the availability
- Electrical tests

Phase 3: Demonstrator module

- Build a 3x3 or 4x4 size detector module

CEA-LETI “via last” TSV process flow



1. UBM deposition
2. Temporary bonding to support wafer and thinning
3. Via etching and isolation
4. Cu deposition and patterning
5. Backside passivation and UBM deposition
6. De-bonding of support wafer and attachment to dicing tape

http://iopscience.iop.org/1748-0221/6/11/C11018/pdf/1748-0221_6_11_C11018.pdf

Phase 1 status 03.2012

- Lot 1: ready and tested
  - Few problems in the process:
    - A bug which resulted high contact resistance to front side UBM: fixed for lots 2 & 3
    - Copper deposition problem in wafer P02 - the wafer was stripped of copper and dropped to Lot #2
    - Isolation problem, some vias have high leakage current
  - P01 diced - Problem with releasing chips from the tape
  - P02 dropped to lot 2
  - P03 sent back to CEA-LETI, tape released, waiting for dicing at LETI
- Lot 2: ready and tested
  - Some issues with the process (seed layer deposition) – low yield
  - Waiting for dicing and chip testing – low priority
- Lot 3: Preliminary measurements done
  - Switch to a new and better metal deposition equipment – huge improvement in copper seed layer conformity
  - Lot divided to optimize the process
  - First measurements on test structures done, promising results
    - Via resistivity 100% yield from test structures
    - Isolation better than Lot 1, some variation over the wafer though
  - UBM deposition ongoing, final results next week
  - Looks good!

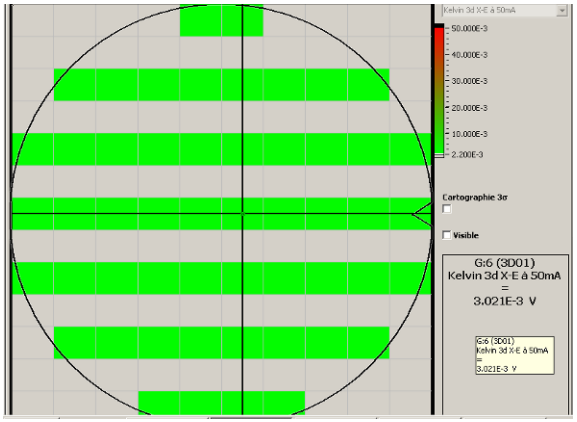
Very preliminary results LOT 3

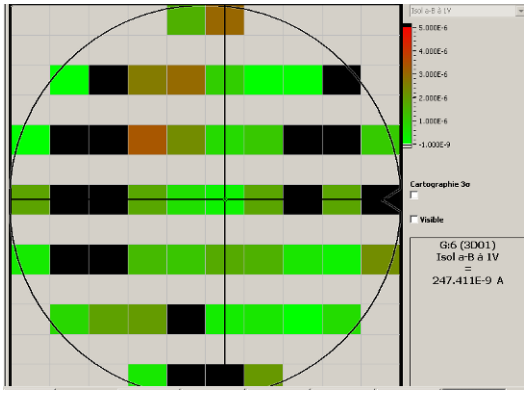
Measurements on TSV test structures, performed at CEA-LETI

Green
Resistance under 1 ohm

Black
Leakage over 10^-6 A @ 1V

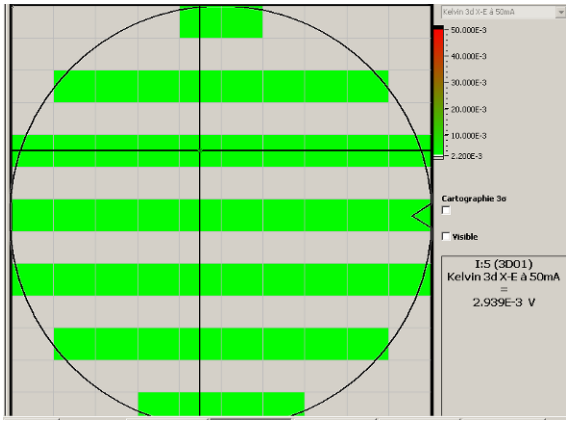
P01

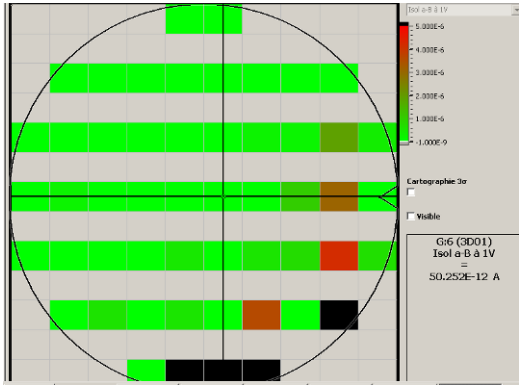




15% bad isolation

P03

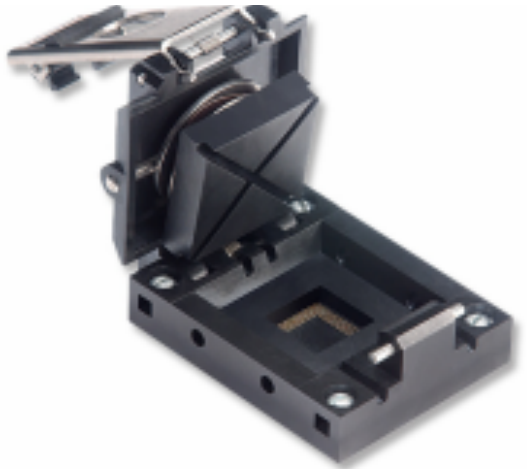




4% bad isolation

Phase 2 status 03.2012

- Order in place with VTT
  - Dicing of wafers, chip picking and inspection
  - Flip chip assembly of 20 chips
- Availability of sensors currently a minor problem – a rush order in place at VTT
  - We have 4 bumped singles (not perfect) with thick solder bumps, as backup for TSV assemblies
- Test board with a probe socket that allows testing bare chips and assemblies is being designed
  - Test socket ready
  - PCB is being designed
  - Expected to be ready 04-2012



Phase 3 status

- A joint development is planned with LHCb collaboration
  - A light weight Kapton extension cable is being designed to connect TSV processed Medipix3 chips to an existing read out electronics
- Scheduled to be fabricated by the end of 2012

Conclusions & outlook

- Wafer processing:
  - Lot 1: Processed, waiting for dicing & chip picking
    - Wafer P03 tests reasonably good, class A chips will be used to make assemblies
  - Lot 2: Processed, waiting for dicing & chip picking
    - Yield problem, chips need to be tested to verify usability
  - Lot 3: Preliminary measurements done for 2 wafers
    - Promising preliminary results, final results next week
- FC bonding planned at VTT as soon as chips and sensors are available
  - Estimated 04-05 2012
- Test board is currently being built
  - Ready 04-2012

Backup slides

List of TSV Test Structures

2 TSV chains
TSV Kelvin structures (four point measurement)
Capacitive TSV structures (oxide thickness)
UBM-ALU contact resistance on front side
RDL serpentine for thickness measurement
RDL-UBM contact resistance
UBM serpentine for thickness measurement
TSV to bulk isolation test structure

+ all the process monitors for alignment, lithography, line widths, etc...

TSV process description

- Under Bump Metallisation is deposited on the front side of the wafer. This is identical to the step used normally by the bump bonding suppliers and will permit the finished die to be flip chip assembled to sensors which have been bumped with a solder bumps.
- The front side of the wafer is bonded using a temporary adhesive to a dummy support wafer. The wafer is then thinned to 120 um (2 times the diameter of the TSV opening).
- Vias are drilled in the wafer using deep reactive ion etching and the vias are coated conformally with an insulating layer.
- Contact holes are etched through the insulation in the bottom of the vias and a 5um thick Cu layer is deposited on the side of the vias and on the back side of the wafer. The Cu layer is then etched to form the redistribution layer on the backside.
- The back side of the wafer is passivated and the openings for the BGA contacts etched. An UBM metallization is deposited on the BGA contact pads the same way as on the front side.
- The wafers are released from the support wafer and transferred onto a dicing tape. Finally the wafers are shipped for subsequent dicing and flip chip assembly.