Design of an area-effective small digital cell library for pixel readout chip

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Outline

1) Library design targets

2) Library description

3) Current status

Library design targets

The library is optimized for area, for small logic block building

1) there are no well and substrate taps in the cells, separate „TAP” cell is used

2) PMOS/NMOS are not balanced

3) Cells not optimized for routing density - there is some routing in the MET2 layer in d-flop and latch cells

4) D-flops and latches have no buffered outputs, separate buffers available

5) set and reset signals of the D-flops are not connected internally (have to be connected externally)

Routing information – CMOS GF130nm

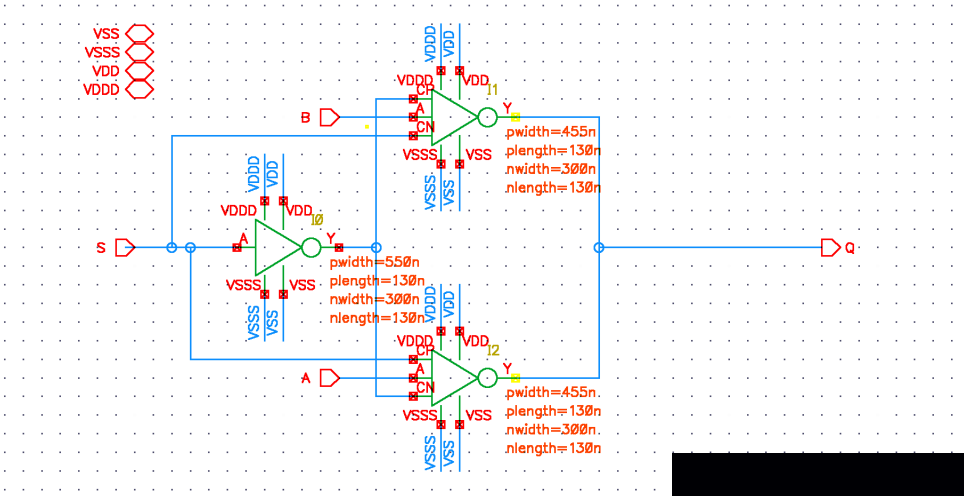
Metal	routing direction	pitch[μm]	offset [μm]
MET1	vertical	0.51	0.255
MET2	horizontal	0.48	0.0
MET3	vertical	0.51	0.255
MET4	horizontal	0.48	0.0

Row height: 2.4 *μm*
Placement x-pitch: 0.51 *μm*
Power net name: VDD
Ground net name: VSS
Substrate net name: VSSS, VDDD

Cell list

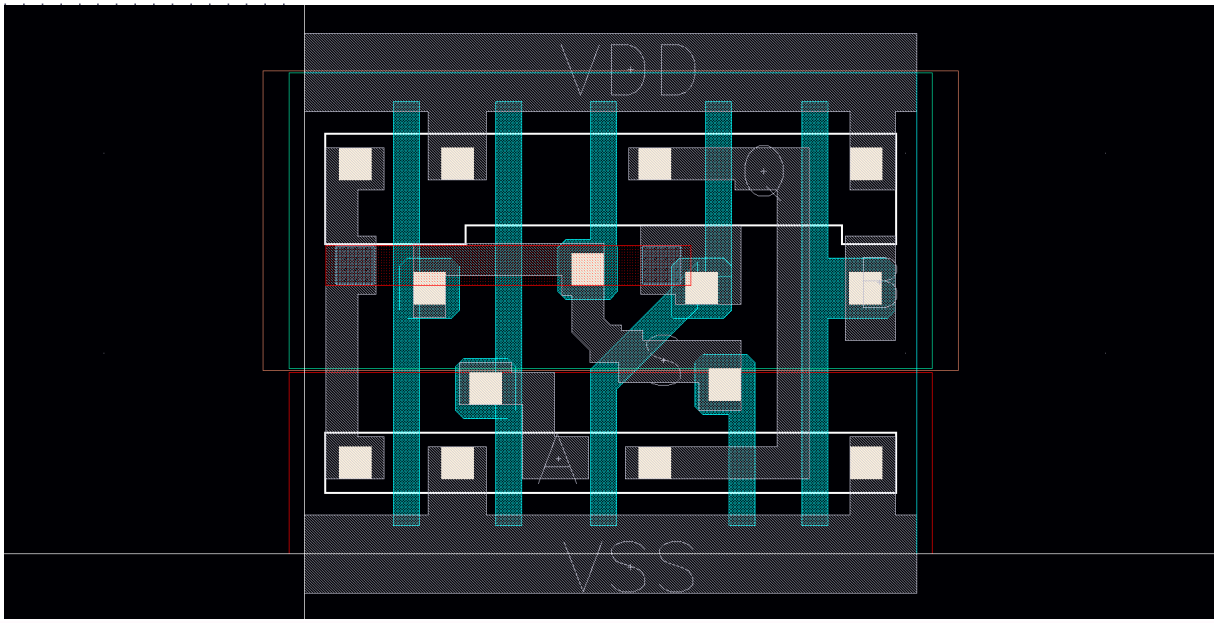
	Cell name	*description*	*status*	*layout size [µm x µm]*
1.	AND21X1	2-input AND	DRC, LVS, QRC	2.04 x 2.4 = 4.896
2.	AOI21X1	AND-OR-INVERT with 2 input AND	DRC, LVS, QRC	2.04 x 2.4 = 4.896
3.	BUFX1	Buffer	DRC, LVS, QRC	1.53 x 2.4 = 3.672
4.	DFFSBRBX1	D-flop with async set active low and reset active low; set has higher priority	DRC, LVS, QRC	10.2 x 2.4 = 24.48
5.	DFFSBX1	D-flop with async set active low	DRC, LVS, QRC	8.16 x 2.4 = 19.584
6.	DFFSX1	D-flop with async set active high	DRC, LVS, QRC	8.16 x 2.4 = 19.584
7.	DFFRX1	D-flop with async reset active high	DRC, LVS, QRC	8.16 x 2.4 = 19.584
8.	DFFRBX1	D-flop with async reset active low	DRC, LVS, QRC	8.16 x 2.4 = 19.584
9.	DFFX1	D-flop	DRC, LVS, QRC	6.63 x 2.4 = 15.912
10.	DLATCHX1	Transparent latch	DRC, LVS, QRC	3.57 x 2.4 = 8.568
11.	IMUX21X1	Inverting 2-input multiplexer	DRC, LVS, QRC	3.06 x 2.4 = 7.344
12.	INV1X1	Inverter	DRC, LVS, QRC	**1.02 x 2.4 = 2.448**
13.	INV1X2	Inverter 2x drive	DRC, LVS, QRC	1.53 x 2.4 = 3.672
14.	INV1X4	Inverter 4x drive	DRC, LVS, QRC	2.55 x 2.4 = 6.12
15.	MUX21X1	2-input multiplexer	DRC, LVS, QRC	3.57 x 2.4 = 8.568
16.	NAND21X1	2-input NAND	DRC, LVS, QRC	1.53 x 2.4 = 3.672
17.	NOR21X1	2-input NOR	DRC, LVS, QRC	1.53 x 2.4 = 3.672
18.	OAI21X1	OR-AND-INVERT with 2 input OR	DRC, LVS, QRC	2.04 x 2.4 = 4.896
19.	OR21X1	2-input OR	DRC, LVS, QRC	2.04 x 2.4 = 4.896
20.	TAP	Substrate and well contact	DRC	1.02 x 2.4 = 2.448

Cell - example

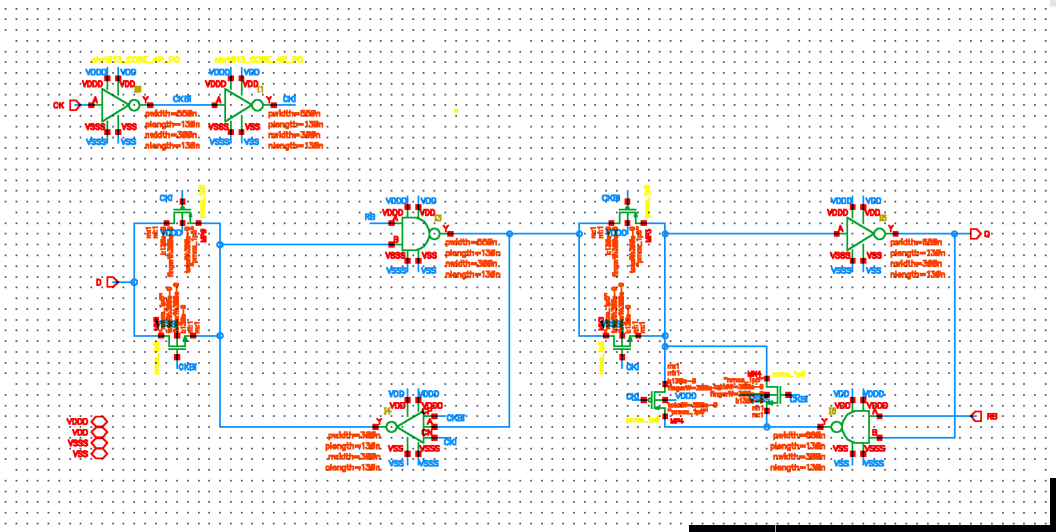


IMUX21X1

3,06 µm x 2,4 µm

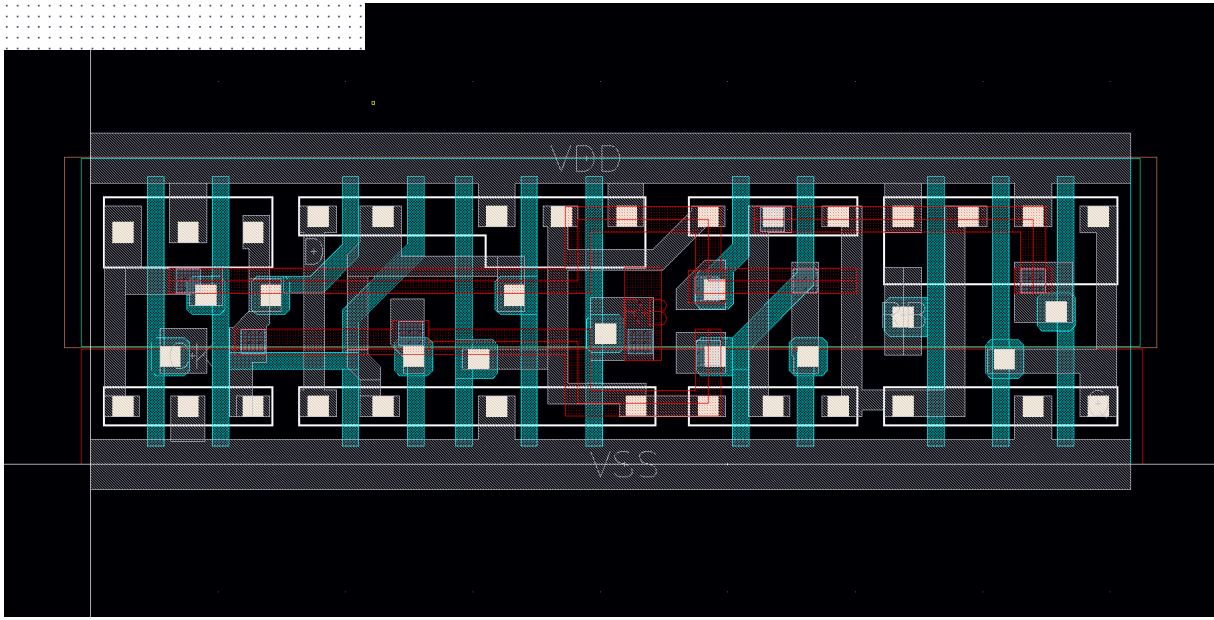


Cell - example

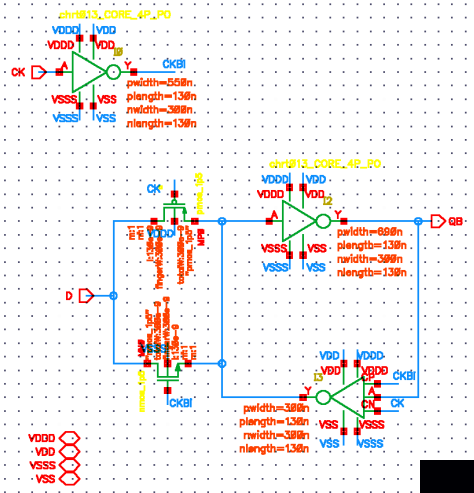


DFFRBX1

8,16 µm x 2,4 µm

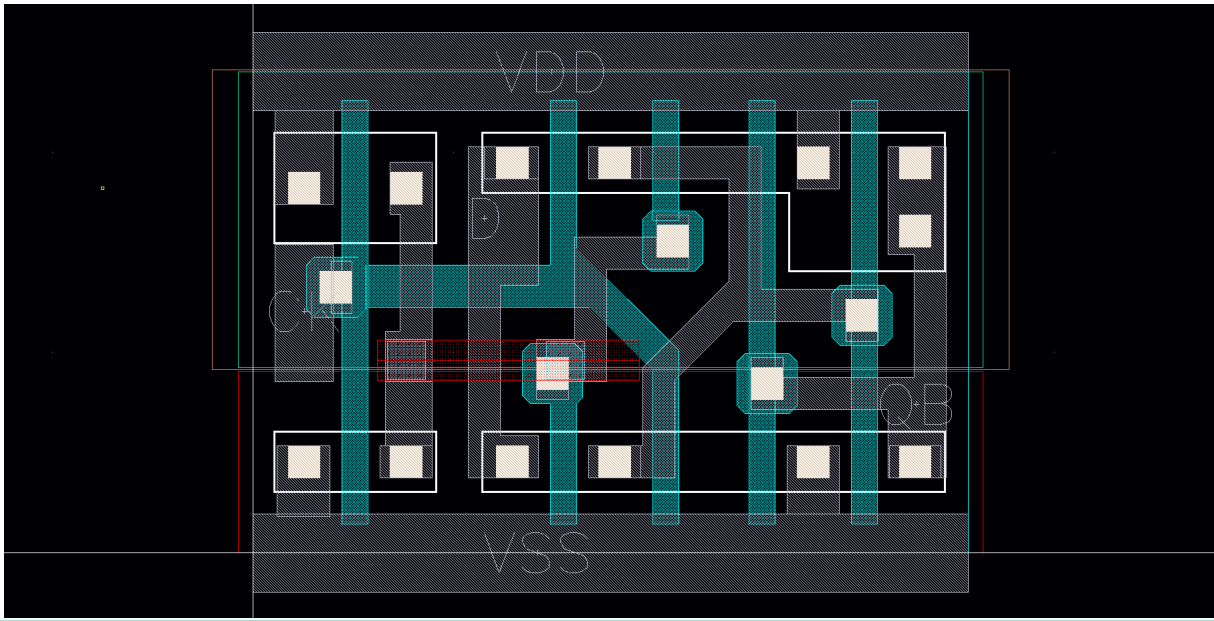


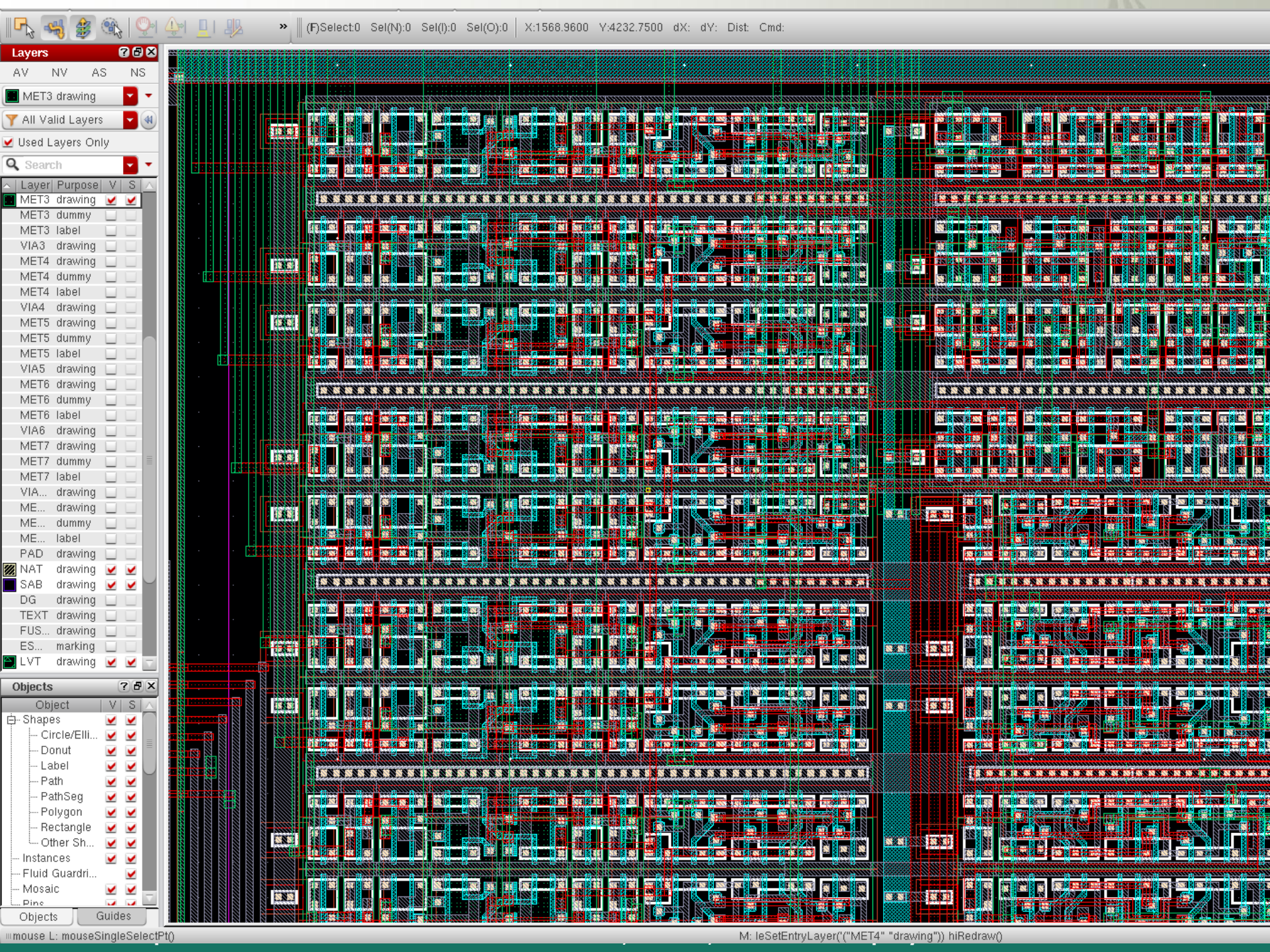
Cell - example



DLATCHX1

3,57 µm x 2,4 µm




(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X:1568.9600 Y:4232.7500 dX: dY: Dist: Cmd:
Layers
AV NV AS NS
MET3 drawing
All Valid Layers
Used Layers Only
Search
Layer Purpose V S
MET3 drawing
MET3 dummy
MET3 label
VIA3 drawing
MET4 drawing
MET4 dummy
MET4 label
VIA4 drawing
MET5 drawing
MET5 dummy
MET5 label
VIA5 drawing
MET6 drawing
MET6 dummy
MET6 label
VIA6 drawing
MET7 drawing
MET7 dummy
MET7 label
VIA... drawing
ME... drawing
ME... dummy
ME... label
PAD drawing
NAT drawing
SAB drawing
DG drawing
TEXT drawing
FUS... drawing
ES... marking
LVT drawing
Objects
Object V S
Shapes
Circle/Elli...
Donut
Label
Path
PathSeg
Polygon
Rectangle
Other Sh...
Instances
Fluid Guardri...
Mosaic
Pins
Objects
Guides
mouse L: mouseSingleSelectPt()
M: leSetEntryLayer('("MET4" "drawing")) hiRedraw()

Current status

	Task	Status
1	Layout pre-study (define row height, metal pitch/offset, etc.)	Done
2	dfII technology file modifications	90%
3	Abstract generator configuration	90%
4	Cell schematics	100%
5	Cell layouts	100%
6	Verilog models	90%
7	Verilog models verification (vs analog simulations)	5%
8	Timing characterization setup (ETS 10.11)	Generated for ss, tt, ff corners and VDD=1.2, VDD=1.5
9	Synthesis tests	50%
10	Technology LEF files	20%
11	Place & route tests	0%
12	Import to Virtuoso tests	0%
13	Post-route DRC/LVS	0%
14	Post-layout verilog simulations	0%
15	Mixed-mode simulations	50%