AIDA

Common work on 65nm CMOS technology: proposal for IP blocks from WP3 groups

Bonn (from February EVO meeting)

- LVDS/SLVS pads
- PLL
- Gigabit driver

INFN

- Discriminator
- Charge injection circuits for Front-End calibration
- n-bit D/A Converter (current steering topology)
- I/O PADs (LVDS to CMOS, CMOS to LVDS)

+ Technology characterization

CNRS (LAL, LAPP, LPNHE)

- Bandgap
- OTA
- Preamp (pixels LAPP)

- DAC (LAL)
- ADC (LAL,[LPSC], LAPP)

- Service serial link (LPNHE)
- SPI serial interface
- I2C (IPNL/LAPP)
- JTAG controller (LAPP)
- I/O cells
- PLLs (TOT, pixels, LAL, LAPP)

CNRS (CPPM) (from February EVO meeting)

- Monitoring ADC
- Temperature sensor
- Generic amplifier

AGH

- LVDS/SLVS pads
- PLL