AGH UNIVERSITY OF SCIENCE AND TECHNOLOGY

AIDA WP3
AGH-UST plans for IP blocks

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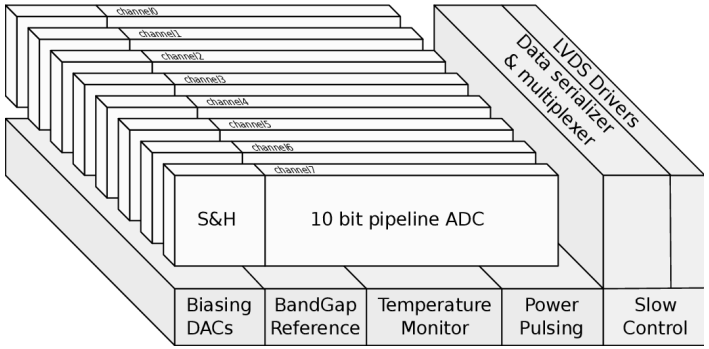
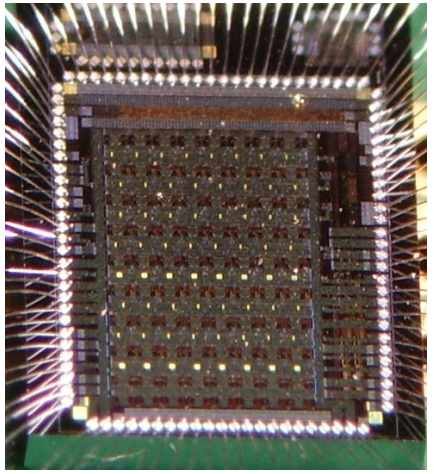
Blocks for multichannel digitizer system

Multichannel digitizer comprising 8 channel ADC plus peripherals was developed in AMS 0.35um. The idea is to develop similar blocks in 130/65 nm for faster system, with lower power consumption. Presently works are done in IBM130nm. Possible development within AIDA also in 65nm.



8 channels of 10 bit ADC
Digital multiplexer/serializer:
- Serial mode and parallel output mode
High speed LVDS drivers&receivers (<=1GHz)
Various DACs for analog controls
Precise BandGap reference source
Temperature sensor
Power pulsing



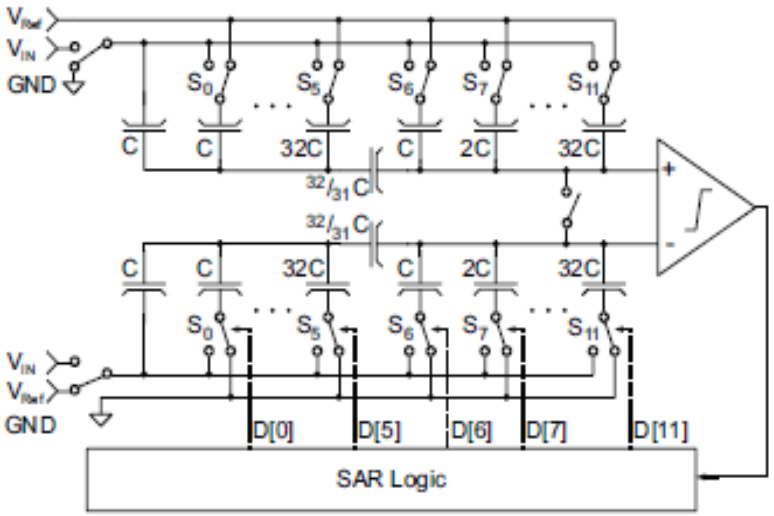
M. Idzik, K. Swientek, T. Fiutowski, Sz. Kulis, D. Przyborowski "A 10-bit multichannel digitizer ASIC for detectors in particle physics experiments", IEEE Trans. Nucl. Sci. 2012, in print

Developments in IBM 130nm

- Designed and submitted (February 2012) prototypes
  - 10-bit scalable Frequency&Power SAR ADC
  - Scalable Frequency&Power PLL
  - SLVS I/O
- Design in progress...
  - 6-bit scalable Frequency&Power SAR ADC
  - Extended version of scalable Frequency&Power PLL
- Design of other blocks (Bandgap, temperature sensor, DACs, …) possible but not yet decided...

All works done by now have been supported with non-AIDA resources.

Design of SAR ADC in IBM 130nm



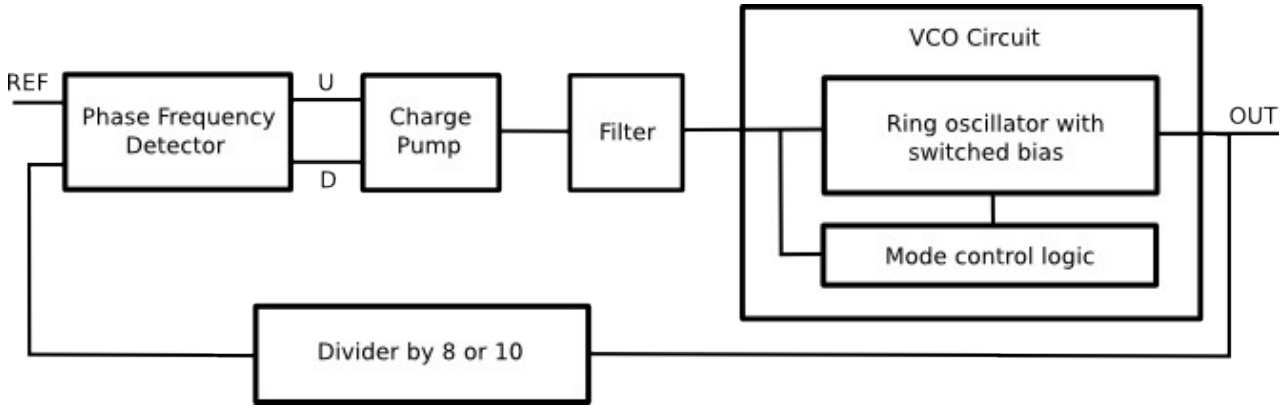
Prototype 10-bit ADC submitted in February 2012

- Architecture: SAR ADC with segmented DAC
- Scalable frequency (up to ~50 MS/s) and power consumption
- 1-2mW at 40MS/s
- ~150um pitch

Design of 6-bit ADC (for tracking)

- Architecture: SAR ADC with segmented DAC
- Scalable frequency (up to ~100 MS/s) and power consumption
- <0.5 mW at 40MS/s
- ~40um pitch

Design of PLL for data serialization in IBM 130nm



Prototype submitted in February 2012

- Architecture: type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO freq. range
- VCO frequency range 60MHz – 520MHz,
- VCO frequency division by 8 or 10
- Power consumption <0.5mW at 500MHz
- Area 200um x 160um
- Simulated jitter RMS<5ps

PLL design in progress

- Architecture: type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO freq. range
- VCO frequency range 8MHz – 3GHz,
- VCO frequency division by 6, 8, 10 or 16
- Power consumption <2mW at 3GHz
- Jitter RMS<5ps

Summary and plans

- In 2012 we have submitted and will submit various blocks designed in IBM 130nm (ADCs, PLLs, SLVS, and possibly other...). These works are supported from non AIDA resources. Maybe some of these designs could be used also for AIDA WP3...?
- We are interested in the design of some of the mentioned blocks, in 65nm CMOS. We can start work in 65nm at the end of 2012.

Thank you for your attention