



# AIDA 1st ANNUAL MEETING

## Wednesday 28 March 2012

### WP3 Microelectronics - Sem 5 (14:00 - 16:10)

time	[id] title	presenter
14:00	[62] Introduction	MOSER, Hans-Günther RE, Valerio
14:20	[63] Bonn/CPPM plans for 3D integration	BARBERO, Marlon Benoit
14:40	[64] INFN/IPHC plans for 3D integration	RATTI, Lodovico
15:00	[65] LAL plans for 3D integration	LOUNIS, Abdenour
15:20	[66] MPI plans for 3D integration	WEIGELL, Philipp
15:40	[69] Univ. Barcelona plans for WP3.2	DIEGUEZ, Angel
15:50	[67] Discussion	

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time	[id] title	presenter
14:00	[76] CERN TSV activities with CEA-LETI	DANNHEIM, Dominik
14:20	[68] Uppsala plans for WP3.2	BRENNER, Richard
14:30	[71] CNM plans for WP3.2	
14:50	[72] AGH-UST plans for IP blocks	IDZIK, Marek
15:05	[75] Design of an area-effective digital library for pixel readout chips	GRYBOS, Pawel SZCZYGIEL, Robert
15:25	[100] CNRS plans for IPs in 65nm	Mr GENAT, Jean-Francois
15:35	[73] IP blocks in SiGe	MARTIN-CHASSARD, Gisele
15:45	[74] Discussion	