Silicon Tracking and Vertexing at the Linear Colliders

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- *Basic features of the ILC and CLIC projects :*
  - prominent physics objectives
  - accelerator related running conditions
- *Experimental concepts under development :*
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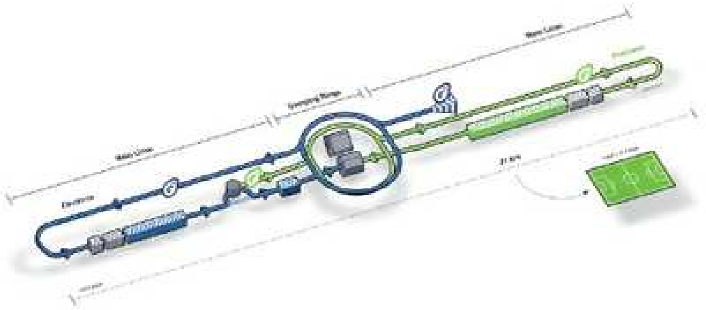
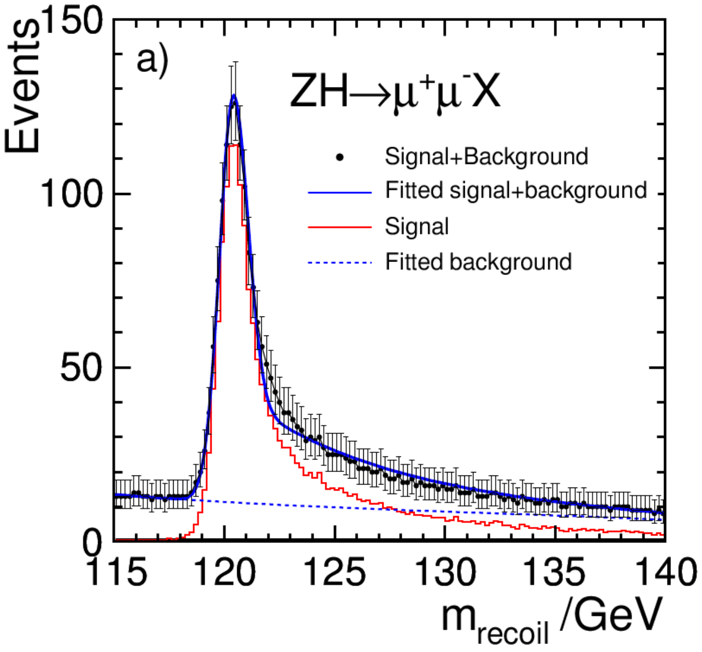
- *Tracking and Vertexing :*
  - Objectives, Sub-systems, Technologies, Limitations $\Rrightarrow$ R&D
- *Summary*

ILC & CLIC : Prominent Features



- **LC $\equiv$ next large scale accelerator after the start of LHC :**
  - ⋇ e^+e^- collisions **ILC** $\nearrow$
  - ⋇ 2 accelerator projects under way :
    - · ILC : collision energy up to 1 TeV $\rightarrowtail$ most advanced
    - · CLIC : collision energy up to 3 TeV $\rightarrowtail$ highest potential but most challenging



- **Scientific motivation :**
  - ⋇ investigate in detail the mechanism of EW Symmetry Breaking
  - ⋇ search for - and study - new physics at the highest energy scale

. . . elaborate on LHC results **. . .**

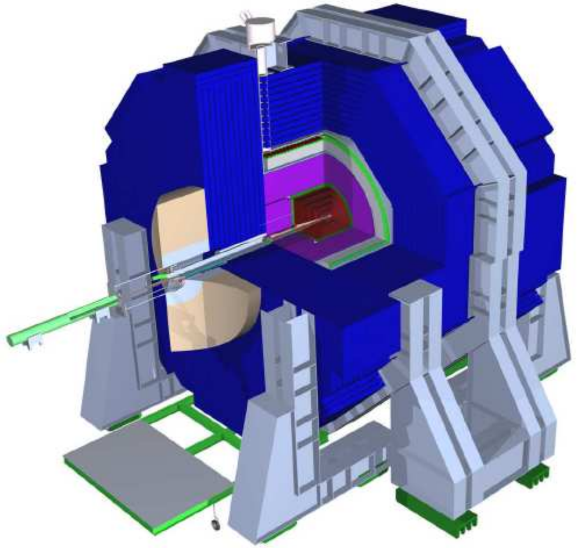
- **Highlights of the project :**
  - ⋇ **machine :** very well known beam parametres
  - ⋇ **experiment :** high precision (multi-jet) final state reconstruction capability over $\sim 4\pi$ solide angle

Experiments and their Strong Points

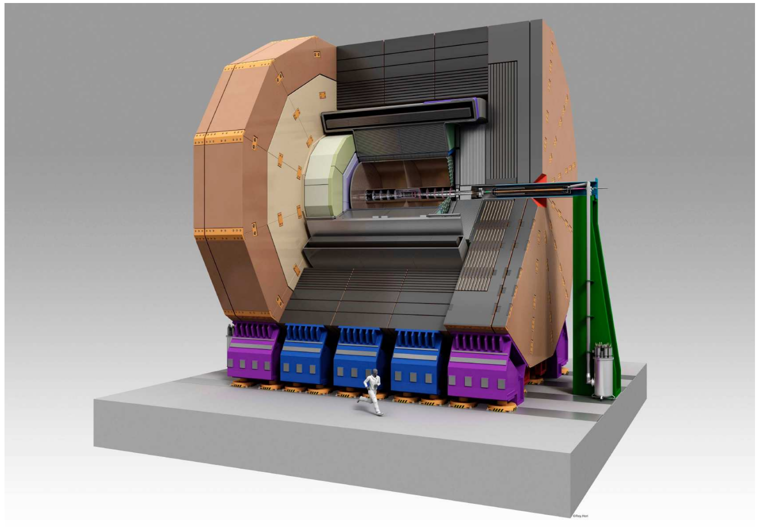
- **2 detector concepts proposed for ILC** *(L.o.l. in 2009)* **:**
  - SiD: entire tracking based on Si sensors
  - ILD: Central tracking provided by TPC

    Intermediate & End-cap trackers based on Si sensors
  - both concepts extended to CLIC running *(see CDR-2012)*

SiD ▷



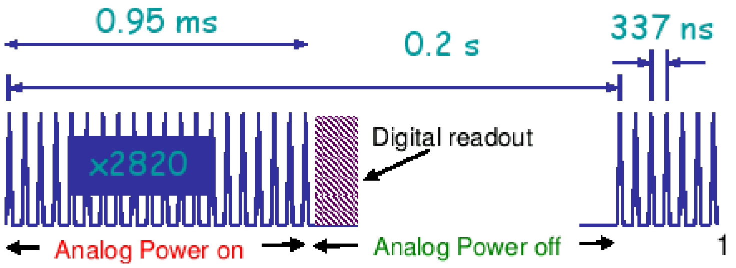
ILD ▷



- **Specific aspects exploiting ILC running conditions :**
  - very well known beam energy and polarisation
  - relatively moderate background ($<<$ at LHC)

    ⇛ detector design governed by **physics driven specifications**
  - beam time structure : 1 ms BX interspaced with 199 ms without beam

    ⇛ **switch off apparatus** inbetween bunch trains to **save power**

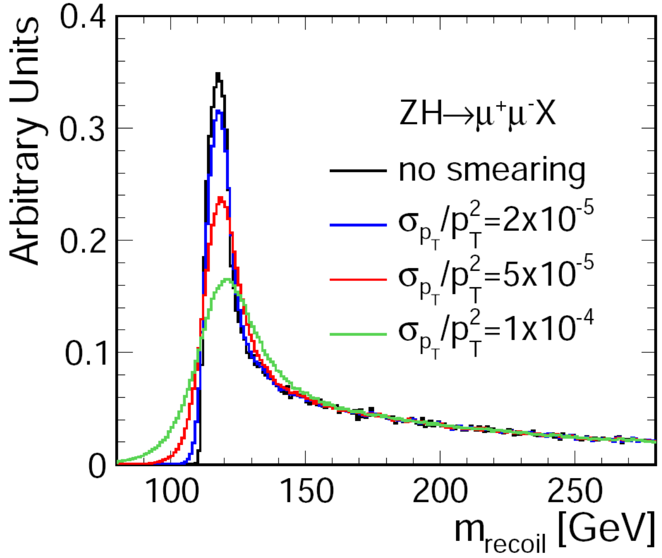


- **CLIC : 156 ns long bunch trains separated by 20 ms**

  ⇛ some sub-systems (e.g. vertex detector) feature more severe specifications (see slide Nr.8)

Tracking and Vertexing Performance Goals

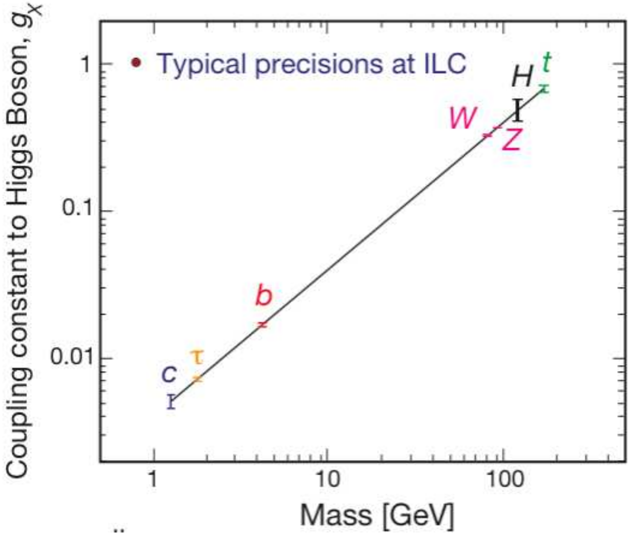
- **Tracking:**
  - ⋇ reconstruct all charged tracks down to p $<<$ 1 GeV/c, including kincks
    - $\Rrightarrow$ hermiticity, precision, low material budget (multiple scatt., second. interactions)
    - $\hookrightarrow$ ILD/SiD: $\sigma_{1/p_t} \simeq$ 2/5×10^{-5}GeV^{-1}
  - ⋇ allow precise extrapolation to calorimetres for $e^{\pm}\gamma$ separation
    and for identifying "all" showers generated by neutral particles (PFA)

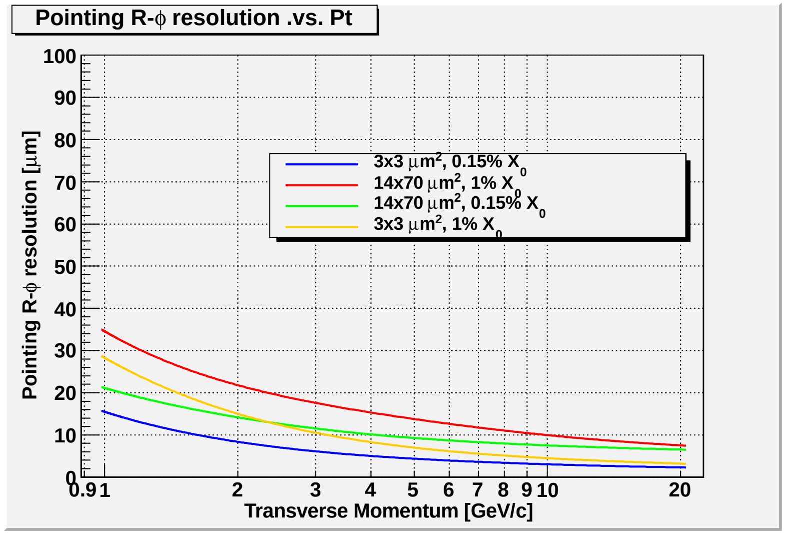


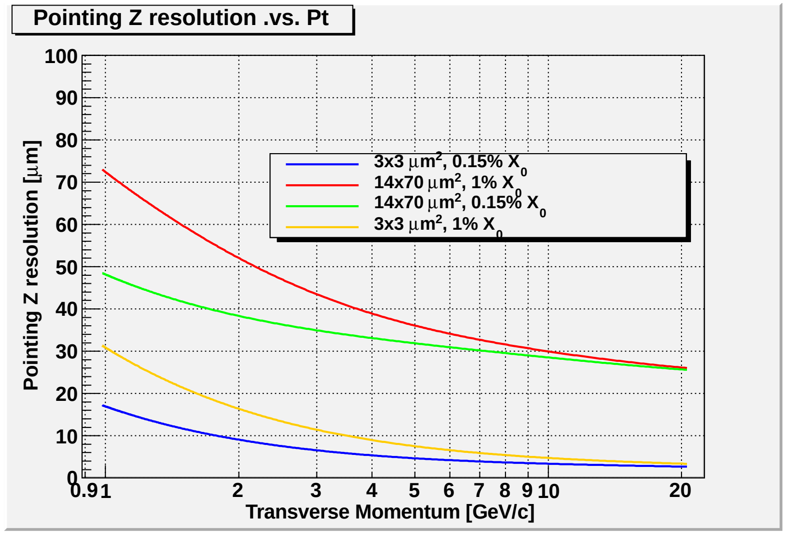
- **Vertexing:**
  - ⋇ achieve high efficiency and purity flavour tagging (charm & tau !!!)

$\hookrightarrow \sigma_{R\phi,Z} \leq 5 \oplus 10/p \cdot sin^{3/2}\theta \;\; \mu m$ ▷ LHC: $\sigma_{R\phi} \simeq 12 \oplus 70/p \cdot sin^{3/2}\theta$

▷ Comparison: $\sigma_{R\phi,Z}$(ILD) with VTX made of ATLAS-IBL or ILD-VTX pixels:



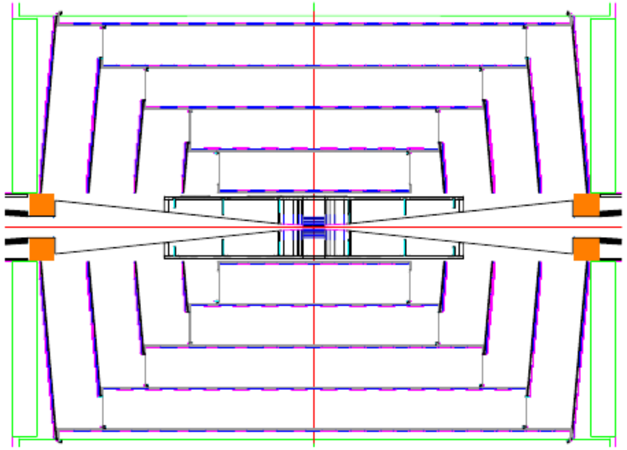


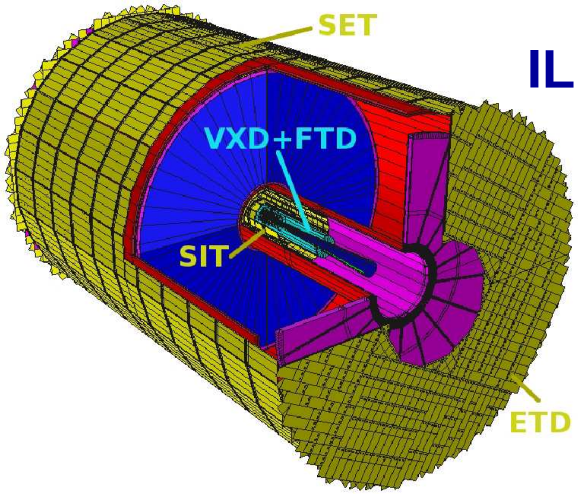


Tracking Devices

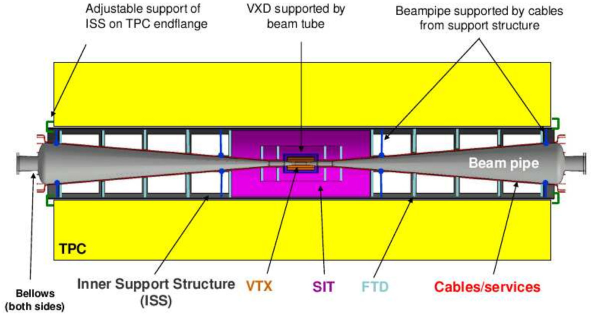
- **Main characteristics:**
  - ⋇ **SiD :** Main tracker $\equiv$ 5 layers (25+2$\times$10 m^2) of Si μstrips
    $\Rrightarrow$ **5** points/track
    - 3 layers at shallow angle in each end-cap
  - ⋇ **ILD :** Main tracker $\equiv$ TPC $\Rrightarrow$ **224** points/track
    - SET (25m^2) & ETD (2$\times$10m^2) around TPC
    - SIT (2 layers, 3 m^2) bridging TPC with VTX
    - 7 layers in each end-cap
    - $\lesssim$ 0.65% X_0/layer – $\sigma_{R\phi/Z}$ = 7/50μm^2
- **R&D topics:**
  - ⋇ μstrip sensors : edgeless $\rightarrowtail$ 3D planar
    $\triangleright$ thinner, lower voltage, larger wafers, ...
  - ⋇ pixel sensors : thickness, large area, cost, power, ...
  - ⋇ integration needs: $\multimap$ low-power, on-sensor connectable, **read-out ASICs**
    $\multimap$ light, heat conducting & rigid **supports** - very light **cooling system**
  - ⋇ **power** distribution and **pulsing** over **large surfaces** in **high magnetic field** $\triangleright$ mechanical stability

SiD: B=4 T





ILD: B=3.5 T

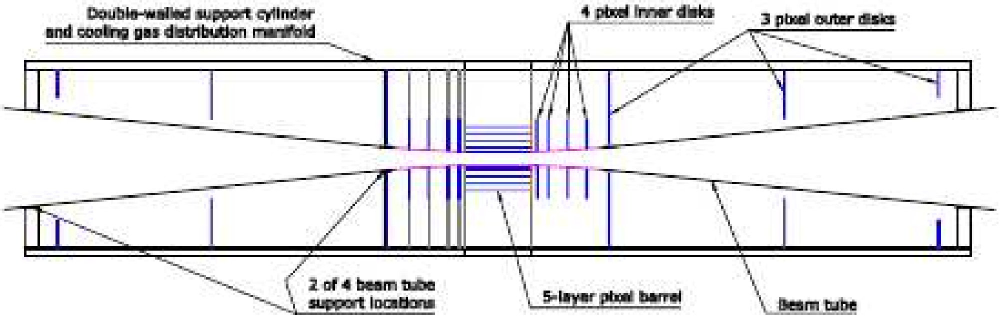


ILC Vertexing Devices

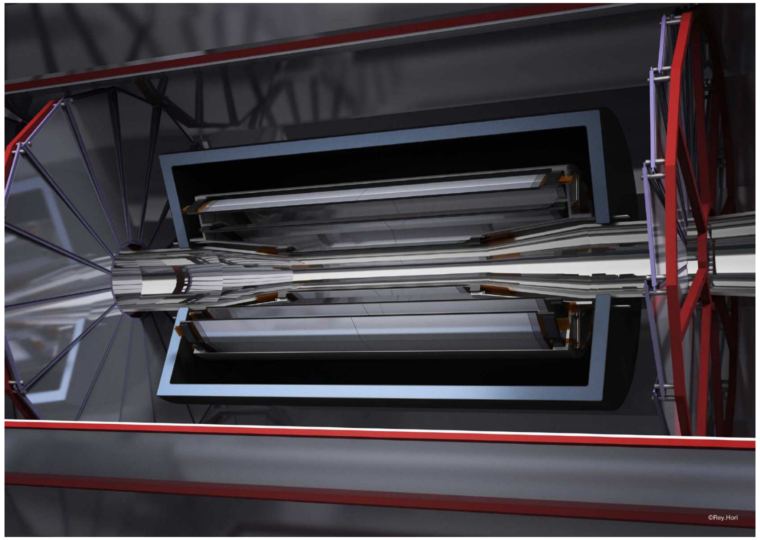
- **Main characteristics:**
  - ⋇ SiD : short barrel complemented by end-cap disks
  - ⋇ ILD : long barrel geometry
  - ⋇ Layers : 2 options (R $\simeq$ 15 to 60 mm)
    - 5 single-sided layers : $\lesssim$ 0.2% X_0/layer
    - 3 double-sided layers : $\lesssim$ 0.3% X_0/layer
    - $\sigma_{R\phi,Z} \lesssim 3\ \mu m$
  - ⋇ 2 read-out alternatives : during trains or inbetween trains
    - during 1 ms trains $\Rrightarrow$ fast read-out against occupancy
      - ILD : 10-50 μs
      - SiD : 0(1) $\mu s \rightarrowtail$ standalone tracking

- **Issues:**
  - ⋇ High precision, thin and low power pixel sensors adapted to relatively high beam related background
  - ⋇ Material budget keeping multiple scattering at an affordable level compatible with required sensor cooling

SiD

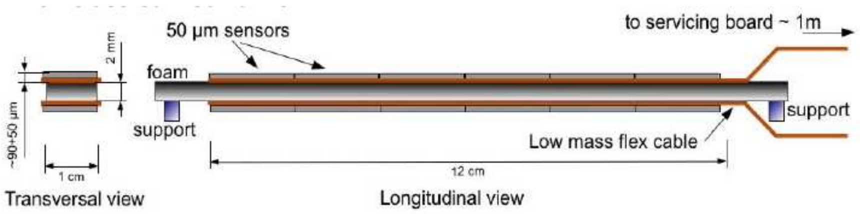


ILD



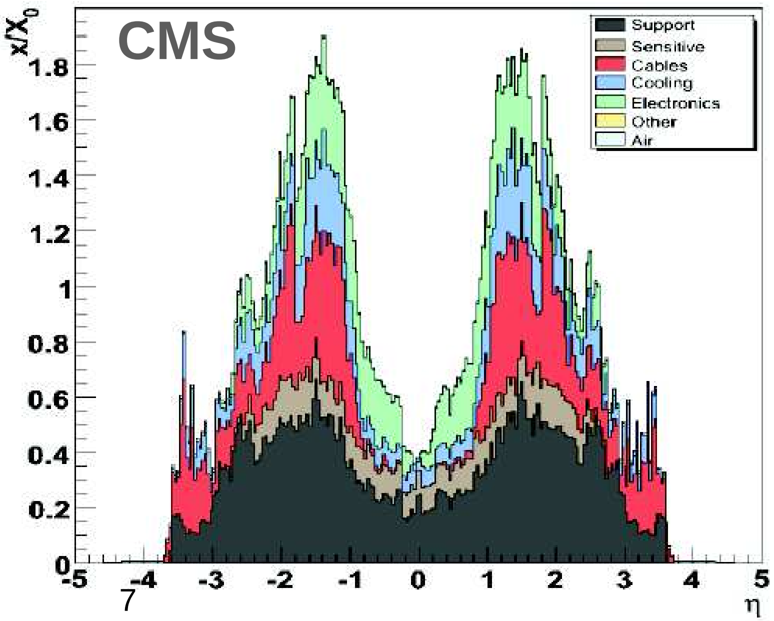
ILC Vertexing Devices: Major R&D Issues

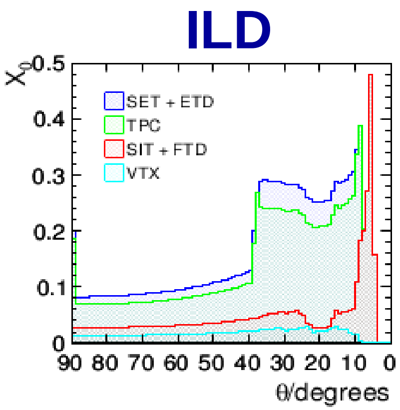
- Pixel technology
  - Trade-off between precision (small pixels) and read-out speed
  - Several technologies considered :
    - continuous read-out : CMOS sensors (various types), DEPFETs
    - delayed read-out : FPCCD, ISIS (?), ...
  - Major R&D issues:
    - cope with beam-related background in innermost layer ⇛ read-out speed
    - power consumption ⟶ avoid active cooling (material budget ↘)



- Integration issues
  - **material budget :** ⟶
    - **flex cable**
    - **mechanical support**
  - **power** distribution and **pulsing** over **large surfaces**

    in high magnetic field ▷ mechanical stability
  - **micro-channel cooling** would be very helpful ....

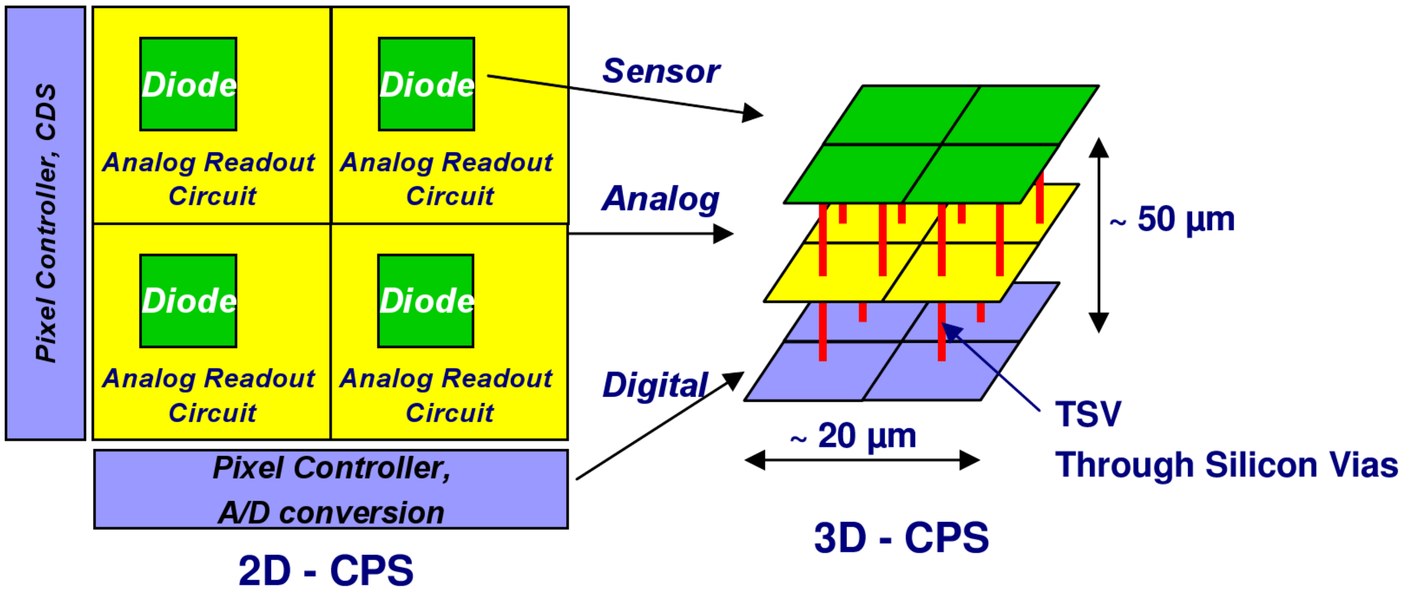




CLIC Motivated R&D Goals

- **Prominent changes w.r.t. ILC :**
  - Beam time structure : 156 ns long trains of 312 bunches (0.5 ns spacing)
  - Background increase : beamstrahlung & $\gamma\gamma$ collisions
    - $\hookrightarrow$ impacts nominally vertex detector inner layers (occupancy)
  - Continuous read-out mandatory : $t_{int} < 10$ ns imposed (keeping 3 μm resolution)
    - $\hookrightarrow$ present technologies far from this set of performances

- **Major R&D issues :**
  - Investigate 3D Integrated technologies
    - $\hookrightarrow$ Through Silicon Vias (TSV)
  - Allows combining thin tiers dedicated to specific & complementary functionalities: charge sensing, analog r.o., digital proc., ...
  - Allows integrating high density signal processing μcircuits in small pixels !



- **Development started in 2009 from various sensing technologies (hybrid, CMOS, ...)**
  - facing interconnectivity difficulties
  - BUT technology has very high potential for Position Sensitive Detectors $\Rrightarrow$ broad interest

SUMMARY

- ILC/CLIC: world wide project driving multi-directional R&D on Si based Position Sensitive Detectors

- 2 major experimental concepts :
  - ⁕ **SiD** (only Si tracking) and **ILD** (combining Si detectors with TPC)
  - ⁕ both feature $\sim$ 50 m^2 Si μstrips and $\gtrsim$ 1/2 m^2 Si pixels

- State-of-the-art not yet complying with specifications $\Rrightarrow$ intensive R&D :
  - ⁕ **μstrips :** edgeless, thinner, ... (goals as for LHC upgrades)
  - ⁕ **Pixel sensors :** 2D sensors with thin, fully depleted, sensitive volume hosting integrated FEE

    $\hookrightarrow$ 3D $\equiv$ multi-tier sensors with pixel-level interconnections (10-20μm pitch TSV)

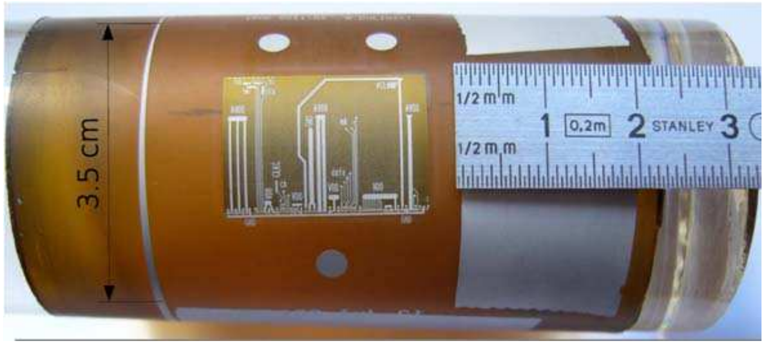
    And : stitching, redistribution layer, ...
  - ⁕ **Flex cable & connectivity :** high density traces, very thin kapton, redistribution layer, wireless connectivity
  - ⁕ **Mechanical supports :** very light and rigid, heat conducting, alignment monitoring, ...
  - ⁕ **Cooling :** μchannels, new heat conducting materials, ...

- Many activities would win from exchanges with industry $\rightarrowtail$ spin-offs (?)

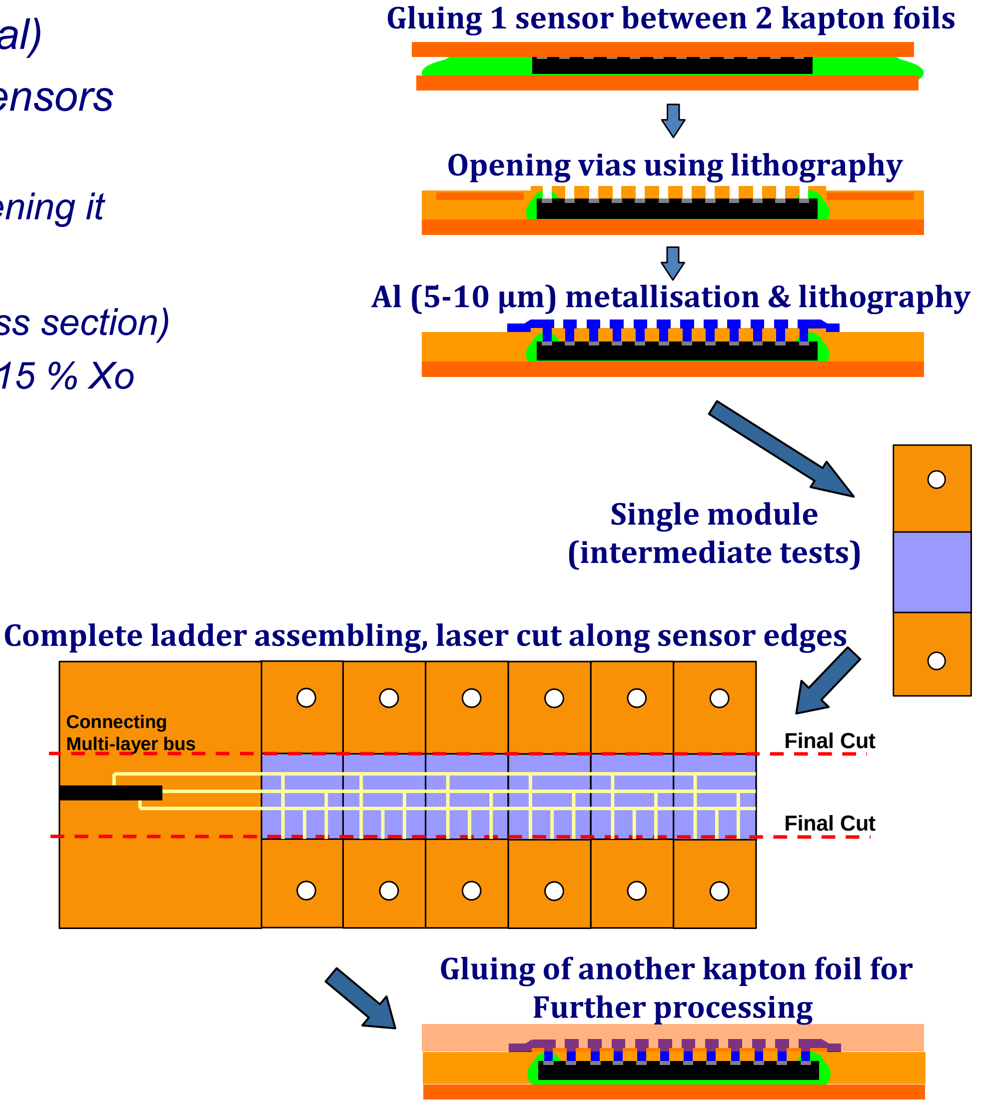
Sensor Embedding

SEnsor Row Neatly Wrapped In Extra-Thin Envelope ➔ SERNWIETE

- *Rationale*
  - *Get rid of the wire bonds (less material)*
  - *Provide a mechanical protection to sensors*
    - *allows thinner sensors*
    - *Allows more mechanical stress by evening it*
  - *Possibilities*
    - *Lower material budget (average ~ cross section)*
      - ☐ *Expected material budget <~ 0.15 % Xo*
    - *Support less*
    - *cover non planar surface*



Idea from R. De Oliveira, W.Dulinski



Gluing 1 sensor between 2 kapton foils

Opening vias using lithography

Al (5-10 µm) metallisation & lithography

Single module (intermediate tests)

Complete ladder assembling, laser cut along sensor edges

Gluing of another kapton foil for Further processing