ALICE SILICON TRACKER UPGRADE

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for the ALICE Collaboration

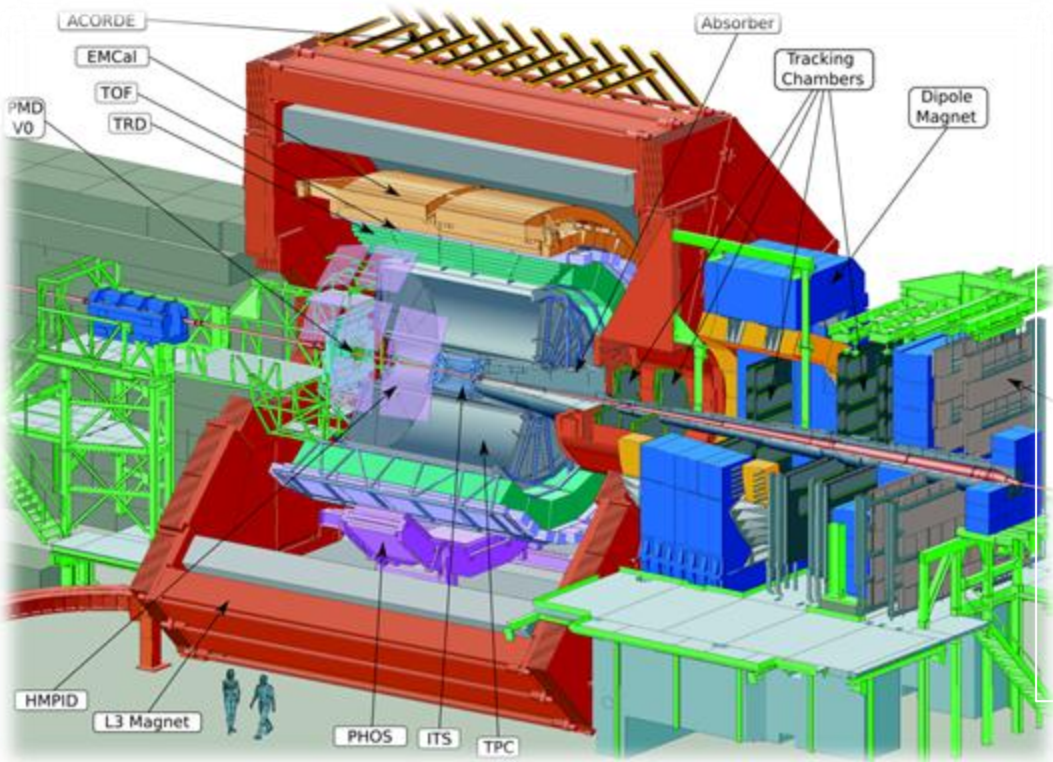
Summary

- The present ALICE Inner Tracking System
- ALICE Silicon Tracker Upgrade motivations
- Detector requirements
- Technology implementation
  - Hybrid Pixel Detectors
  - Monolithic Pixel Detectors
  - Strip Detectors
- Conclusions

The ALICE experiment

Dedicated heavy ion experiment at LHC

- Pb-Pb collisions: Study of the behavior of strongly interacting matter under extreme conditions of energy density and temperature
- Proton-proton collisions: Reference for heavy-ion program and strong interaction measurements complementary to other LHC experiments



Barrel Tracking requirements

- Pseudo-rapidity coverage $|\eta| < 0.9$
- Robust tracking for heavy ion environment
  - Mainly 3D hits and up to 150 points along the tracks
- Wide transverse momentum range (100 MeV/c – 100 GeV/c)
  - Low material budget (13% X_0 for ITS+TPC)
  - Large lever arm to guarantee good tracking resolution at high p_t

PID over a wide momentum range

- Combined PID based on several techniques: dE/dx, TOF, transition and Cherenkov radiation

The present Inner Tracking System

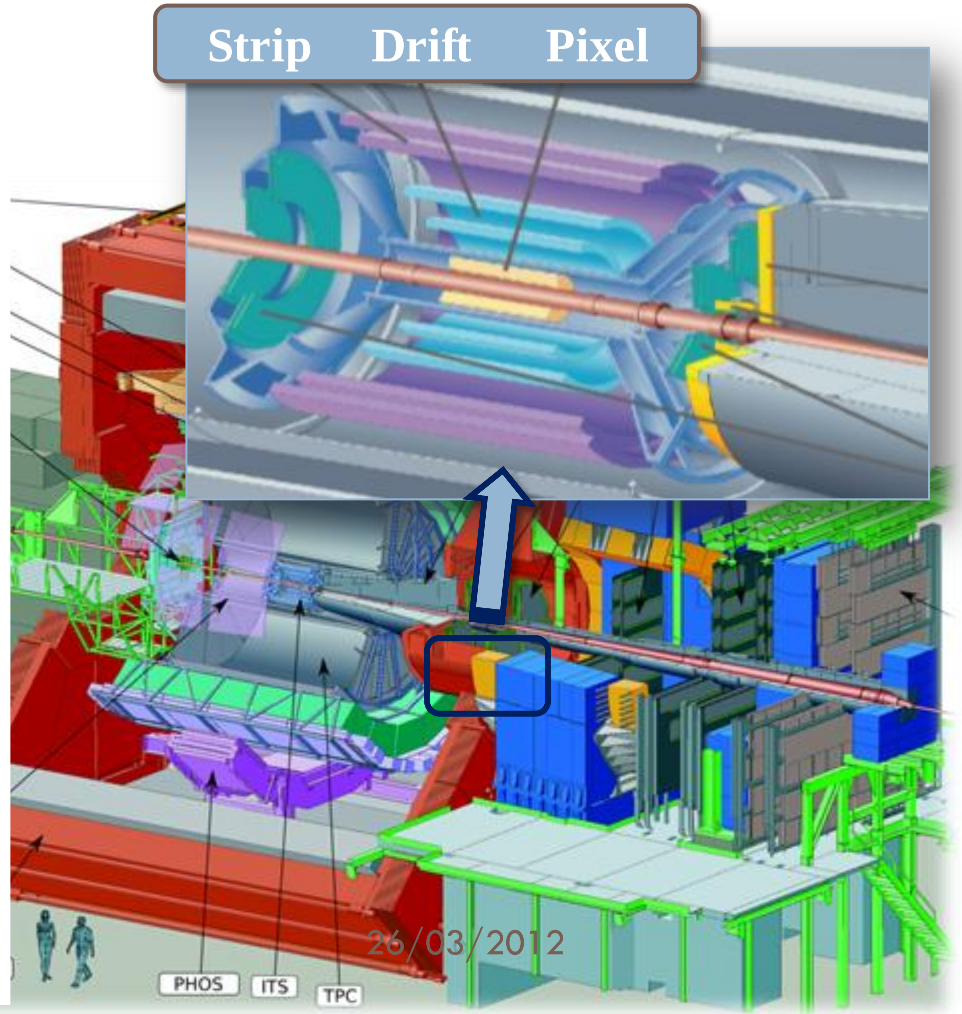
ITS: 3 different silicon detector technologies

The ITS tasks in ALICE

- **Secondary vertex** reconstruction (c, b decays)
  - Good track impact parameter resolution $< 60\ \mu m$ ($r\varphi$) for $p_t > 1$ GeV/c in Pb
- Improve primary vertex reconstruction, momentum and angle resolution of tracks
- **Tracking and PID of low p_t** particles
- Prompt **L0 trigger** capability <800 ns (Pixel)

Detector characteristics

- Capability to handle high particle density
- Good spatial precision (12–35 μm in $r\phi$)
- High granularity ($\approx$ few % occupancy)
- Small distance of innermost layer from beam axis (mean radius $\approx$ 3.9 cm)
- Limited material budget (7.2% X_0)
- Analogue information in 4 layers (Drift and Strip) for particle identification



Physics Motivations for the Upgrade

Motivations → Physics goals → Design goals

- Quark mass dependence of in-medium energy loss
- Thermalization of heavy quarks in the medium

- Improve the charmed baryonic sector studies
- Access the exclusive measurement of beauty hadrons

- Reconstruct displaced decay vertices
- Track charged particles with high resolution at all momenta
- Identify charged particles down to low transverse momentum
- Implement a topological trigger functionality

Benchmark analysis

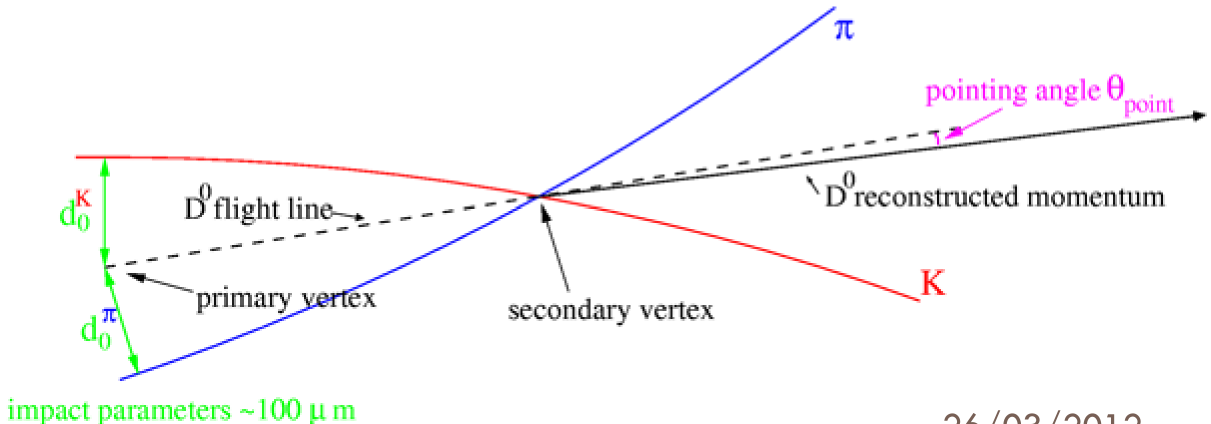
$D^0 \longrightarrow K^-\pi^+$

$\Lambda_c \longrightarrow pK^-\pi^+$

$B \longrightarrow D^0 (\longrightarrow K^-\pi^+)$

$B \longrightarrow J/\psi (\rightarrow e^+e^-)$

$B \longrightarrow e^+$



From Design Goals to Detector Requirements

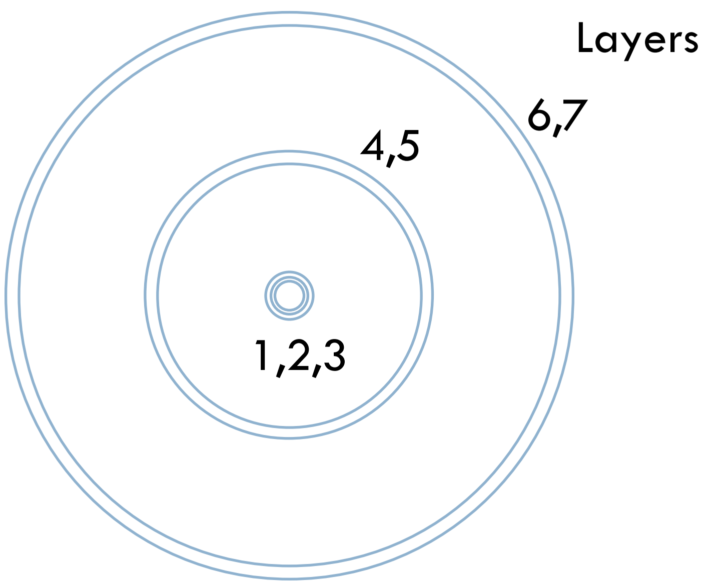
- **Impact parameter resolution improvement by a factor 3**
  - Distance from interaction vertex
  - Material budget
  - Spatial precision

  → *Geometry and technology for innermost layers*
- **Standalone tracking efficiency and transverse momentum resolution**
  - Granularity → *Pixel cell size reduction for inner layers*; *Strip cell size reduction for intermediate radii*
  - Radial extension → *Position of the outermost layers*
  - Layer grouping
- **Experimental environment: 685 krad, 80 part/cm^2**
  - Radiation hardness, granularity → *Technology for innermost layers*
- **Interaction rates: 50 kHz in Pb-Pb, 2 MHz in pp**
  - Fast readout → *Readout architecture*
- **Particle identification capability**
  - Energy loss measurement resolution and range → *dE/dx, ToT techniques*
- **Expected detector lifetime**
  - Detector accessibility and modularity → *Layout, supports, services*

ITS Upgrade geometry

- **Beam pipe** outer radius reduced to 19.8 mm, wall thickness to 0.5 mm
- **First detection layer** close to the beam pipe: r_1 =22 mm
- Increase **radial extension** 22-430 mm
  - Increasing the outermost radius to 500 mm results in a 10% improvement in transverse momentum resolution
- Layers are **grouped:** (1,2,3) (4,5) (6,7)
- η **coverage:** ±1.22 over 90% of luminous region → *z* dimension

Layer	Radius [cm]	+/- z
1	2.2	11.2
2	2.8	12.1
3	3.6	13.4
4	20	39.0
5	22	41.8
6	41	71.2
7	43	74.3



How Detector Requirements drive Technology Choices

Targets for Inner Layers (1, 2, 3)

- $r\phi$ & z spatial precision: 4 μm
  - Pixel size ($r\phi$, z): 20-30 , 20-50 μm
- Material budget per layer: 0.3-0.5% X_0
  - 0.1% X_0 under study for Layer 1
- Radiation env: 685 krad/ 10^{13} n_{eq} per year
- Granularity: 80 cm^{-2} particle density

→ **Monolithic pixel**
Hybrid pixel

Targets for Outer Layers (4, 5, 6, 7)

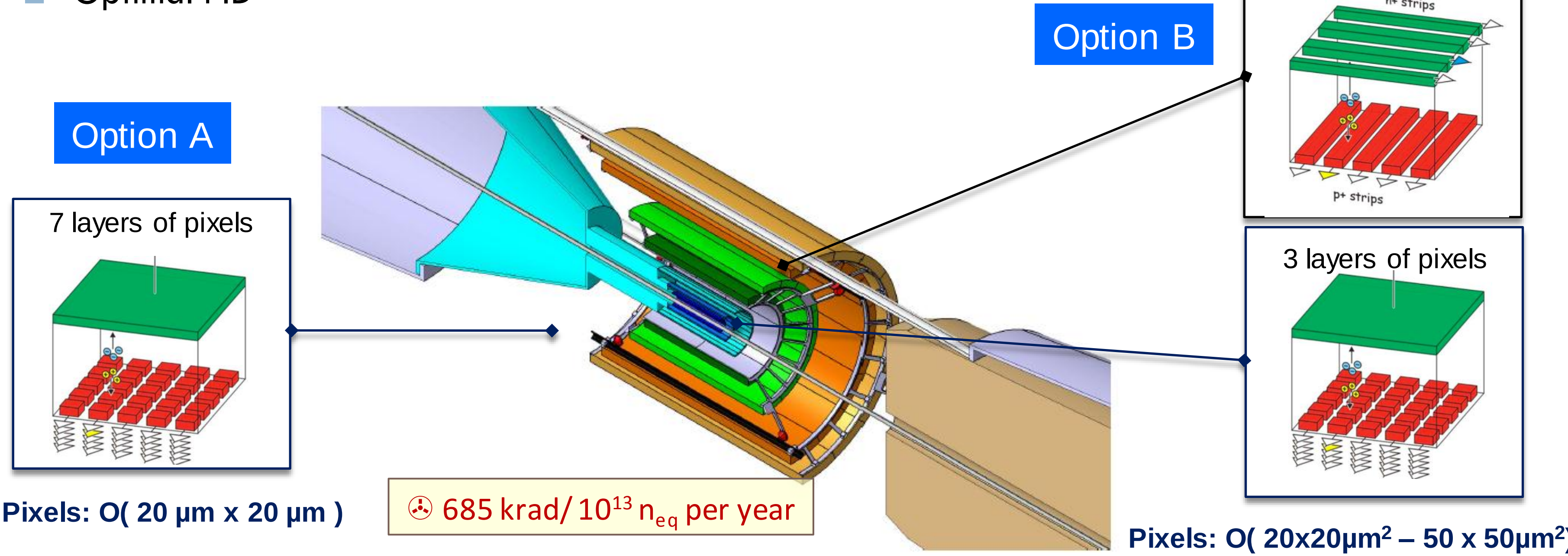
- $r\phi$ spatial precision: < 20 μm
  - Larger pixel size
  - Strip pitch 95 μm, stereo angle 35 mrad
- Material budget per layer: 0.5-0.8% X_0
- Radiation env: 10 krad/ $3*10^{11}$ n_{eq} per year
- Granularity: 1 cm^{-2} particle density
- Low cost per m^2

→ **Monolithic pixel**
Micro-strip

2 layout options

A. 7 layers of monolithic pixel detectors
- Better standalone tracking efficiency and transverse momentum resolution
- Worse PID or no PID

B. 3 innermost layers of hybrid pixel + 4 layers of micro strip detectors
- Worse standalone tracking efficiency and transverse momentum resolution
- Optimal PID



Pixels: O(20 μm x 20 μm)

Pixels: O($20 \times 20 \mu m^2$ – $50 \times 50 \mu m^2$)
Strips: 95 μm x 2 cm, double sided

Monolithic Pixel technology

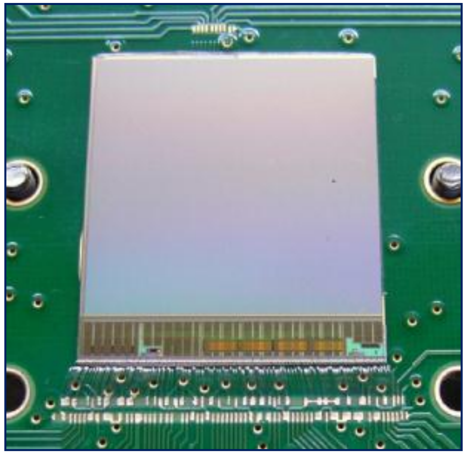
- Features:
  - Made significant progress, soon to be installed in STAR
  - All-in-one, detector-connection-readout
  - Sensing layer (moderate resistivity ~1 kΩcm epitaxial layer) included in the CMOS chip
  - Charge collection mostly by diffusion (MAPS), but some development based on charge collection by drift
  - Small pixel size: 20 μm x 20 μm target size
  - Small material budget: 0.3% X_0 per layer

- To be evaluated
  - Radiation tolerance

Options under study:
- MIMOSA
- INMAPS
- LePIX

Monolithic: MIMOSA (IPHC)

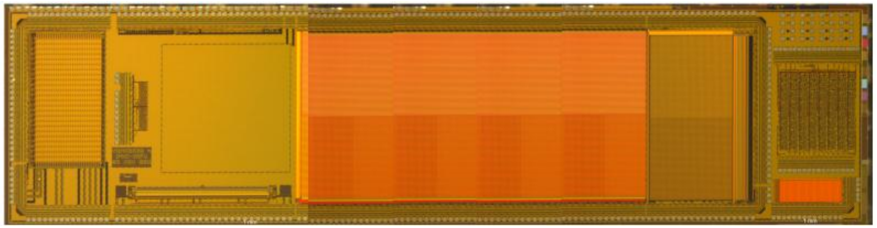
- CMOS sensors with rolling-shutter readout architecture
- MIMOSA series for STAR
  - Continuous charge collection (mostly by diffusion) inside the pixel
    - Charge collection time ~200 ns
  - Pixel matrix read periodically row by row: column parallel readout with end of column discriminators
    - Integration time ≡ readout period ~100 μs
    - Low power consumption (150-250 mW/cm^2): one row is powered at time
  - Pixel size 20 μm
  - Total material budget x ~ 0.3% X_0
  - 0.35 μm technology node



ULTIMATE sensor for STAR HFT

Monolithic: MIMOSA - 2

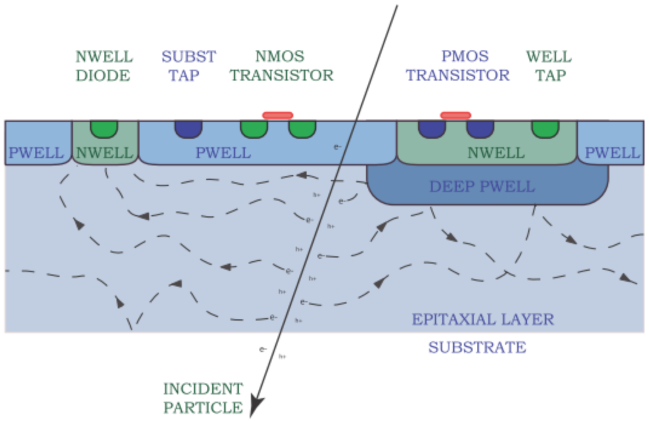
- MISTRAL development for ALICE
  - 0.18 μm technology node
    - Radiation tolerance improvement by factor 10x
  - Double-sided readout
    - Reduction of integration time down to 20-40 μs target
    - Double power consumption (more columns active at the same time)
      - Target power dissipation: < 250 mW / cm^2



- Submitted prototypes
  - MIMOSA32 (delivered), MonaliceT1 test chip.
    - Evaluation of the technology
      - detection efficiency, S/N, quadrupole-well
    - Test of radiation hardness, SEU sensitivity

Monolithics: INMAPS (RAL/Tower Jazz)

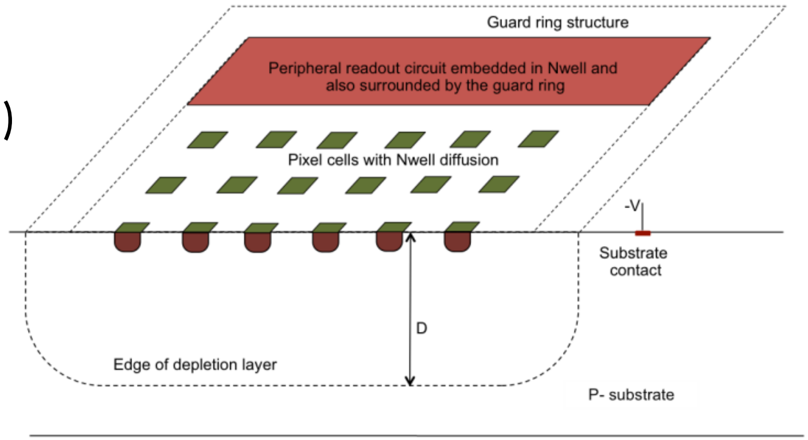
- In-pixel signal processing using an extension (deep p-well) of a triple-well 0.18 μm CMOS process developed by RAL with TowerJazz (technology owner)
  - Standard CMOS with additional deep p-well implant
  - 100% efficiency and CMOS electronics in the pixel
    - Size limitation: 30 μm x 30 μm in 0.18 μm
    - Power saving: matrix read only upon trigger request
      - further improvement with sparsified r.o.
  - Charge collection by diffusion
    - 18 μm detection thickness
    - 100 e^- minimum signal
    - good S/N with low sensor capacitance



- New development dedicated to ITS upgrade started in 2012 (Daresbury, RAL - ARACHNID Collaboration)
  - Verify radiation resistance for innermost layers
  - Reduce power consumption exploiting detector duty cycle (5% for 50 kHz int. rate)
  - Develop fast readout

Monolithics: LePIX

- Monolithic pixel detectors integrating readout and detecting elements with:
  - 90 nm CMOS technology
  - Moderate resistivity wafers
- Low power consumption (target < 30mW / cm^2)
- Large depletion region (tens of μm)
- Fast processing: full matrix readout at 40MHz
- Moderate bias voltage (< 100 V)



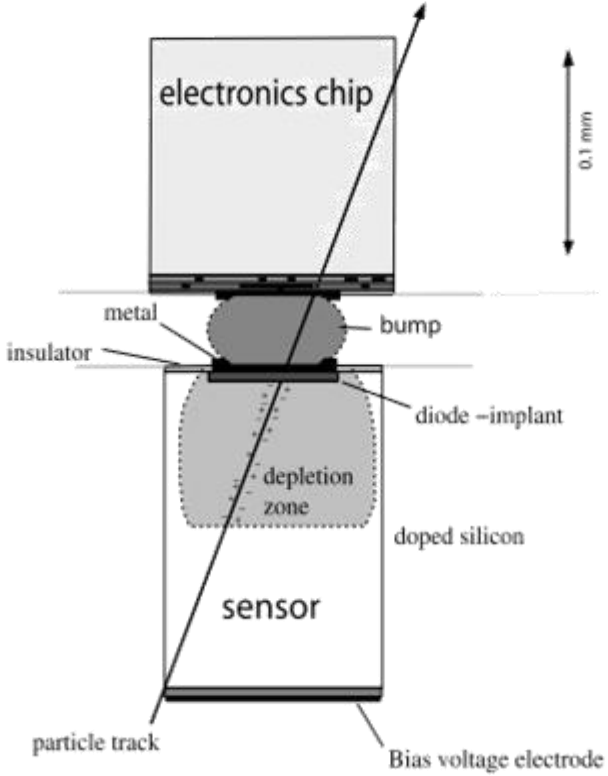
- Charge collected by drift
  - Reduce irradiation bulk damage
  - Control charge sharing
  - Improve charge collection speed

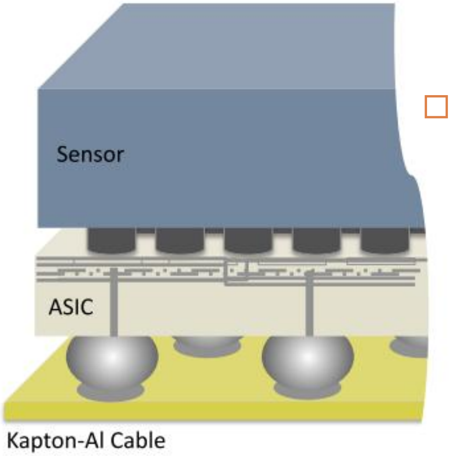
- Large Signal-to-Noise ratio
  - PID with large depletion region

- Tests on standard resistivity prototypes
  - Large breakdown voltage (>30 V) → 50 μm depletion is achievable
  - Small collection capacitance (<1 fF) → high S/N, small power consumption
  - Qualification for radiation hardness

Hybrid Pixel technology

- State of the art in LHC experiments
- CMOS chip + high resistivity (~80 kΩcm) sensor
  - Targets:
    - 50 μm + 100 μm thickness
    - Material budget $x/X_0 < 0.5\%$
- Charge collection by drift
- High S/N ratio: ~ 8000 e-h pairs/MIP ➡ S/N > 50

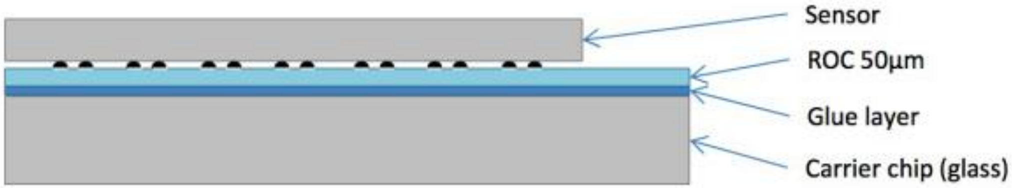


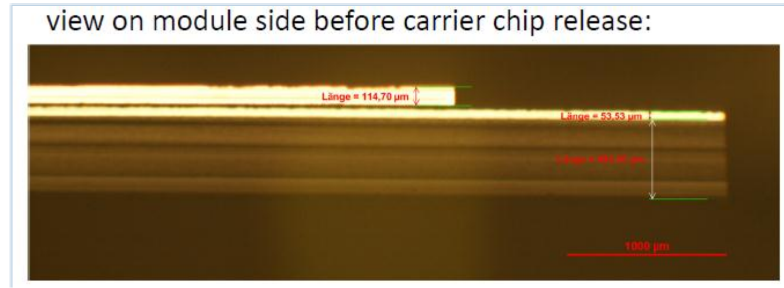


- Connections via bump bonding
  - Bump dimensions
    - Limiting the pixel size to 30 μm x 30 μm
  - High cost with fine-pitch
    - Limiting the application to larger surfaces

Hybrid Pixel R&D

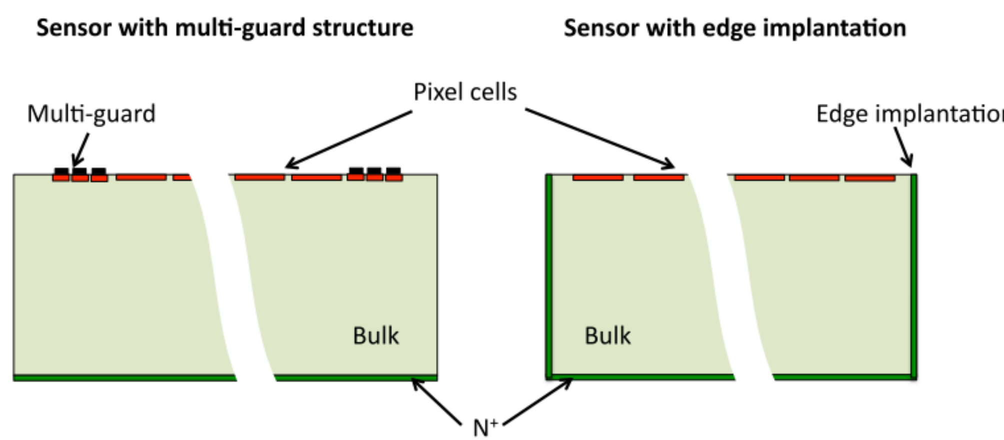
- Sensor thinning to 100 μm





Sensor 100μm, readout chip 50μm, glass carrier 300μm

- Edgeless detectors
  - Introduce a highly n-doped trench
  - Reduce the dead region
    - from ~ 600 μm to ~ 20 μm
  - Back-side removal for bumping



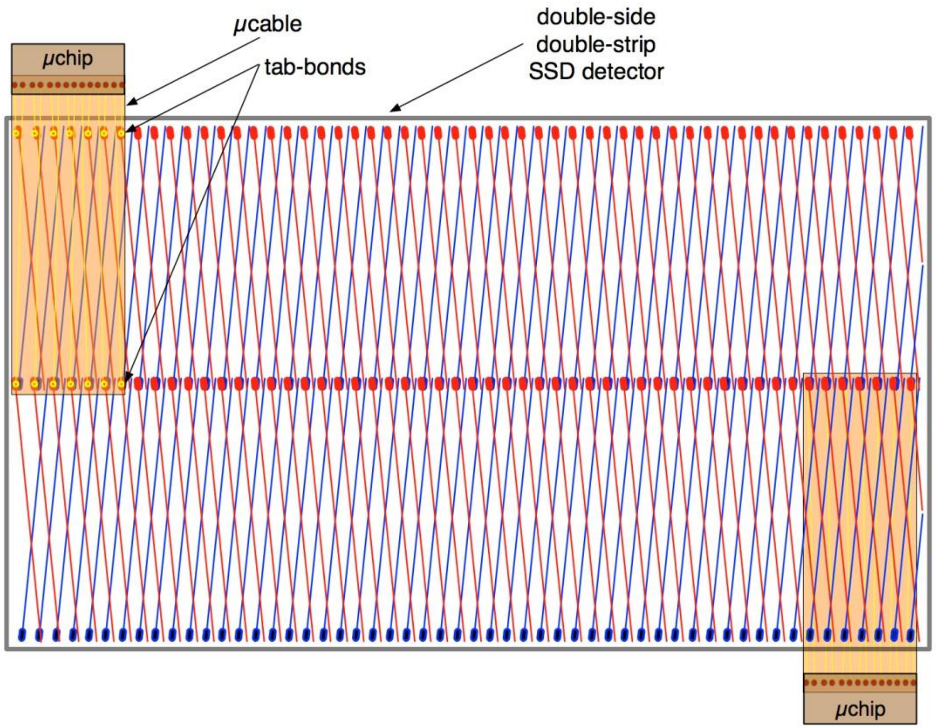
- Low-cost bump bonding
- Lower power FEE chip

Strip detector concept

- Sensor design based on current ALICE SSD
  - Standard 300 μm double-sided micro-strip sensors (7.5 cm x 4.2 cm)
  - 35 mrad stereo-angle between p- and n-side strips
- Reduced strip length down to 20 mm
  - Half cell-size: 95 μm x 20 mm
    - Higher granularity
    - >95% ghost hit rejection efficiency

Improvements

occupancy: - 50%
> ambiguity resolution
< capacitive noise
> S/N ratio
~ spatial resolution
< 2 x power consumption

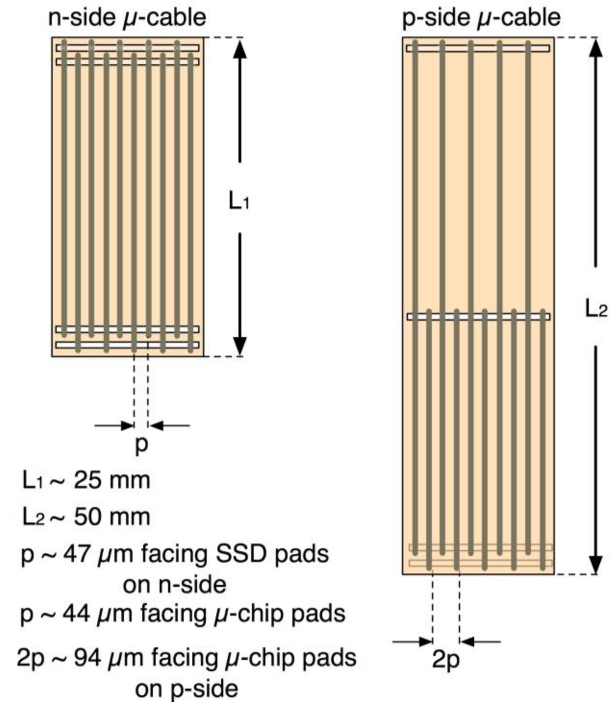


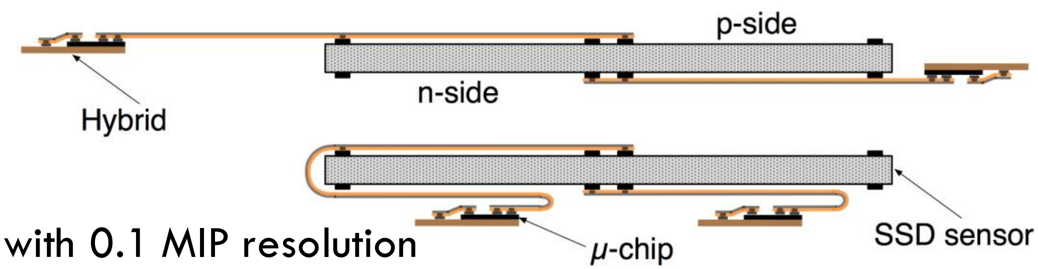
Drawbacks

- Doubled channel density
  - Challenging interconnections
  - Increased power consumption

Strip detector development

- Interconnection cables R&D
  - Micro-cables in aluminum-polyimide
  - Thickness: 10 µm + 10 µm
  - Pitch: 42.5-44.5 µm (chip) / 47.5 µm (sensor)
  - Length: ~ 25 mm / ~ 50 mm
- Assembly and folding
  - TAB bonding technique:
    - Allows chip tests, less material, safe folding
    - Challenging at pitch < 50 µm
  - Bonding test on dummy components
  - Compact module layout
- ASIC development
  - 0.18 µm technology (rad. hard)
  - 400 e⁻ noise (5 pF load)
  - Low power and fast ADC (10 bits)
  - Provide dE/dx over 20 MIP range with 0.1 MIP resolution

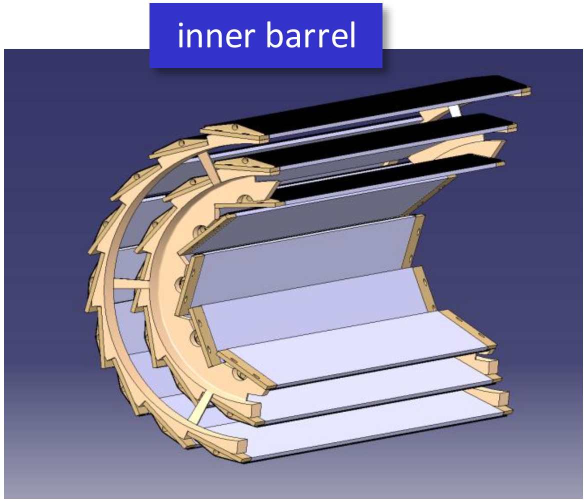




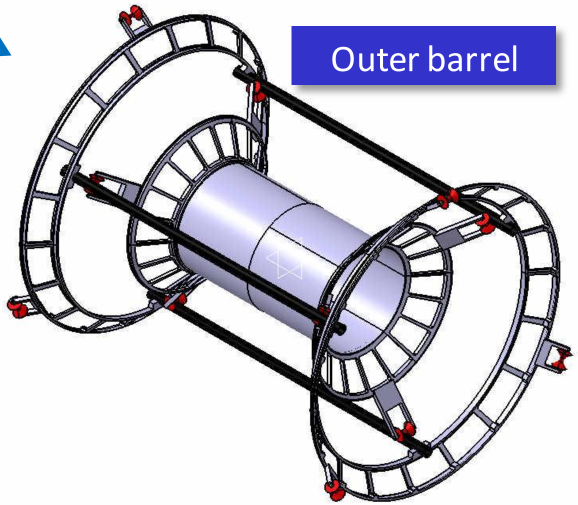
Support structure design

- ❑ Complete accessibility
- ❑ Maximum modularity
- ❑ Minimum material

- Inner barrel: 3 layers of pixels
  - 3-layer structure equipped held on carbon fiber wheels
  - Independent staves for testing/characterization



- Outer barrel: 4-layer structure
  - 4 pixel/strip layers mounted on 2 barrels
  - 3 tubes of carbon composite or beryllium, fixed between the two structures to provide rigidity and support/guide the inner part insertion



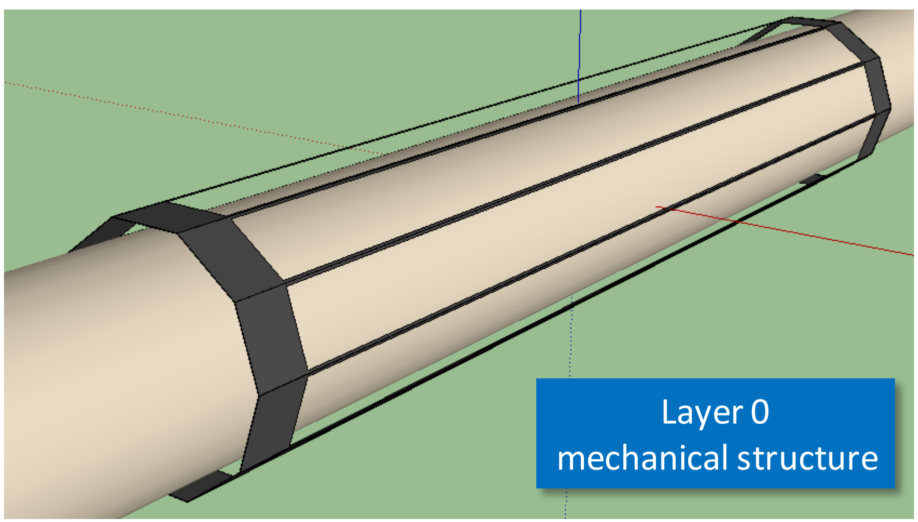
- Inner layer stave material budget

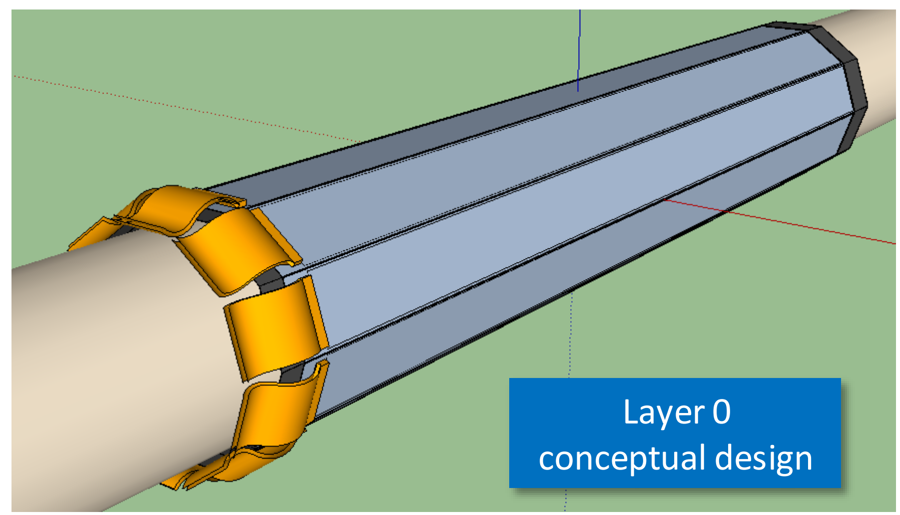
Component	Material budget X/X_0 %	Notes
Support Structure	0.07 – 0.22	carbon foam or polyimide or silicon
Glue	0.045	2 layers of glue 100 µm thick each
Pixel module	0.053 – 0.16	Monolythic (50 µm) – hybrid (150 µm)
Flex bus	0.15	single layer flex bus
Total	**0.32 – 0.58**	

Idea for an ultra-light innermost layer

- Very light structure with almost no material (only silicon) in the active area
- Very light stave without glue layers, electrical bus, etc.
  - Large silicon structures integrating the electrical bus for signal and power distribution
  - Stitching fabrication process
- No overlap to simplify the geometry
- Air cooling to avoid the extra material

$X/X_0 \sim 0.1\%$





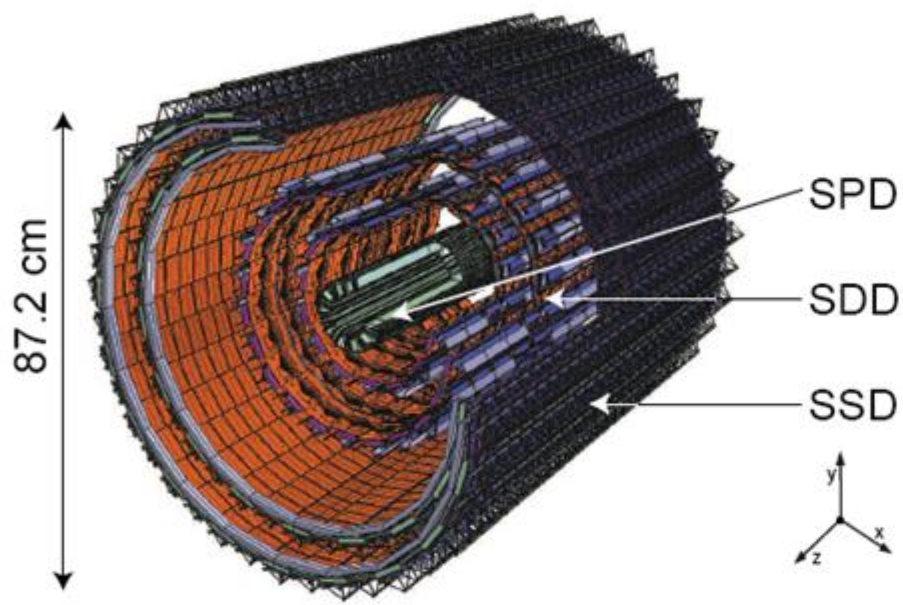
Conclusions

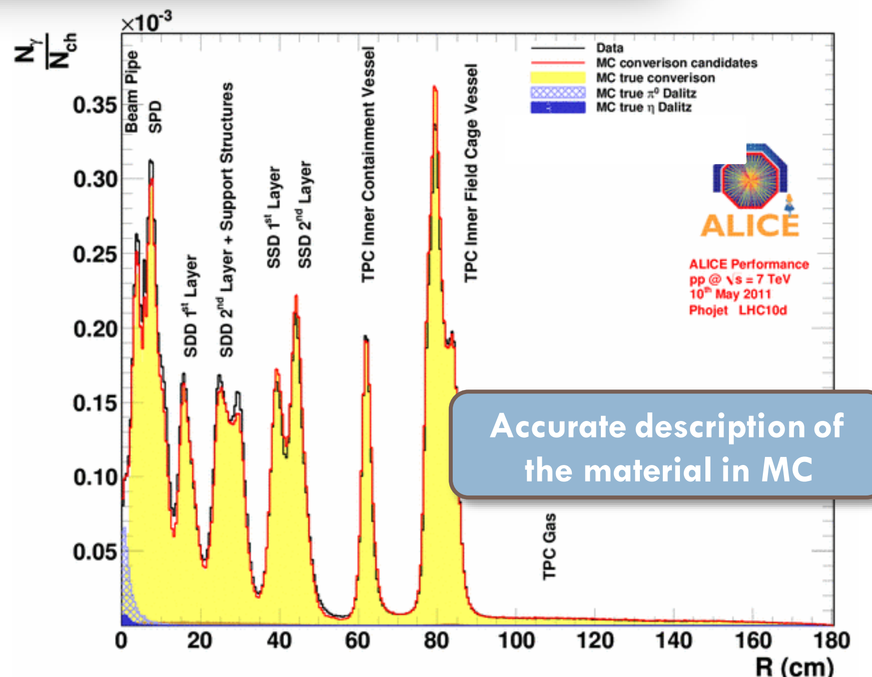
- The ALICE Silicon Tracker Upgrade is required to study:
  - Quark mass dependence of in-medium energy loss
  - Thermalization of heavy quarks in the medium
- New Tracker composed of 7 silicon layers characterized by:
  - Impact parameter resolution improved by factor 3x
  - First detecting layer @20 mm from the beam line
  - Material budget $x/X_0 \sim 0.3\text{-}0.5$ % in the first layers
  - High spatial precision (~ 4 μm in the first layers)
  - Very high standalone tracking efficiency down to low p_t (> 95% for p_t > 200 MeV/c)
  - PID capability
  - Fast access for maintenance
- Detector technologies considered for the Upgrade
  - Monolithic Pixel Detectors
  - Hybrid Pixel Detectors
  - Micro-Strip Detectors
- Low material budget supports allowing access and repair
- To be built and installed by 2019!!!

Backup slides

The present ITS parameters

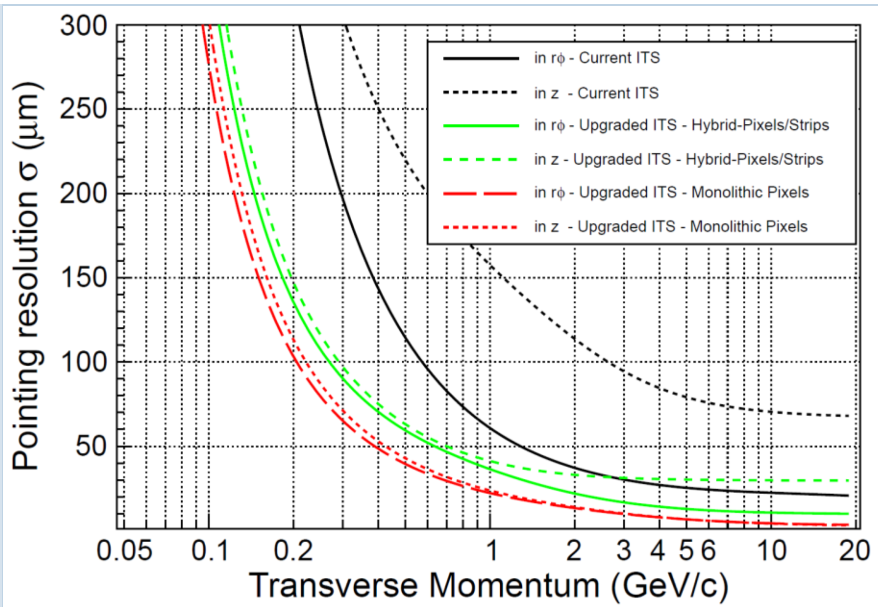
Layer	Det.	Radius (cm)	Length (cm)	Surface (m2)	Chan.	Spatial precision (mm)		Cell (μm2)	Max occupancy central PbPb (%)	Material Budget (% X/X_0)	Power dissipation (W)	
						rφ	z				barrel	end-cap
1	SPD	3.9	28.2	0.21	9.8M	12	100	50x425	2.1	1.14	1.35k	30
2		7.6	28.2						0.6	1.14		
3	SDD	15.0	44.4	1.31	133 K	35	25	202x294	2.5	1.13	1.06k	1.75k
4		23.9	59.4						1.0	1.26		
5	SSD	38.0	86.2	5.0	2.6M	20	830	95x40000	4.0	0.83	850	1.15k
6		43.0	97.8						3.3	0.86		

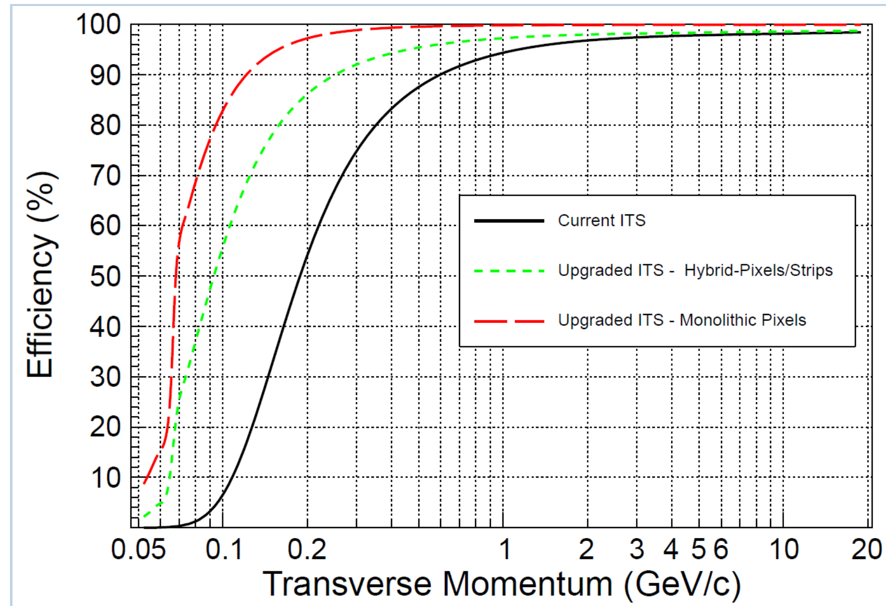




Accurate description of the material in MC

Improvement of impact parameter resolution & tracking efficiency





HYBRID PIXELS (state-of-the-art) and comparison with MAPS

Simulations for two upgrade layouts

Layout 1: "All New" – Pixels (7 pixel layers)

- Resolutions: $\sigma_{r\phi} = 4\ \mu m$, $\sigma_z = 4\ \mu m$ for all layers
- Material budget: $X/X_0 = 0.3\%$ for all layers

Layout 2: Pixel/Strips (3 layers of pixels + 4 layers of strips)

- Resolutions: $\sigma_{r\phi} = 12\ \mu m$, $\sigma_z = 12\ \mu m$ for pixels $\sigma_{r\phi} = 20\ \mu m$, $\sigma_z = 830\ \mu m$ for strips
- Material budget: $X/X_0 = 0.5\%$ for pixels $X/X_0 = 0.83\%$ for strips

radial positions (cm): 2.2, 2.8, 3.6, 20, 22, 41, 43

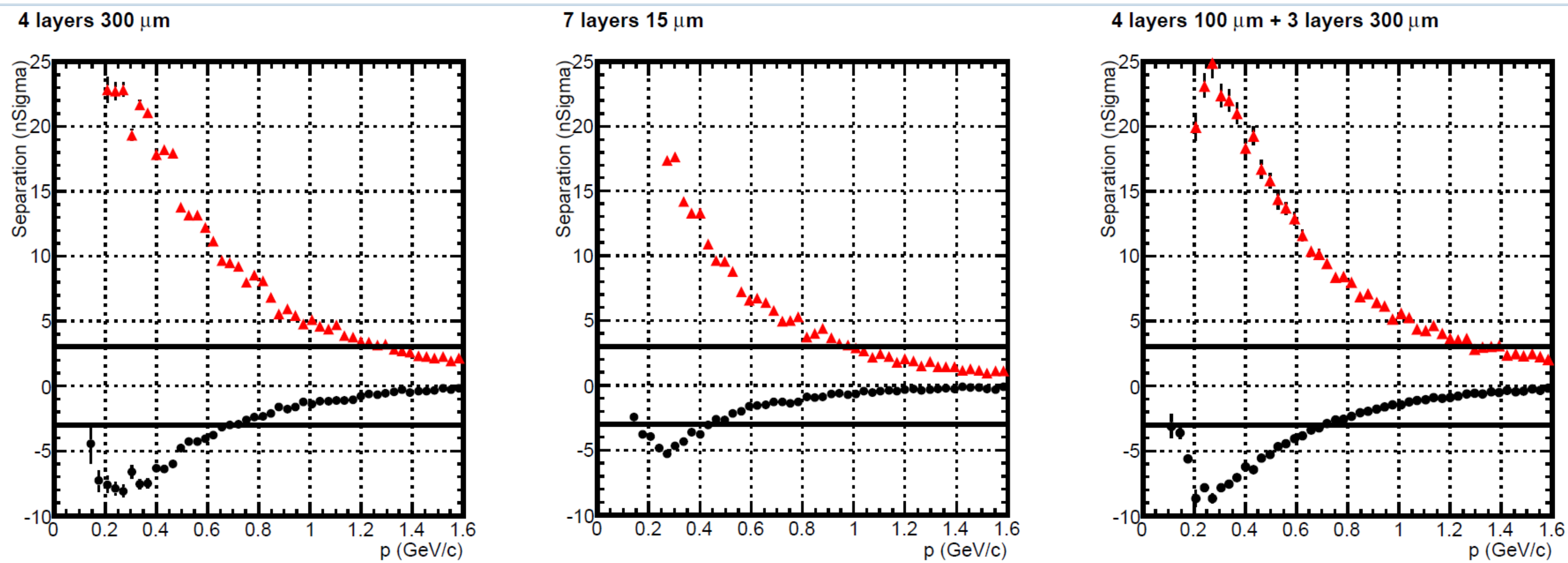
Same for both layouts

Material Budget

	Monolithic Pixels	Hybrid Pixels	Strips
Silicon Sensor	-	0.11% X_0 (100 um)	0.40% X_0
Silicon ASIC	0.05% X_0 (50 um)	0.05% X_0 (50 um)	0.15% X_0
Other components	0.25% X_0	0.25% X_0	0.28% X_0
Min. Target	0.30% X_0	0.41% X_0	0.83% X_0

ITS PID performance

4 layers silicon strips | 7 layers of MAPS | 4 layers of Hybrid + 3 layers of strips



- A Pion to kaon separation (black circles) and proton to kaon separation (red triangles) in unit of sigma in the case of 4 layers of 300 μm (left panel), 7 layers of 15 μm (central panel) and 4 layers of 100 μm + 3 layers of 300 μm (right panel) silicon detectors. The horizontal lines correspond to a 3 sigma separation.