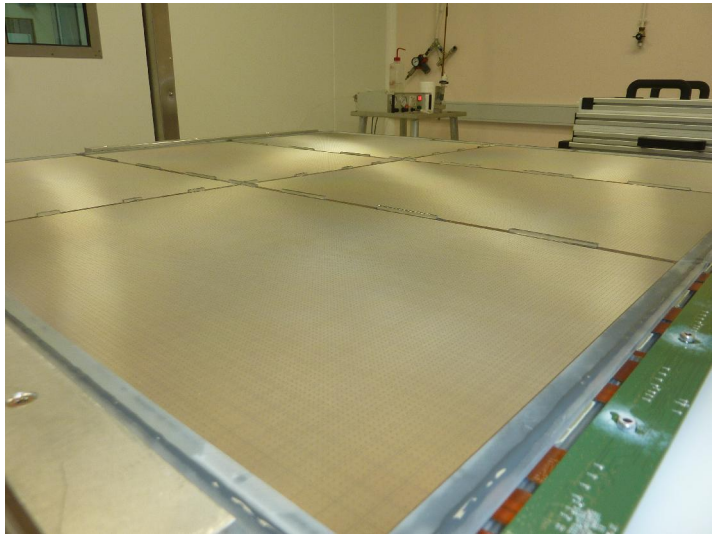
Recent results of Micromegas SDHCAL with a new readout chip



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Linear Collider Detector group
RD51 mini-week, CERN, 21-23 Nov. 2011

Overview

1. New 1 m^2 Micromegas prototype
2. Electronics and Bulk test
3. Performance in beam

1. New 1 m^2 Micromegas prototype

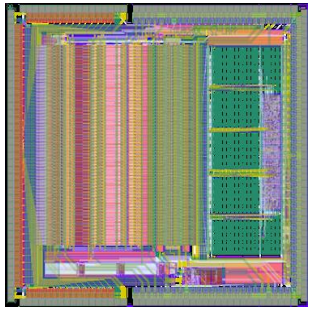
1.1 New front-end chip
MICROROC replaces HARDROC2
Peaking time between 100-200 ns

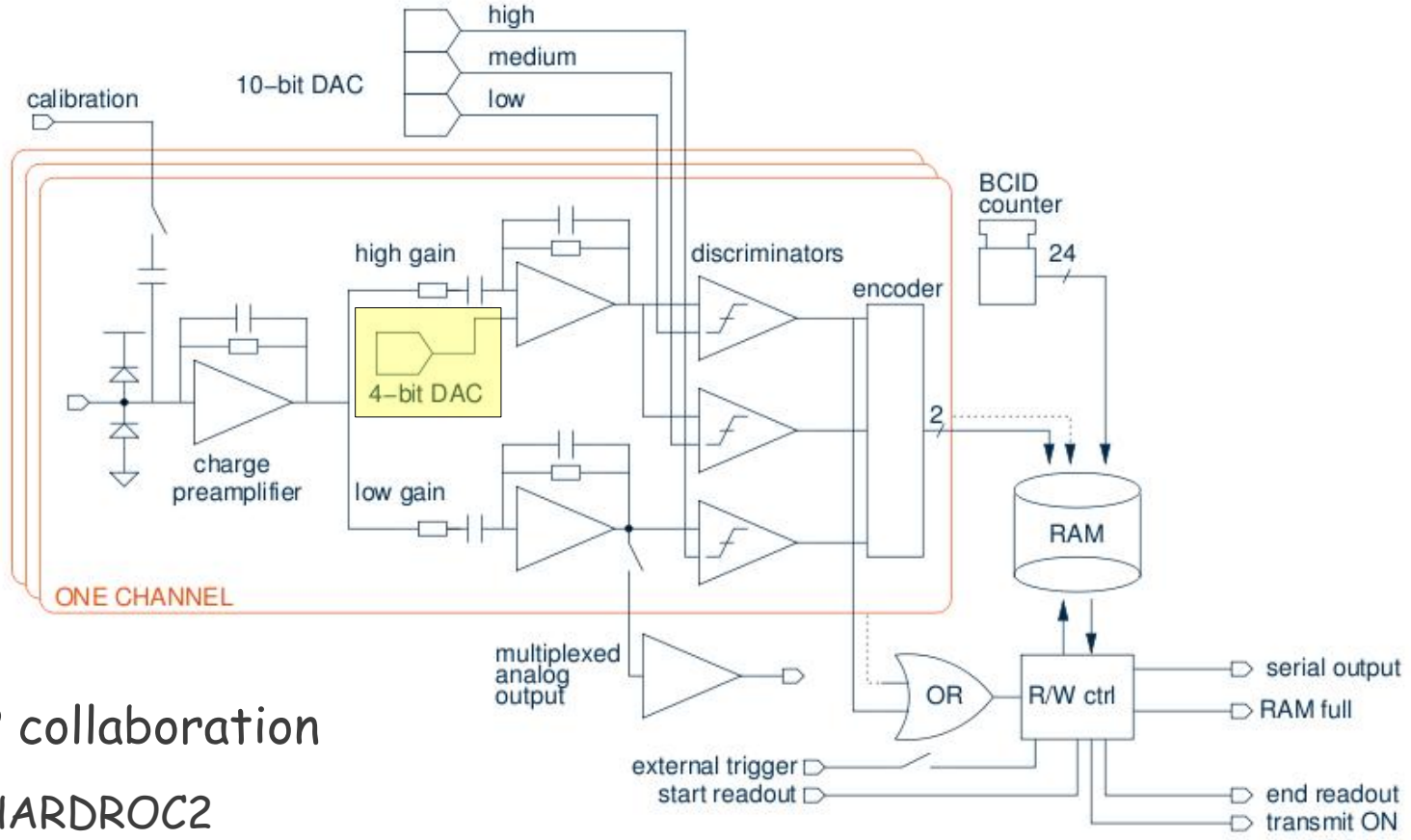
1.2 New Active Sensor Units
Improved spark protection
and EM compatibility

1.3 Improved mechanical design
Thinner chamber

DAQ and software
No changes
All available from last year

1.1. New ASIC, Microroc



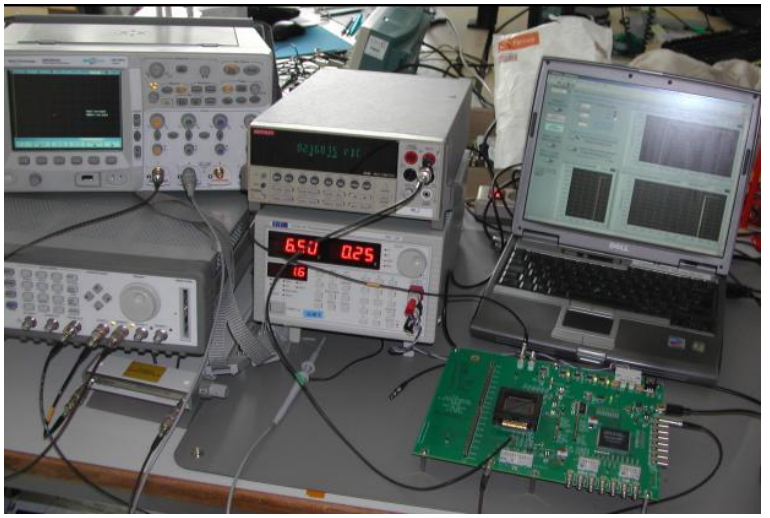


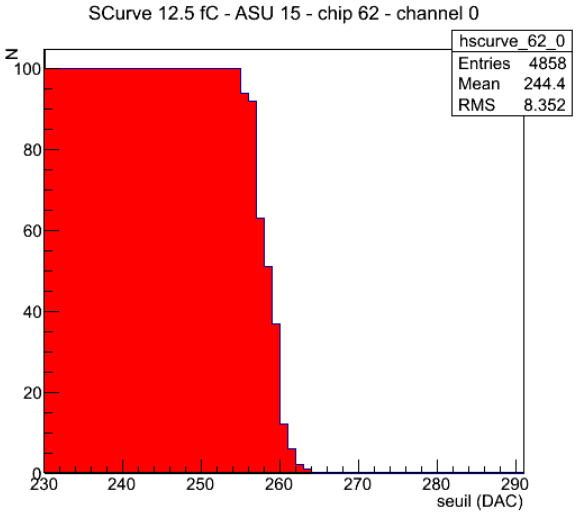
- LAL/Omega and LAPP collaboration
  - Same digital part as HARDROC2
- New analogue part
  - Spark protection inside silicon
  - Low noise charge preamplifier
  - 2 shapers of high/low gain
    with variable peaking time (30-200 ns) and dynamic range of 200 and 400 fC
  - Other features: pedestal alignment (offset) DAC, multiplexed analogue readout

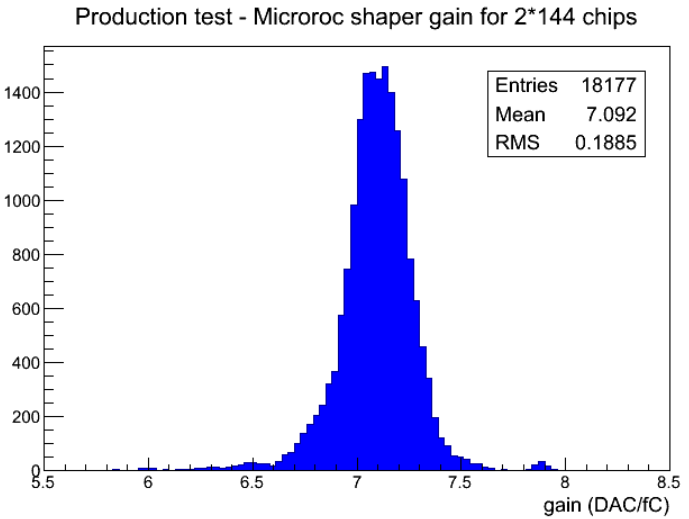
Chip threshold + channel offset
→ virtually 1 threshold / channel

1.1. MICROROC status

- 341 chips produced
  - Tested on test board at LAPP
  - Gain of high gain shaper
    - Scurve of pedestal + 1 test charge (50 fC)
  - Average gain of 7.09 DAC/fC
  - Yield of 91.5 %
- 312 chips can be used for next prototypes





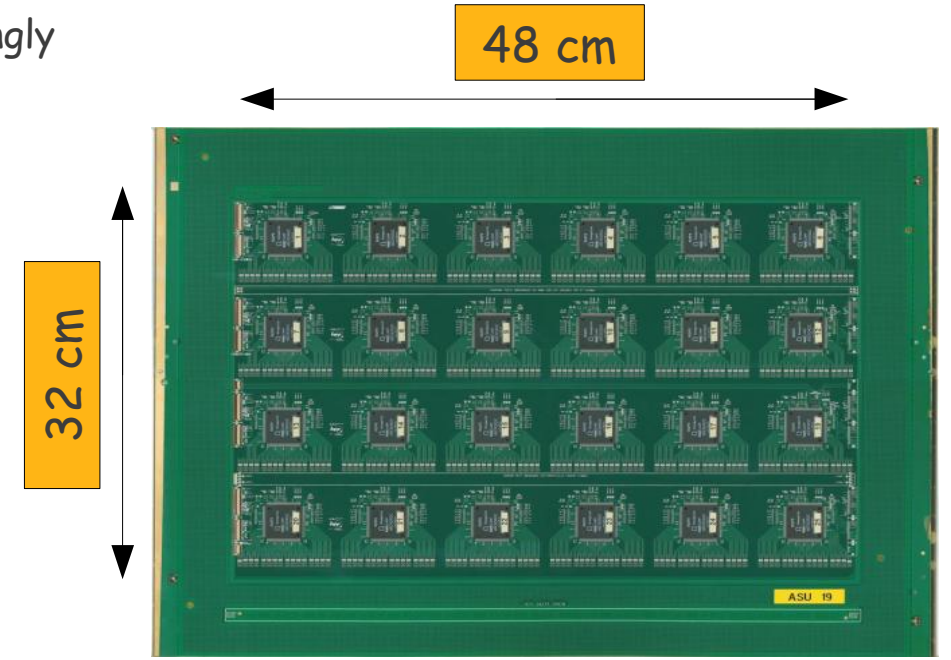


1.2. New Active Sensor Unit

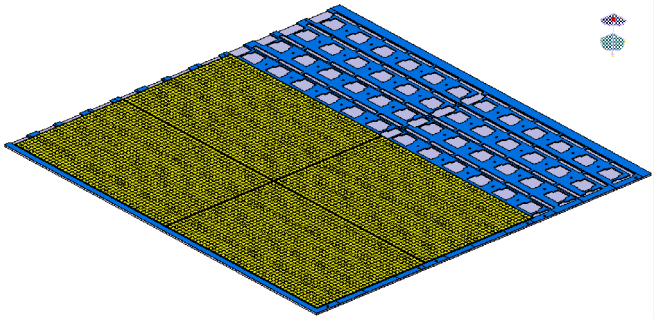
- New PCB routing
  (minor modif. thanks to HR2/MR1 pin-to-pin compatibility)
  - Improved EMC minimizes detector/digital signals X-talk
    3 noisy channels /chip with previous design
  - Chip bypass correctly rooted
    Usefull to identify possible faulty chips (not used so far)
  - Digital + Analog readout
    Allow for detailed characterisation
    + Provides a way to monitor thresholds inside calorimeter
  - Temperature probe
    Monitor T inside HCAL and adjust thresholds accordingly

312 chips
→ 13 ASU of 24 ASIC
→ 2 prototypes

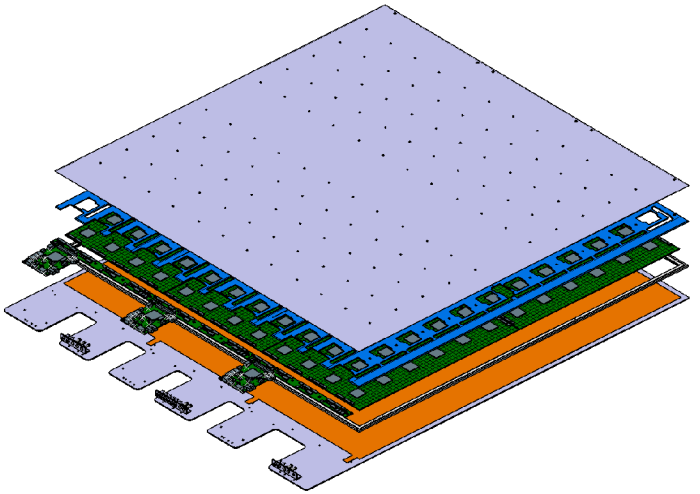
- Improved PCB spark protection network
  - Faster
    Choise based on test of several networks
    from different manufacturers
  - More compact
    Still takes a lot of space on PCB:
    - Burried protections
    - Resistive coating of anode plane



Improved m^2 prototype design

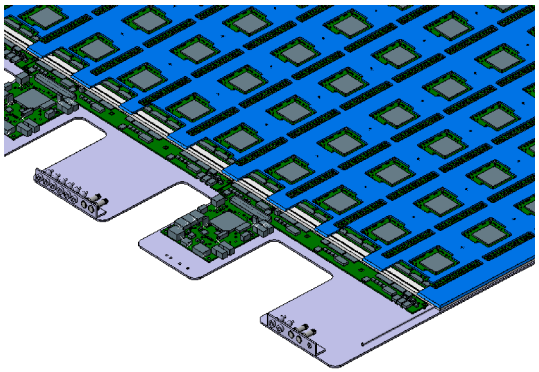


- Gas tightness made by ASU, side frame and drift plate
  → Steel baseplate not necessary anymore (-2 mm)
  → Baseplate screwed instead of glued



  * Gives access to ASIC side of ASU
    - Check digital signals and debug
  * Eventually: get rid of Fe baseplate
    - CLIC W-HCAL : less steel
    - ILC Fe-HCAL : improve absorber stiffness (+2mm)

- ASU mask thickness reduced from 3 to 2 mm (-1 mm)
  → Thinned chamber (7 instead of 8 mm active thickness)



- Easier access to DIF connectors and LV & HV patch panel when chambers are inserted inside structures

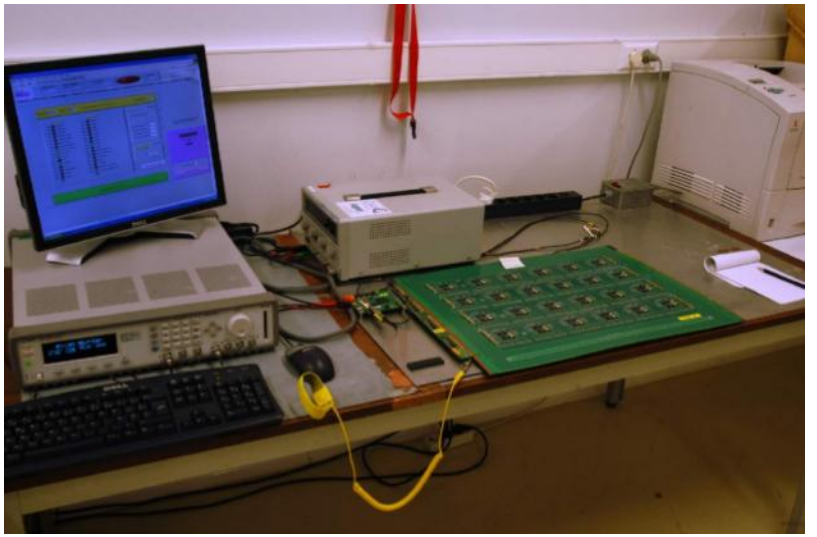
2. Electronics and Bulk test

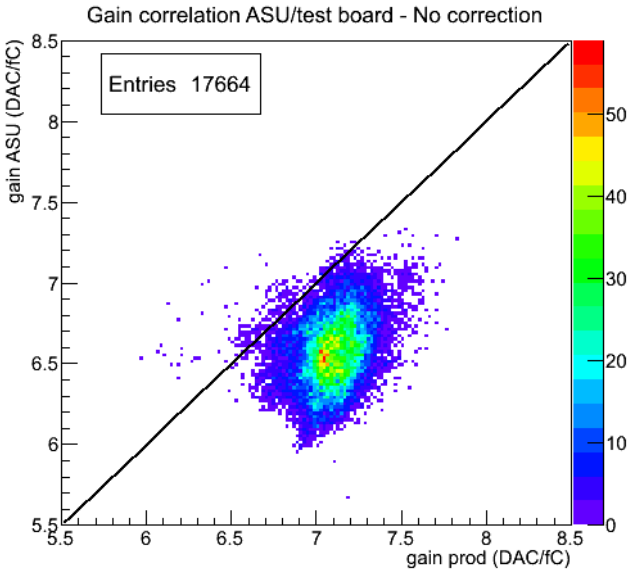
2.1 Electronics test
Check chip functionality on ASU
Determine settings
(3 thresholds and pedestal offset)

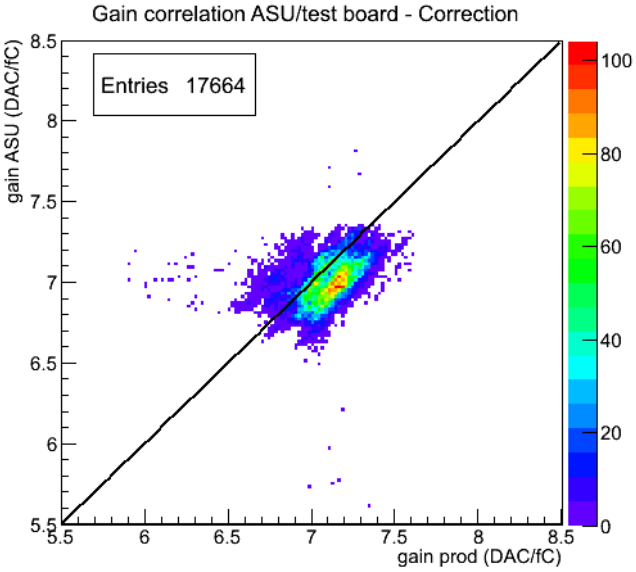
2.2 Bulk test
Check full detection chain
(55Fe quanta counting)

2.1. Electronic test (I)

- Check chip functionnality
  - Before/after Bulk
  - Before/after HV training
- Comparison with single chip measurements
  - Correct for PCB line resistance
  - Good agreement



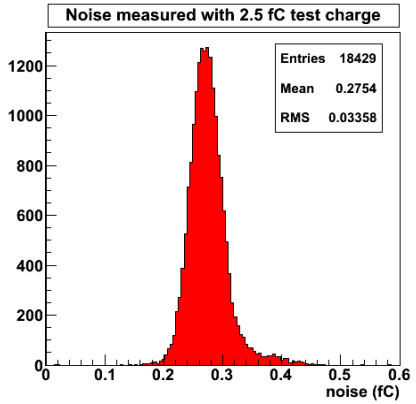


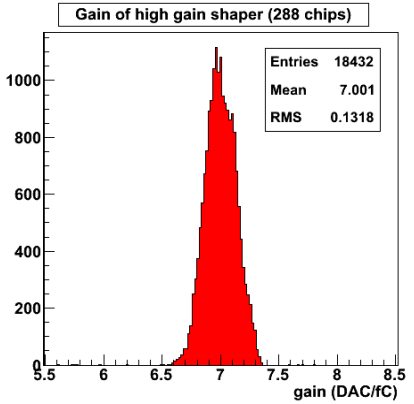


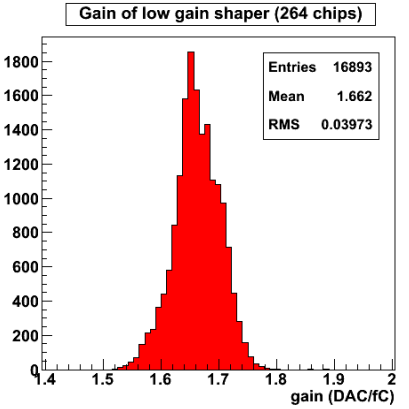
No impact of Bulk lamination and HV training on chip performance

2.1. Electronics test (II)

- Measure chip performance
  - High gain shaper noise
    → minimum detection threshold
  - High and low gain shaper gains
    → adjust 3 thresholds
- Over ~18k channels
  - Noise: (0.28 +/- 0.04) fC
  - High gain: (7.00 +/- 0.14) DAC/fC
  - Low gain: (1.66 +/- 0.04) DAC/fC



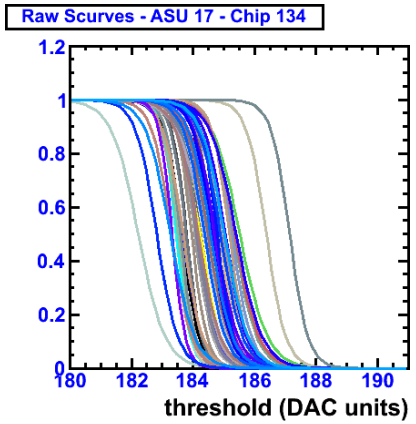


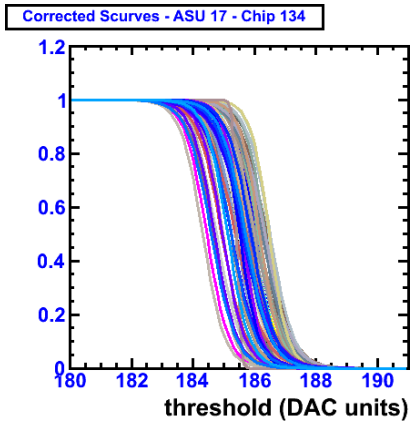


To be expected: Low channel threshold + Uniform detector response

2.1. Electronics test (III)

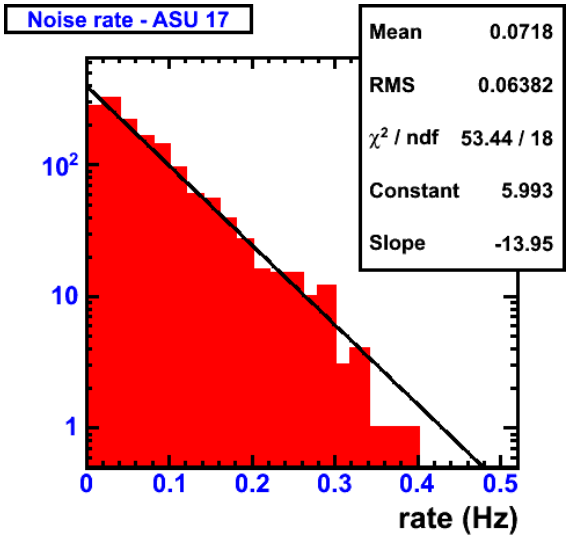
- Determine working settings
  - Determine channel pedestal offset
  - Set value of 3 chip thresholds





Control noise rate and threshold with pedestal offset DAC

- For low threshold
  - Align pedestal for uniform noise rate
    → offset map
    → uniform detection threshold
- For medium and high thresholds
  - Make use of measured shaper gains

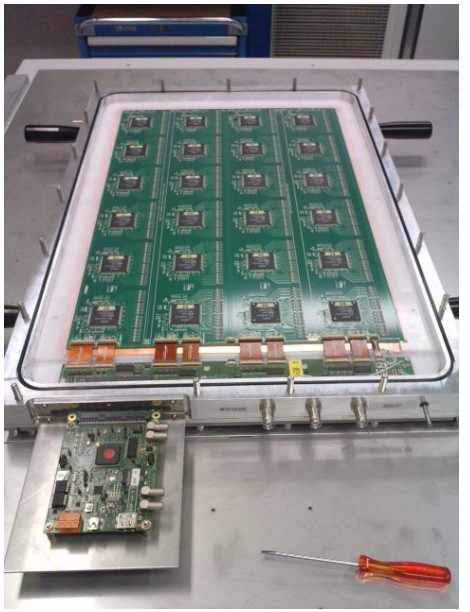


2. Test in gas

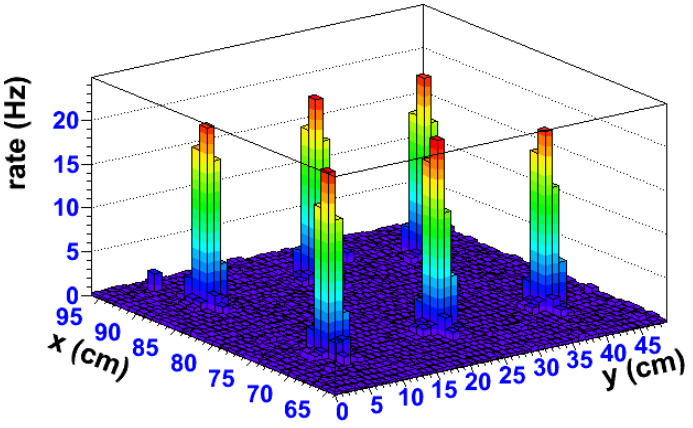
- Clean Bulk from impurities by sparking
  - Increase HV until Paschen's limit is reached (800 V)

- Verify full detection chain and chip settings
  - Place ASU inside test chamber
  - Count ^{55}Fe conversions in 1 cm drift gap
- Photopeak detection (~230 e-) at 260 V in Ar/CF_4/iso 95/3/2!
  → Much better than with HR2 (390 V in Ar/iso 95/5)
  → promising for MIP charge detection (MPV of ~14 e-)

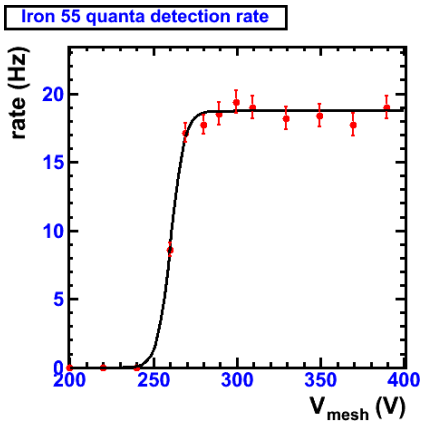
230 e- detected at a gas gain of 100!



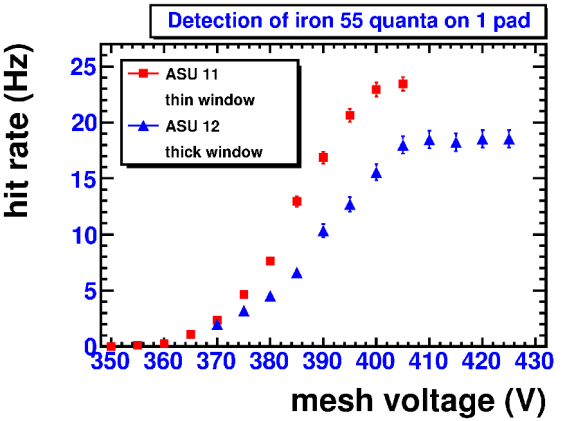
^{55}Fe source profile on 6 positions



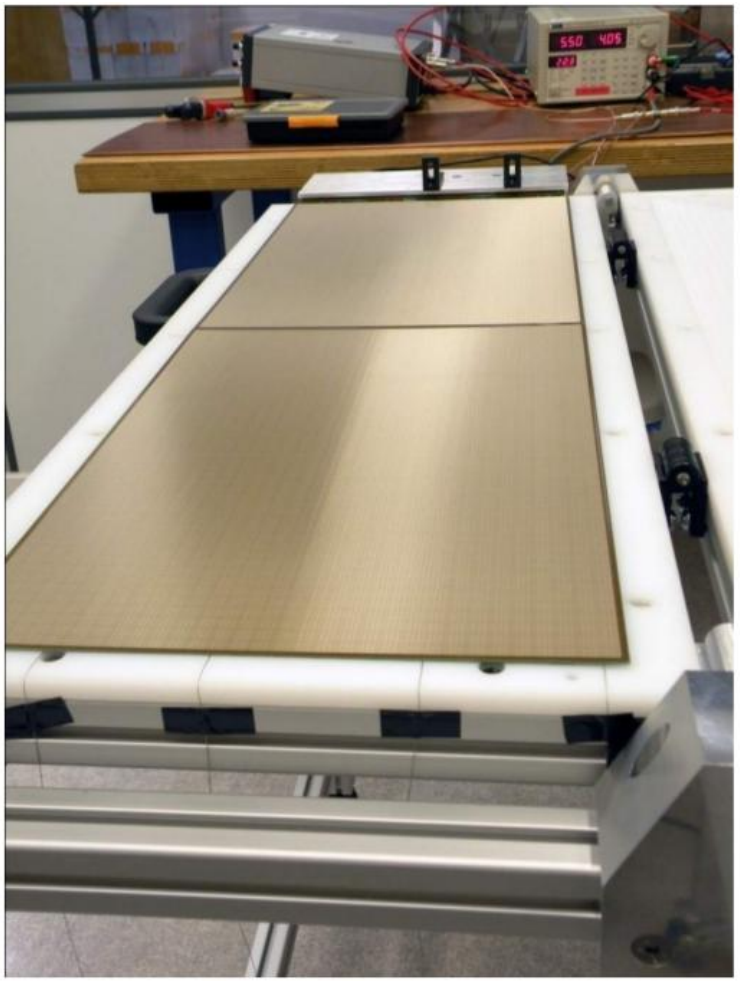
MR1 ASU triple mix.



HR2 ASU double mix.



M2 prototype assembly- June 2011

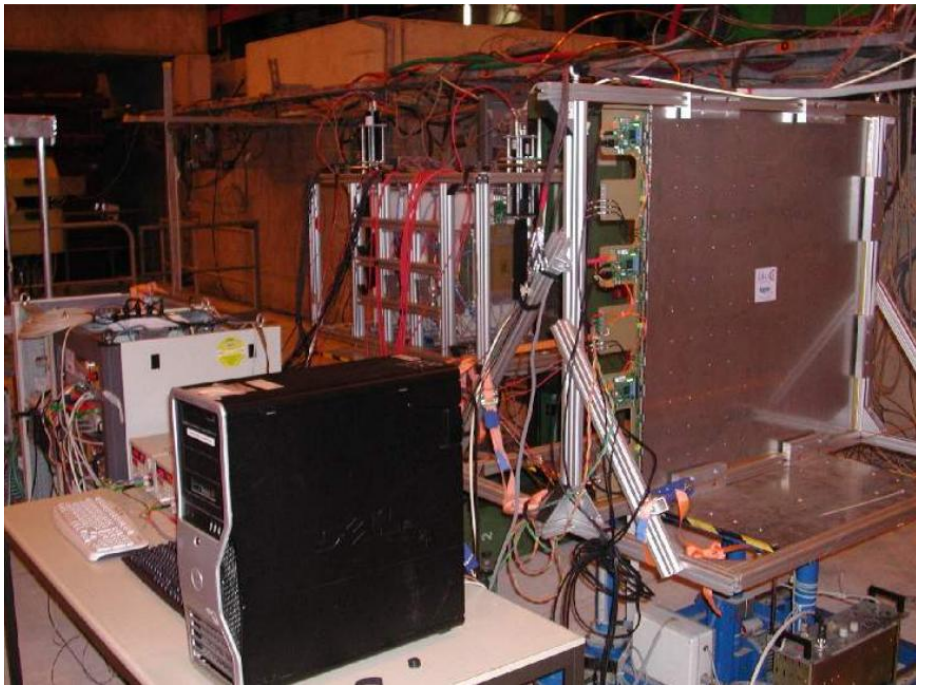


New tools to manipulate SLAB
→ Easier assembly procedure
(takes 1 week)

3. Performance in beam

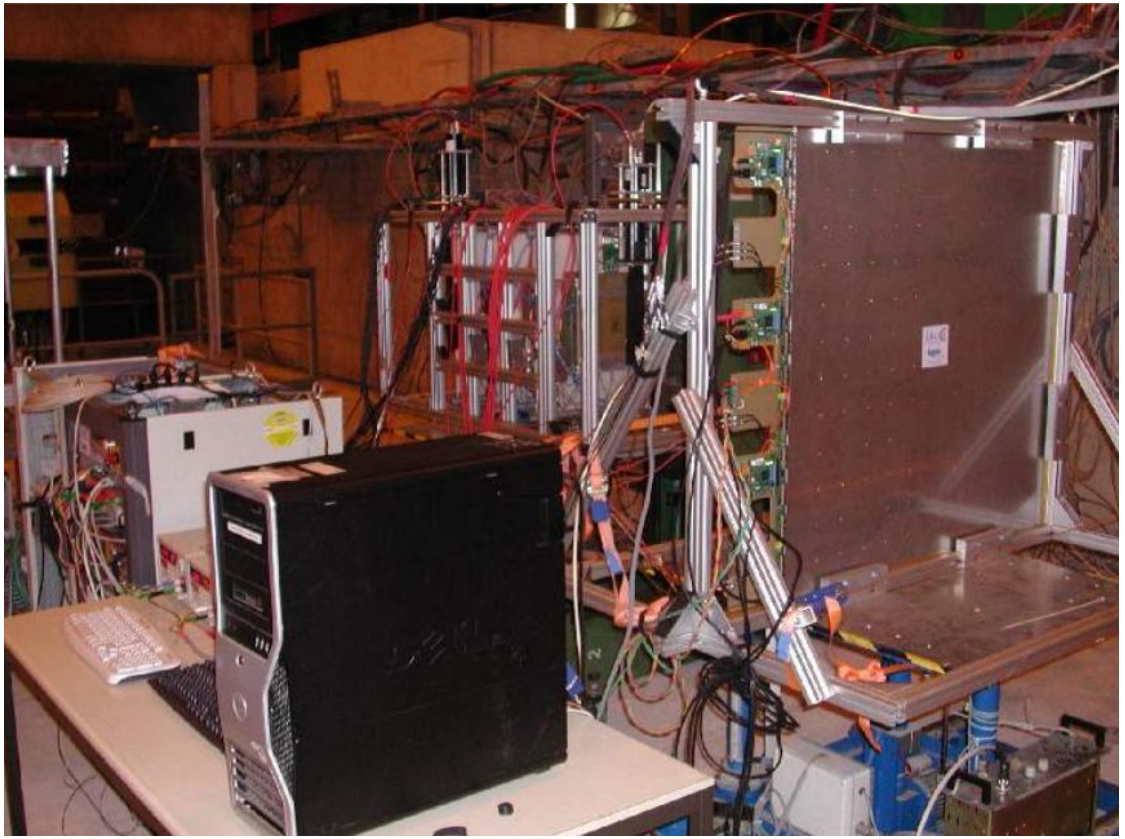
3.1 July 2011 test beam

3.2 Noise
3.3 Mesh voltage scan
3.4 Uniformity
3.5 Threshold scan
3.6 Angle scan
3.7 Analogue Readout
3.8 Hadronic showers



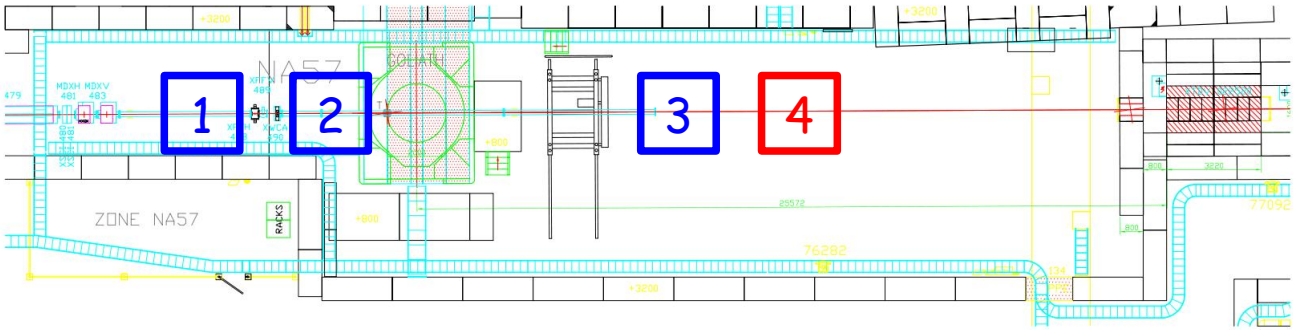
3.1. July 2011 TB - Setup

- SPS/H4 3-22 August
  - 6 days standalone CALICE
  - 13 days multi-users RD51
    4 set-ups



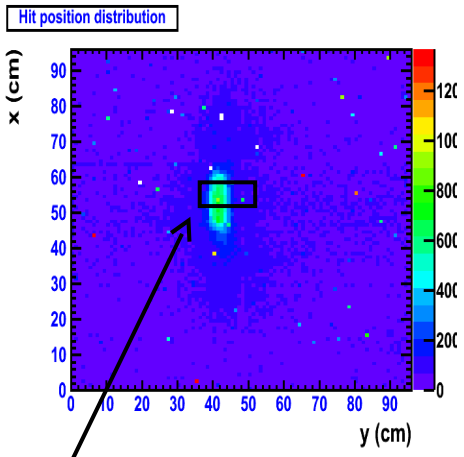
- Setup
  - 3 scintillators, overlap area of 6x16 cm^2
  - Pad (LAPP) and strip (RD51 uM) telescope
  - 1 m2 prototype
  - Non flammable (T2K) gas !
  - Hardware Synchronization telescopes and prototype with busy handshake

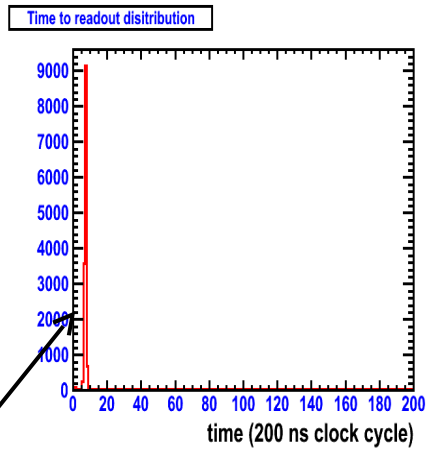
- 6 M events recorded
  - Muons/pions 85/15

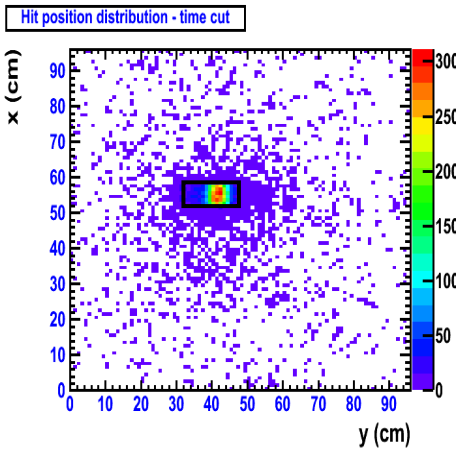


3.1. July 2011 TB - Starting-up

- Installation on 03/08 MD morning
- Noise measurement in the afternoon,
  pedestal and thresholds settings of Microroc chips,
  start flushing gas
- Muon beam 04/08 morning, first beam profile at 8 pm!







Pad chambers

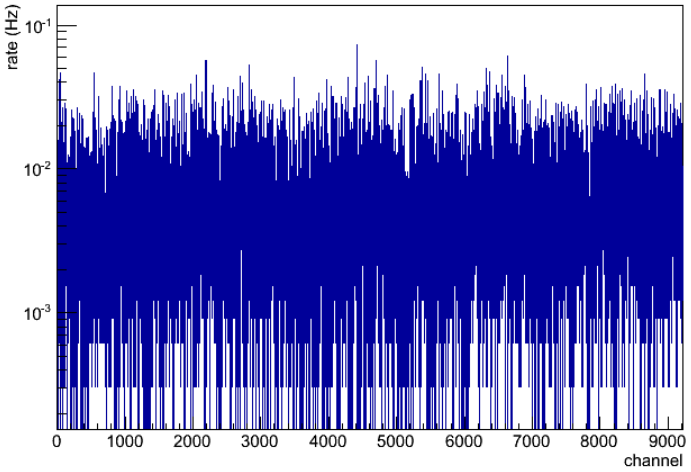
Hits in coincidence
with triggers from scintillators

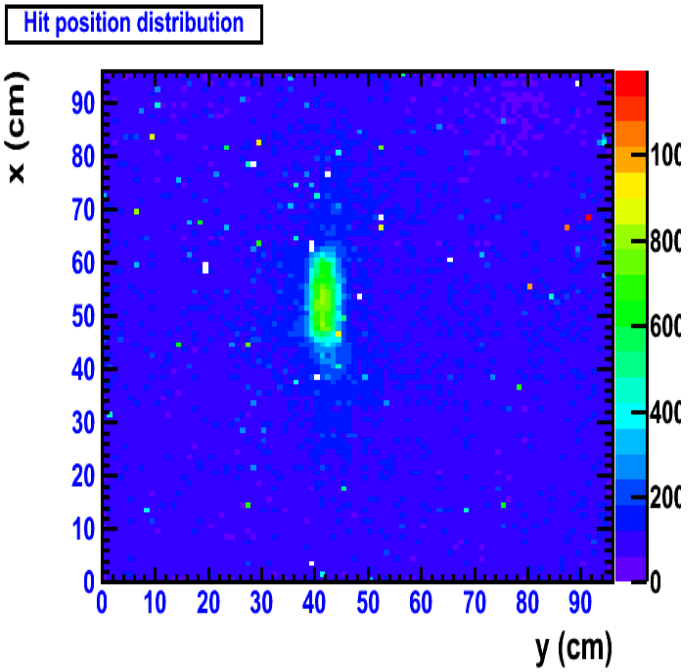
→Telescopes and scintillators structure rotated by 90° to increase coincidence events

3.2. Noise conditions

- Very good noise conditions
  - Pedestal alignment w.r.t. low threshold such that average channel noise rate is 10 mHz
  - Less than 10 noisy channels over 9216 during whole test beam → masked
  - Threshold of about 1 fC
- Time to fill the chip memories up (RAMFULL) = 127 * 0.01 / 64 ~ 200 s if no HV
  With HV: contribution from cosmics → 20 s
  → Memories reset at 0.05 Hz
  → Low enough to see all beam particles (~200 Hz)!

Noise equalization to 10 mHz





V_{mesh} = 360 V
RAMFULL mode
All data from detector.
No cut applied.
Very quiet!

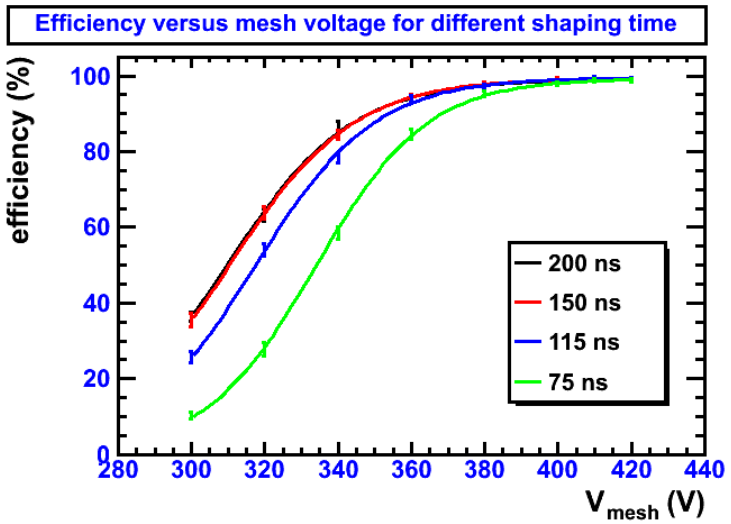
3.3. Preliminary results – Voltage scan

- Efficiency
  - Plateau reached for 4 shaping time
  - Detector signal is 115-150 ns

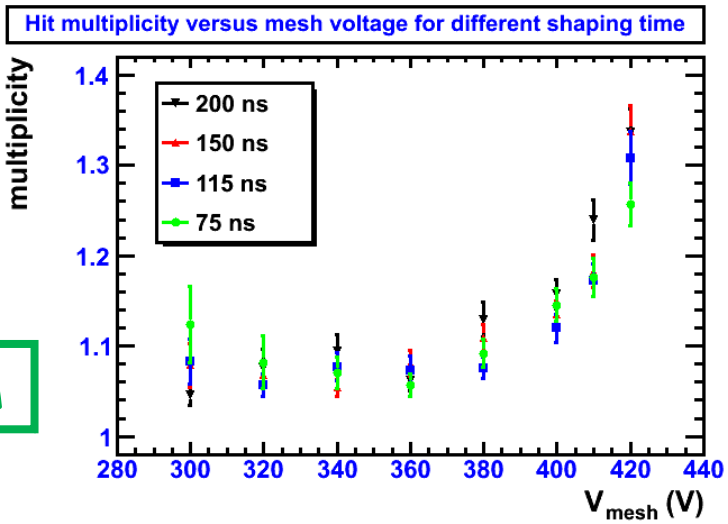
  At 150 ns shaping
  - > 95 % at 365 V
    Gas gain is 1000 only!

- Multiplicity
  - Below 1.1 for efficiency larger than 95 %
  - Compatible with previous measurements

→ Standard settings
200 ns shaping, 1 fC threshold, V_{mesh} = 390V, Gain = 3000, V_{drift} = 480V
efficiency = 98 %, multiplicity = 1.1, noise rate = 10 mHz/channel

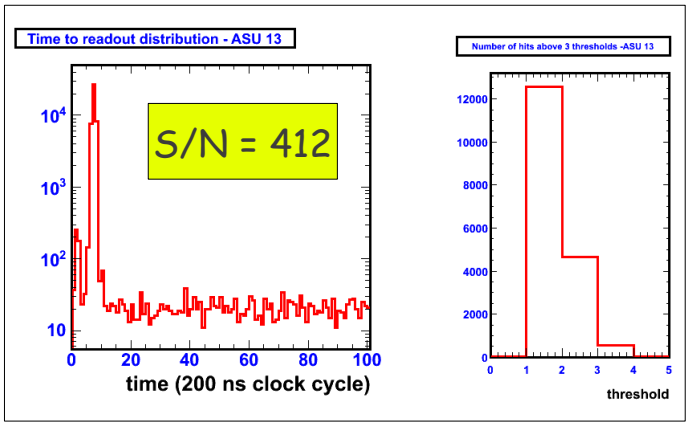


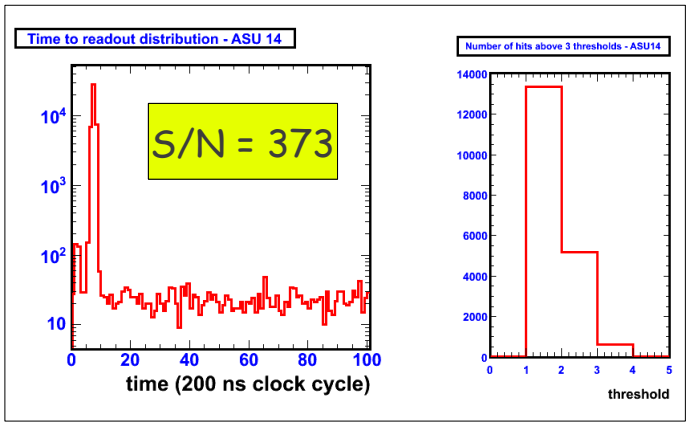
Muon Beam

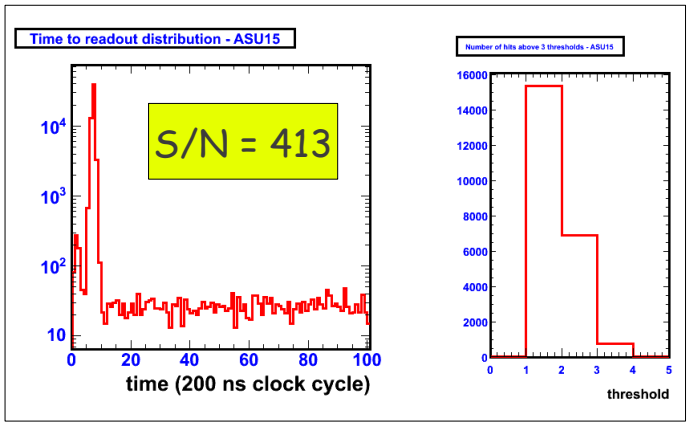


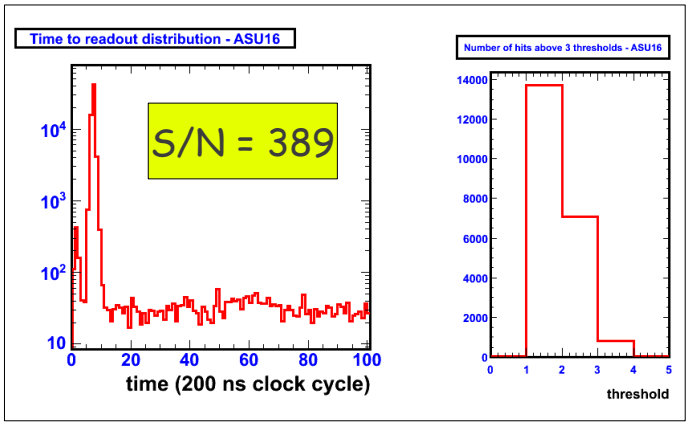
3.4. Preliminary results – Uniformity

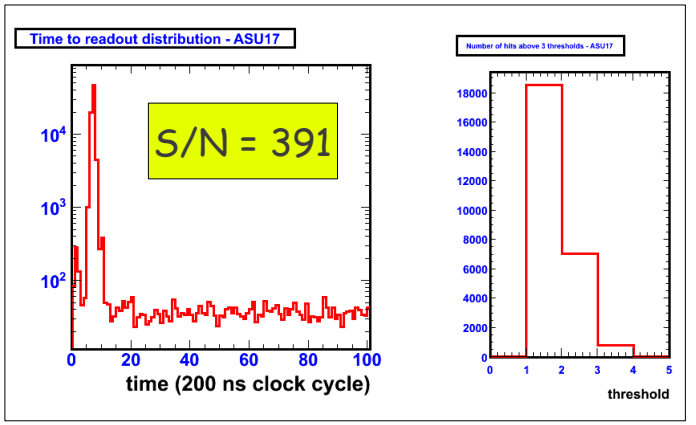
- Global response uniformity (beam area of 6x16 cm^2) over the six Bulk
  - Efficiency: 96-98 % ASU center and 91-92 % ASU junction
  - Multiplicity: 1.08-1.10
  - Signal to noise ratio: 350-450
  - Number of hits above 3 thresholds shows some variations (probably P/T or calibration uncertainty)
- Next steps: measure variations per 3x3 pad area over 2/3 of total prototype area

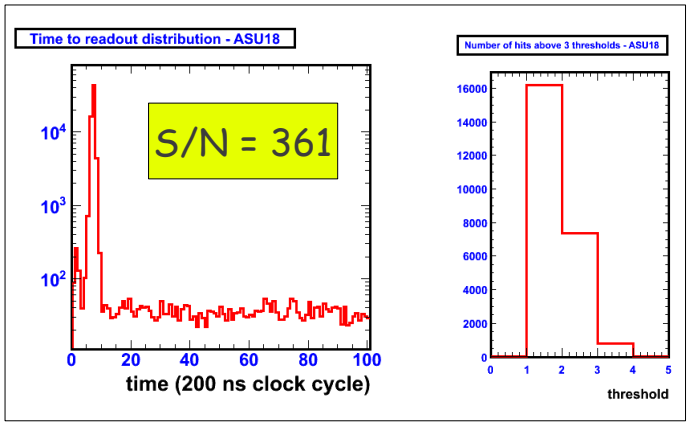








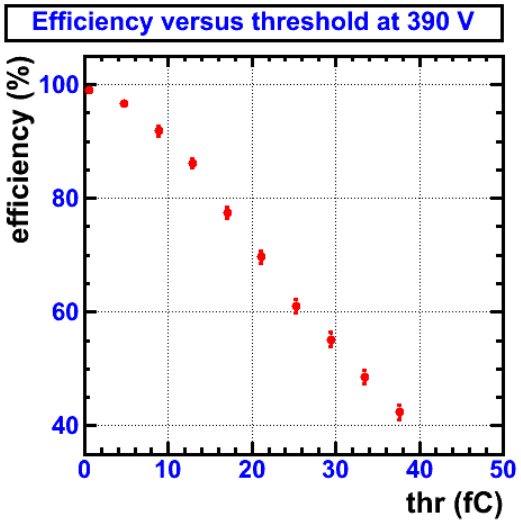


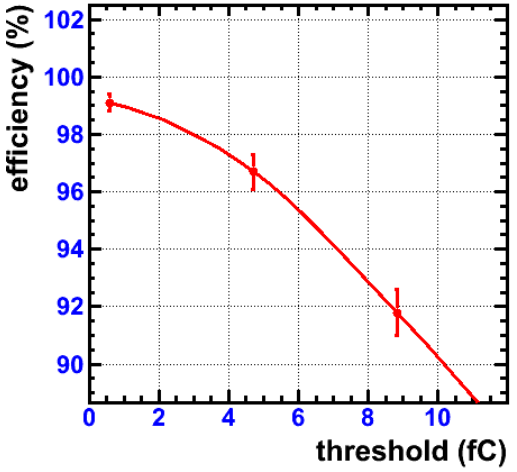


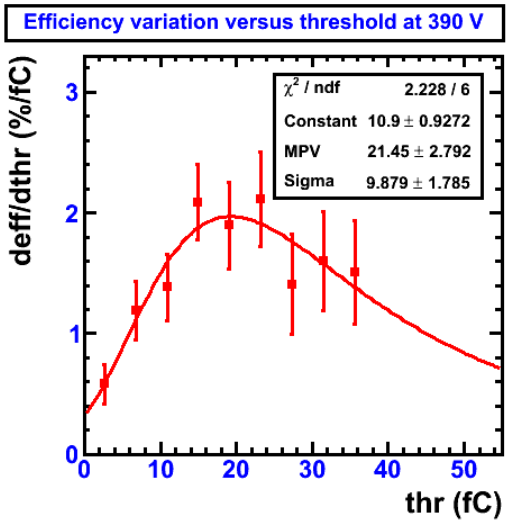
3.5. Preliminary results – threshold scan

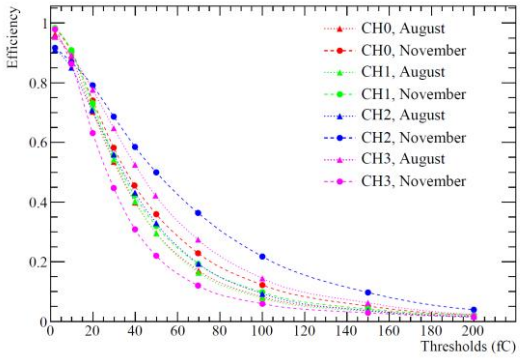
- Minimum threshold ~ 1 fC
  efficiency > 98 %
  noise rate = 10 mHz/channel
- Increasing threshold to 2 fC,
  noise negligible, efficiency still > 98 %

- Muon Landau MPV
  - With 70 % efficiency,
    threshold = MPV = 20 fC
- Taking differential of eff(thr)
  - Yields ~ 22 fC





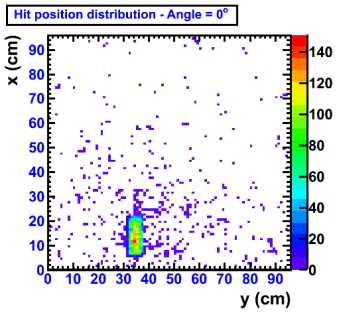




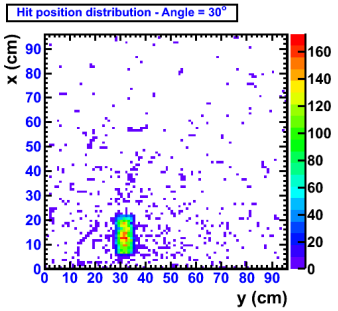
Well compatible with 2008 beam tests
(analog readout, threshold cut offline)

3.6. Preliminary results – Angle scan

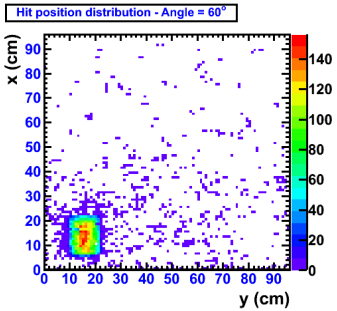
Different angle of beam incidence (0°, 30°, 60°)
(at 0° the beam direction is perpendicular to the m^2 prototype plane)



0°

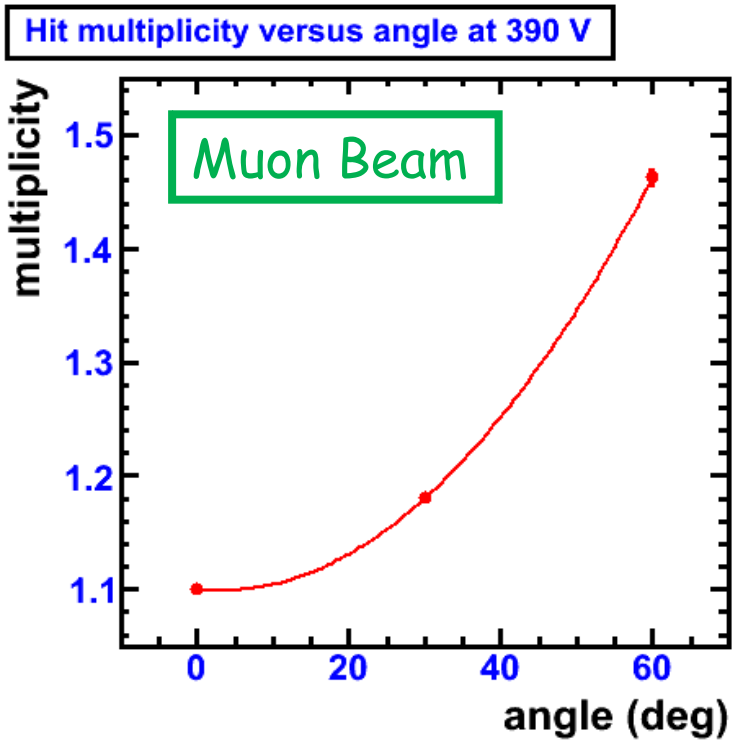


30°



60°

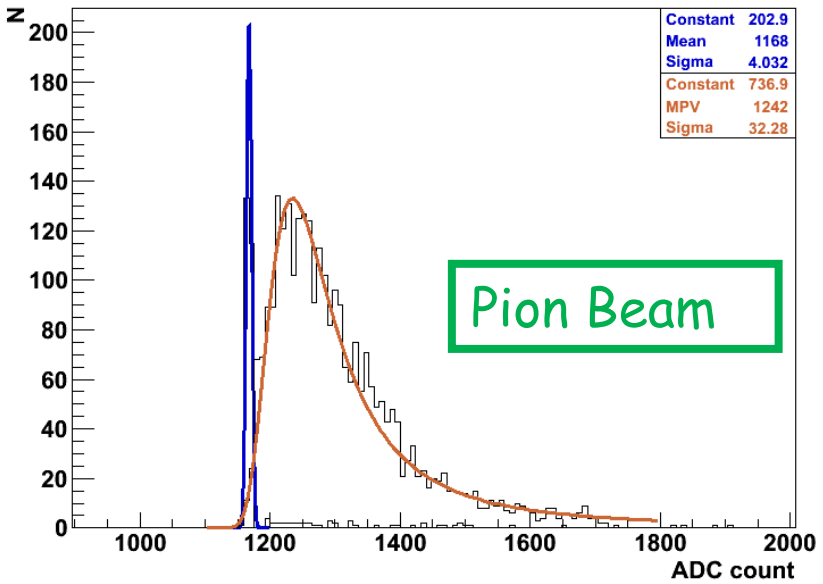
Expected increase of multiplicity with angle
Remains reasonably small: at 60°, below 1.5

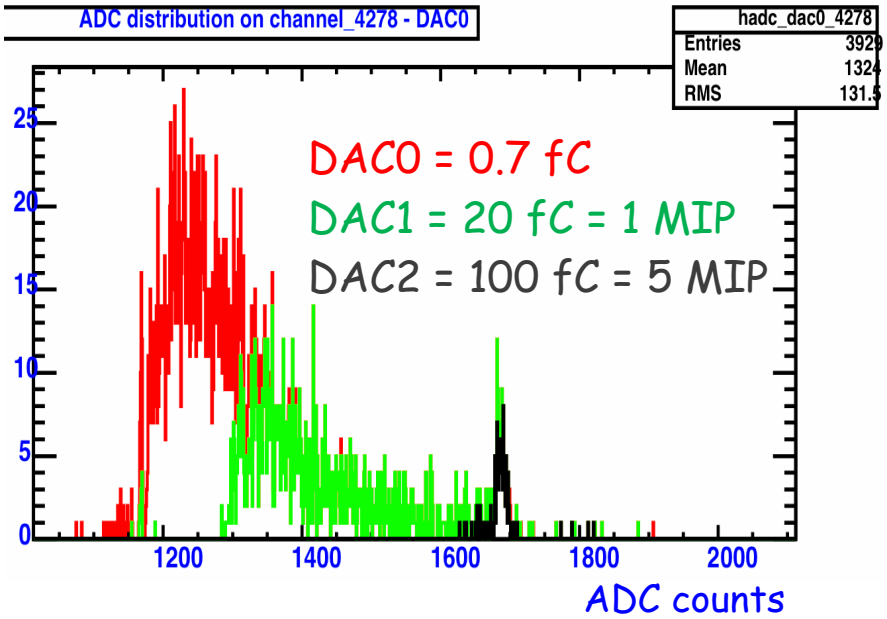


3.7. Preliminary results – Analog RO

- Analog readout
  - Hold of shaper signal (hold time can be varied)
  - Conversion by ADC on DIF board
  - Works with digital readout
- Landau distribution measured on one pad
  - Narrow pion beam (1x3 cm^2) was used
  - 3 thresholds set at ~0, 1 and 5 MIP respectively

3 distribution position agree with threshold settings
→ validate Microroc calibration

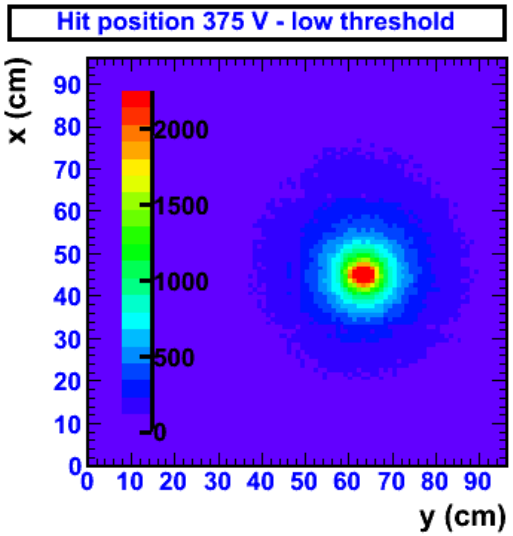


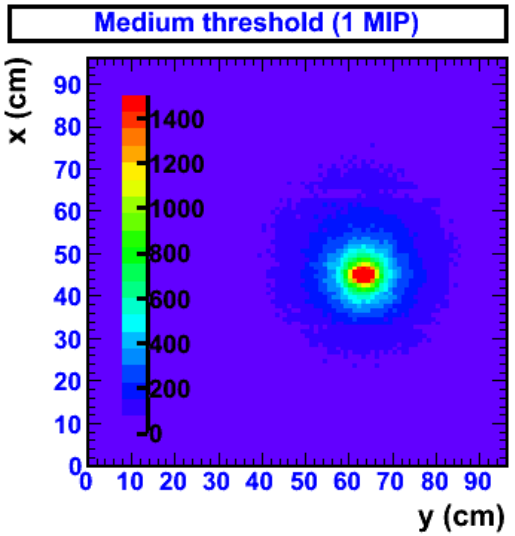


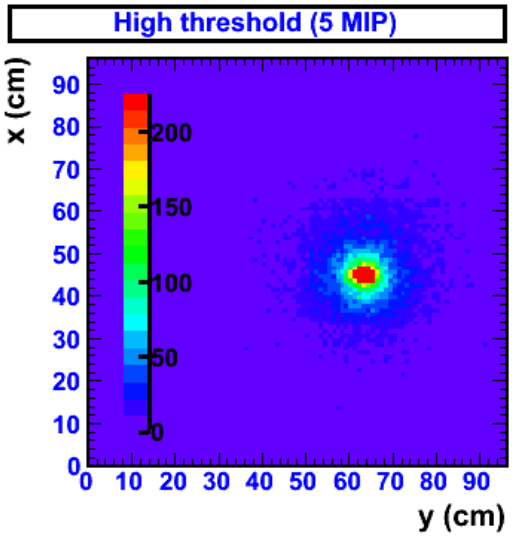
In DHCAL: Analog RO allows to fix and monitor the digital thresholds!

3.8. Preliminary results – Showers (I)

- 150 GeV/c pion shower signals with semi-digital RO at 375 V (50000 triggers)
  - 20 cm iron block placed 50 cm upstream the prototype
  - Only air between block and prototype
  - Medium and high thresholds set at 1 and 5 MIP
- Nicely axially symmetric profiles
  → Uniform response of the detector
- Particle density decreases away from the shower axis
  → Narrower profile obtained from medium and high thresholds





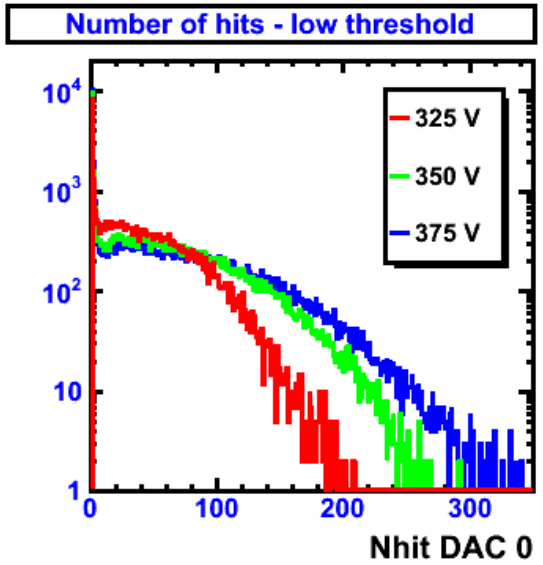


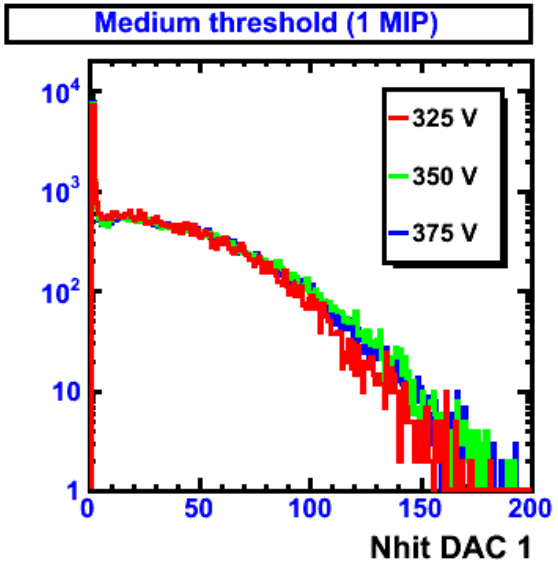
Looks like semi-digital RO of shower signal in Micromegas works!

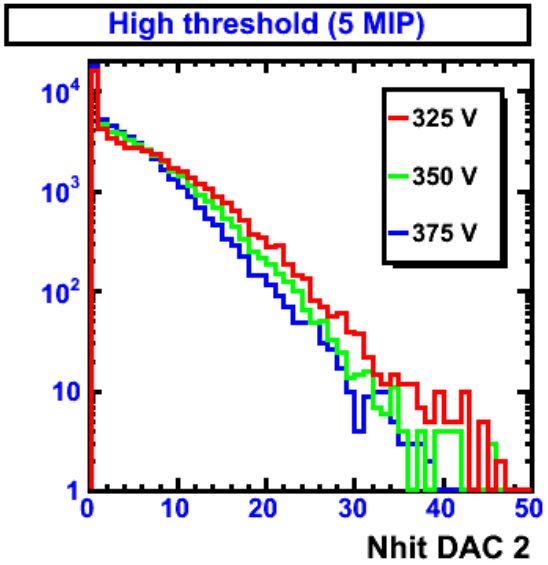
3.8. Preliminary results – Showers (II)

- 3 runs at mesh voltage of 325, 350 and 375 V
  - MPV charge increases with gas gain
  - Adjust medium and high threshold at 1 and 5 MPV

- Up to 300 hits at 375 V (efficiency > 95 %) !
- Distribution of low threshold changes according to the detector efficiency
- Distributions of medium and high threshold however super-impose!







Thresholds can be set for any given mesh voltage

Conclusion on test beam

- From preliminary results, the Microroc m^2 prototype seems to be an excellent detector
  - Efficiency of 98 %, multiplicity of 1.1 at 1 fC threshold
  - Uniform response
  - Almost no noisy channel (8/9216)
  - Noise under control (RAMFULL runs)
  - Semi-digital RO works (thresholds set at will)
  - Shaping 200 ns → signal of 1 µs
    → Max rate of 1 MHz/cm^2
  - Nearly no V_{mesh} trips. Very quiet detector
    At a gas gain of 3000 (390 V), there are very few sparks!
    To be further assessed inside W/Fe structures
    (PS: Rate is not relevant for ILC DHCAL)

Conclusion on project

- Micromegas 1 m^2 prototype
  - Bulk process with embedded chips: OK
  - Mechanics: OK
  - TB results: front-end OK
  - Sofar: performance compatible with HCAL requirements

- Future
  - Lot of data to analyse!
  - A second chamber has been constructed in October 2011
  - Construction of 1-3 planes in 2012
    - Including a resistive one (funds from ANR SPLAM)
  - Test beam 2012
    - 2 weeks RD51 for comparison resistive/standard m2 prototypes
    - CALICE: join physics runs of complete HCAL (W or Fe)

Aknowledegments

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