UPDATE ON SRS FOR THE NEXT EXPERIMENT

PLANNING FOR THE FINAL NEXT-100 DETECTOR

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next

Outline

1. **Quick reminder: what's NEXT?**

2. **Current (NEXT1) DAQ**

3. **Scaling current DAQ to NEXT100 (final design)**

4. **Conclusions**

next

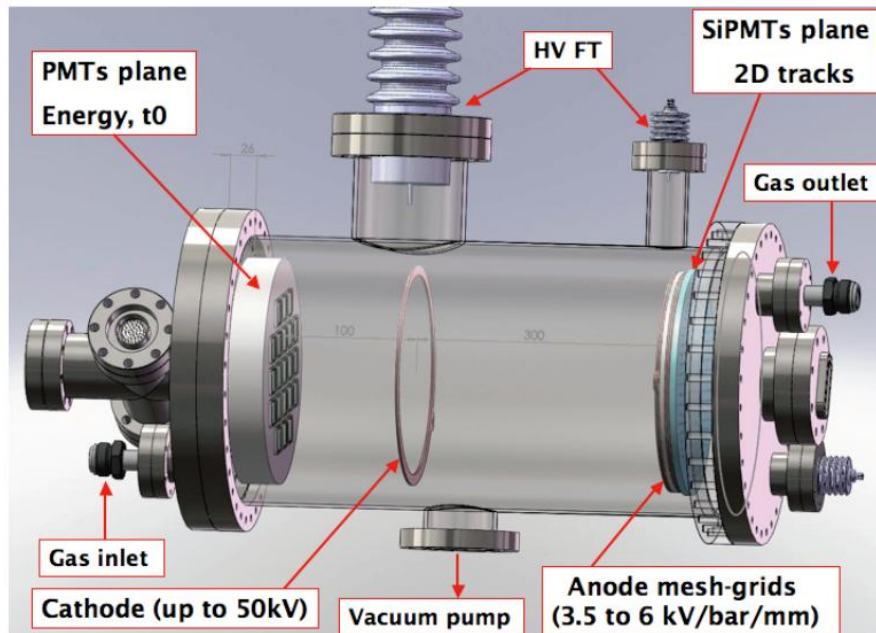# Quick reminder: what's NEXT?

A double-beta decay experiment based on a ^{136}Xe gas-filled TPC with two sensor planes: energy (PMTs) and tracking (SiPM)
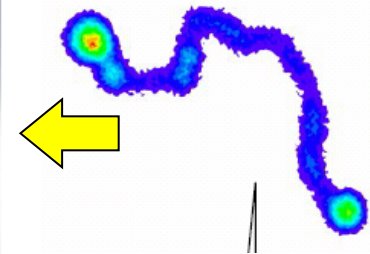
The NEXT-1 prototype (2011-2012)

- ## Non-radiopure, electroluminiscent TPC
  - Energy measured with a PMT plane behind the transparent cathode
  - t0 (primary scintillation) also measured with the same PMTs
  - Tracks reconstructed by a sensor array (such as SiPMs) behind the transparent grids of the anode
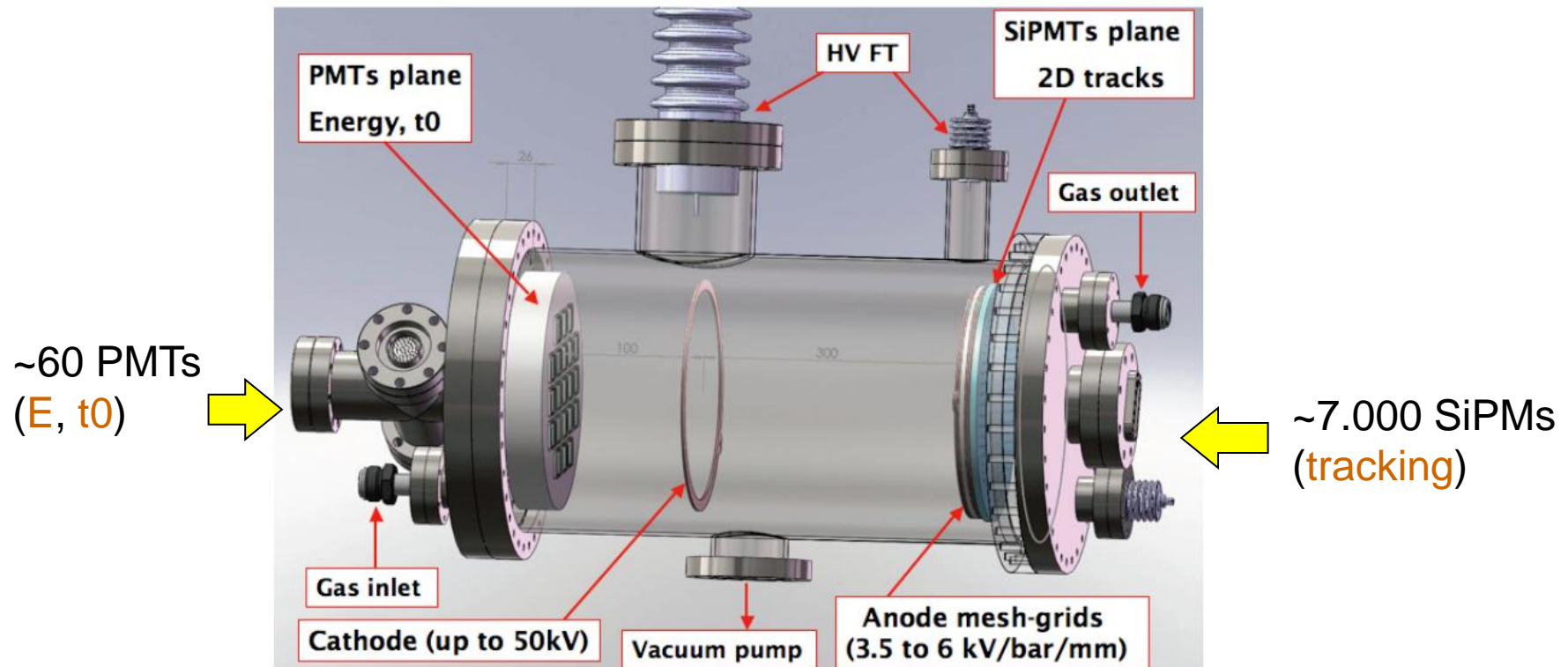

19 PMT ch
(E, t0)

248 SiPMs (tracking)

PMTs plane
Energy, t0

HV FT

SiPMTs plane
2D tracks

Gas outlet

Gas inlet

Cathode (up to 50kV)

Vacuum pump

Anode mesh-grids
(3.5 to 6 kV/bar/mm)

The NEXT-100 detector (2013)

- Full scale detector (approx. 1,2 m diameter and 2,x m long)
  - 100 kg ^{136}Xe
  - **~7-10k tracking channels**
  - **~100 PMTs**

~60 PMTs
(E, t0)

~7.000 SiPMs
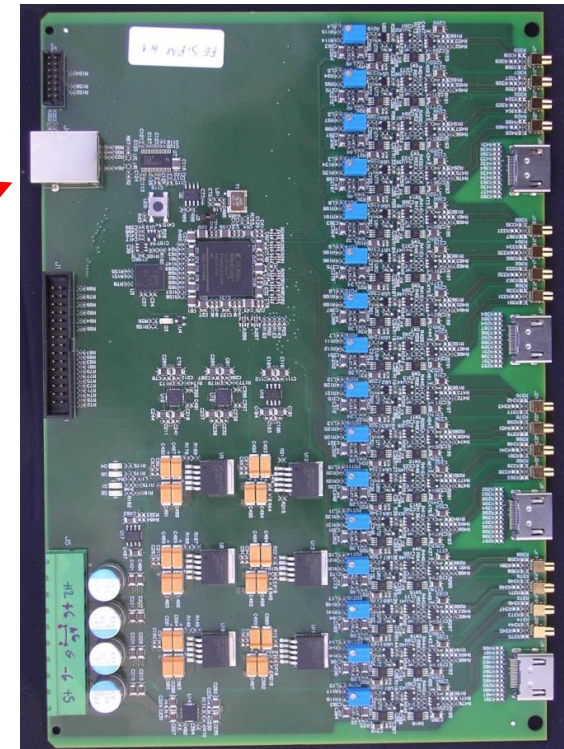(tracking)

Current (NEXT1) DAQ

Based on FEC modules, CERN ADC adapter cards and NEXT LVDS adapter cards

Review: readout scheme for SiPMs

Raw readout mode with DDR2 memory: (1) stores 128 ch/FEC, 819 us data in DDR2 buffer, (2) sends event fragment to DATE, (3) ready for a new trigger

NEXT/RD51 FEC card
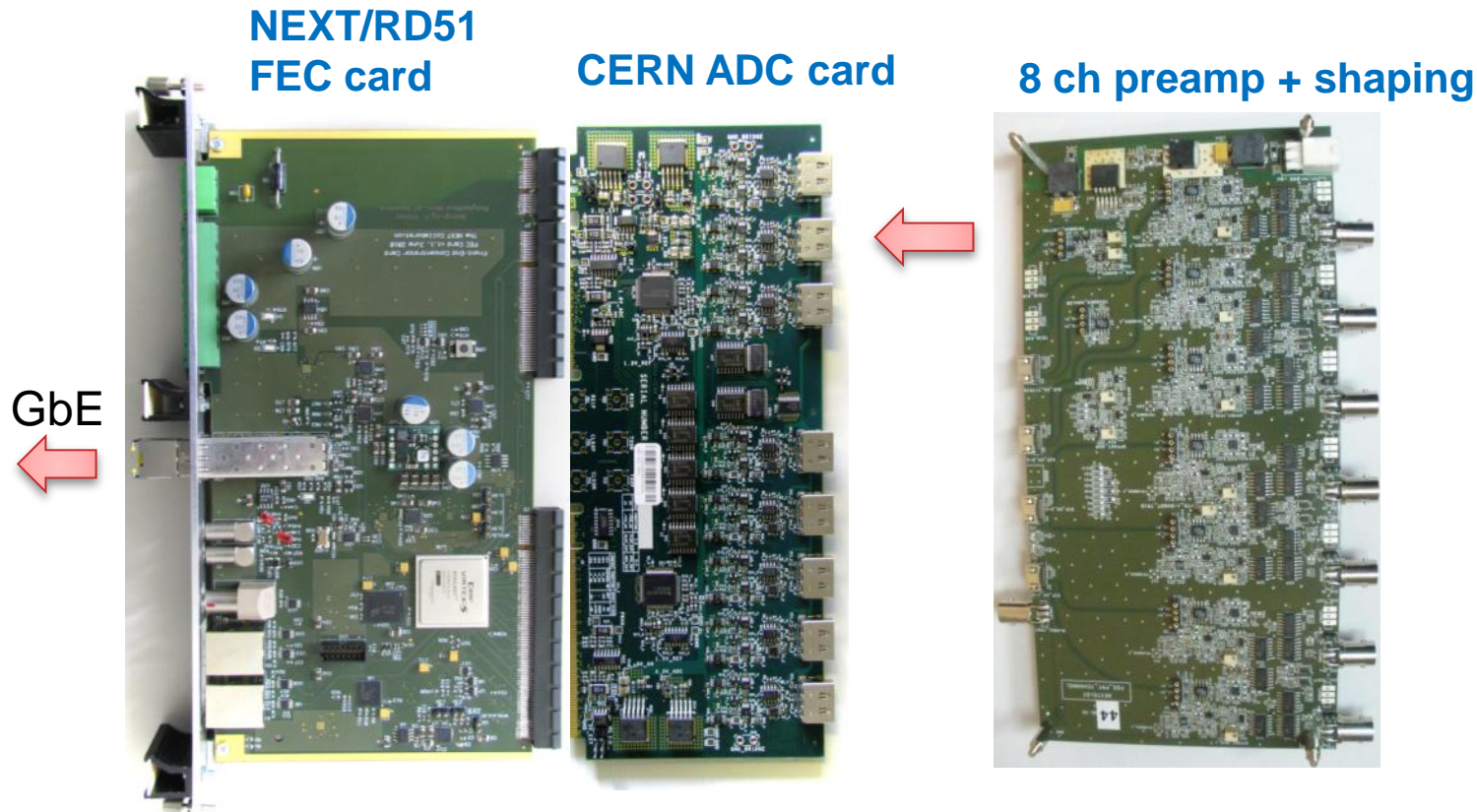
NEXT LVDS card

GbE

Clock + cmd/trigger + 2x data

16x (Amplifier + Integrator + digitizer + data formatter)
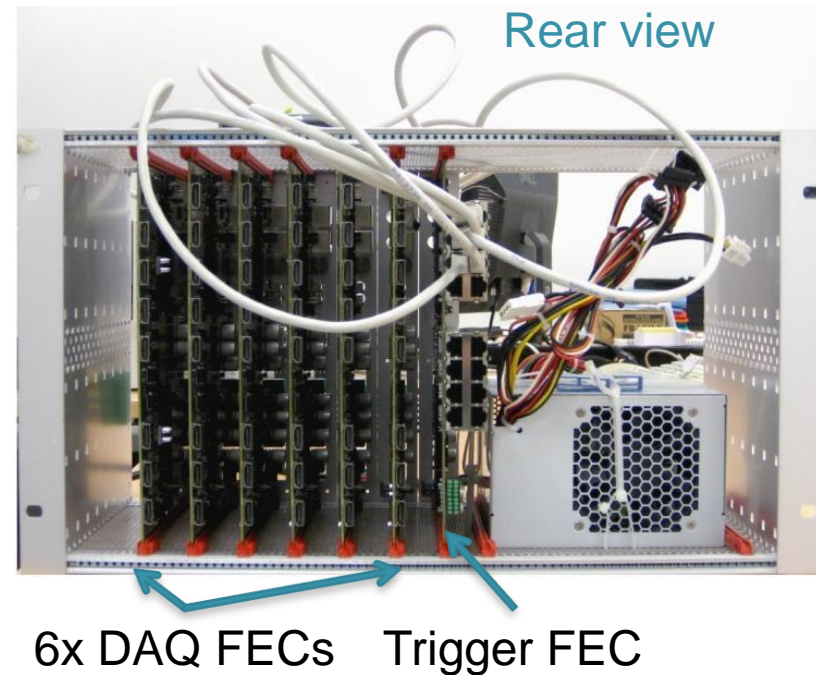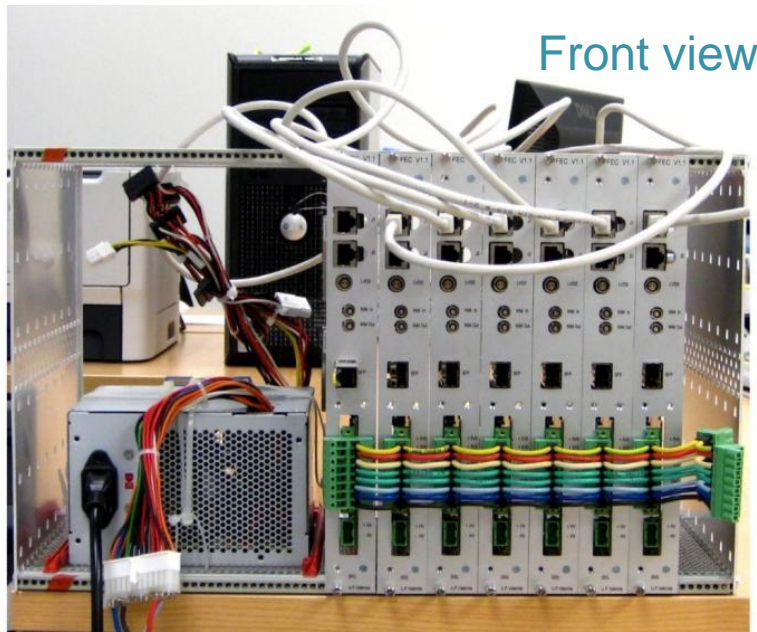
Review: readout scheme for PMTs

Raw readout mode with DDR2 memory: (1) stores 8 ch/FEC, 819 us data in DDR2 buffer, (2) sends event fragment to DATE, (3) ready for a new trigger

NEXT/RD51 FEC card

CERN ADC card

8 ch preamp + shaping
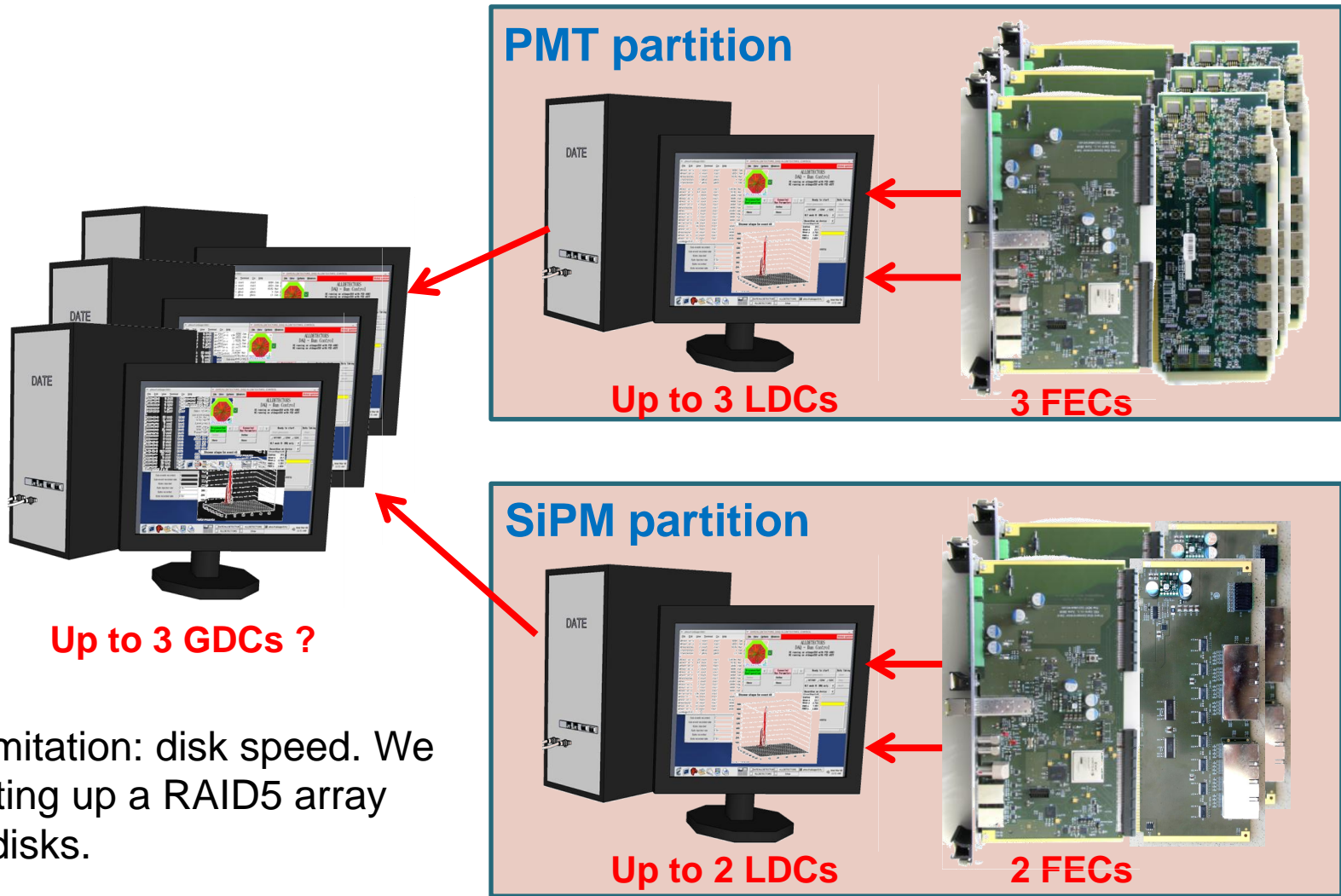
GbE

Review: Trigger in NEXT1

Clock, trigger and commands are sent from Trigger FEC to DAQ FECs

☐ **External trigger mode**

☐ **Internal trigger (single and sequence modes)**

☐ **Calibration mode trigger (with NIM out for sync)**

Front view

Rear view

6x DAQ FECs   Trigger FEC

NEXT1 DAQ architecture: DATE

PMT partition

Up to 3 LDCs   3 FECs

SiPM partition

Up to 2 LDCs   2 FECs

Up to 3 GDCs ?

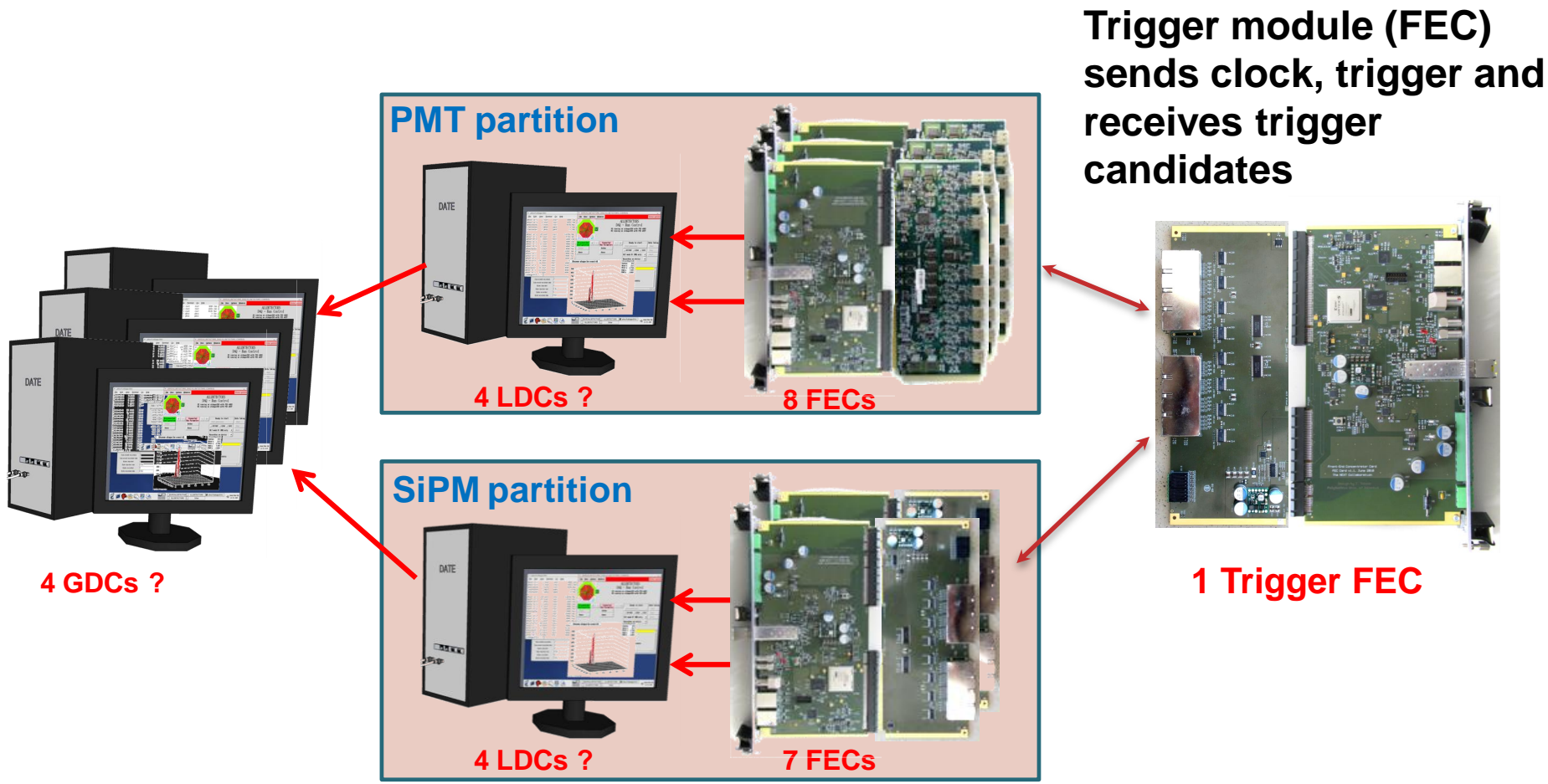GDC limitation: disk speed. We are setting up a RAID5 array with 4 disks.

Scaling current DAQ to NEXT100

Easy upgrade !

Easy scaling up to NEXT100 detector

❑ **~60 PMTs (energy plane) require 8 FECs+ADC adapter cards**

❑ **~6800 SiPMs produce 107 links (20 Mb/s average each, read out at 200 Mb/s) and require 107/16 = 7 FECs+LVDS adapter cards**

❑ **As far as we do not go beyond 16 FECs we ca use a single trigger FEC. Otherwise, an SRU would make a great trigger unit !!**

NEXT100 DAQ & trigger architecture

Trigger module (FEC) sends clock, trigger and receives trigger candidates

PMT partition

4 LDCs ?

8 FECs

SiPM partition

4 LDCs ?

7 FECs

4 GDCs ?

1 Trigger FEC

Conclusions

Full NEXT1 DAQ to be operating in Jan. 2012

DAQ upgrade for NEXT-100 is straightforward, as it is still a small scale SRS setup