Timepix adapter for SRS

A readout system for the Timepix chip

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RD51 Mini week, November 23rd , CERN

Titel

- Timepix chip

- Readout system
  - Current setup (MUROS)
  - New setup (Xilinx Evaluation Board based)
  - Status
  - Outlook (SRS based)

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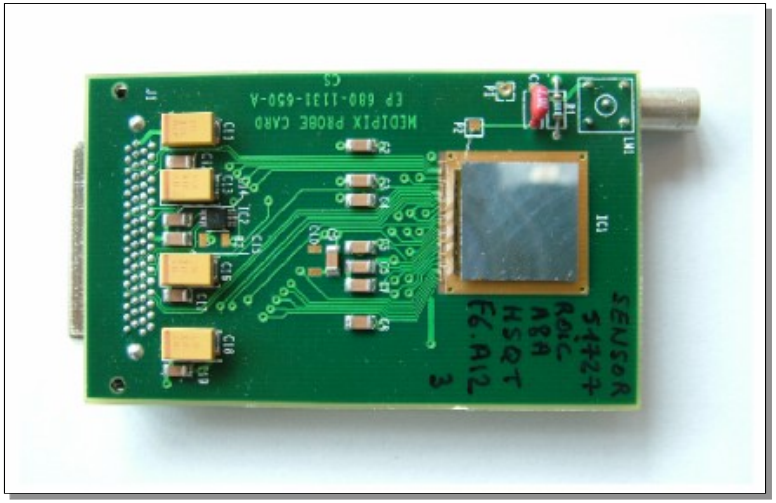
Timepix chip

- Readout chip: The Timepix chip



- Properties
  - 1,4 x 1,4 cm² active surface
  - 256 x 256 pixel matrix
  - CMOS 250 nm technology, IBM
  - 55 x 55 µm² per pixel
  - amplifier/shaper (t_{rise} ~150 ns)
  - 14 bits count clock cycles
    → Pixel pit when/how long
  - clock up to 100 MHz in every pixel
  - lower threshold
  - noise level ~ 500 e-

- Used as readout anode plane in gaseous detectors

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Timepix chip

- 4 different modi to operate

– Medipix:

Pixel hit how often

– Time-over-threshold:

Pixel hit how long

→ proportional to charge

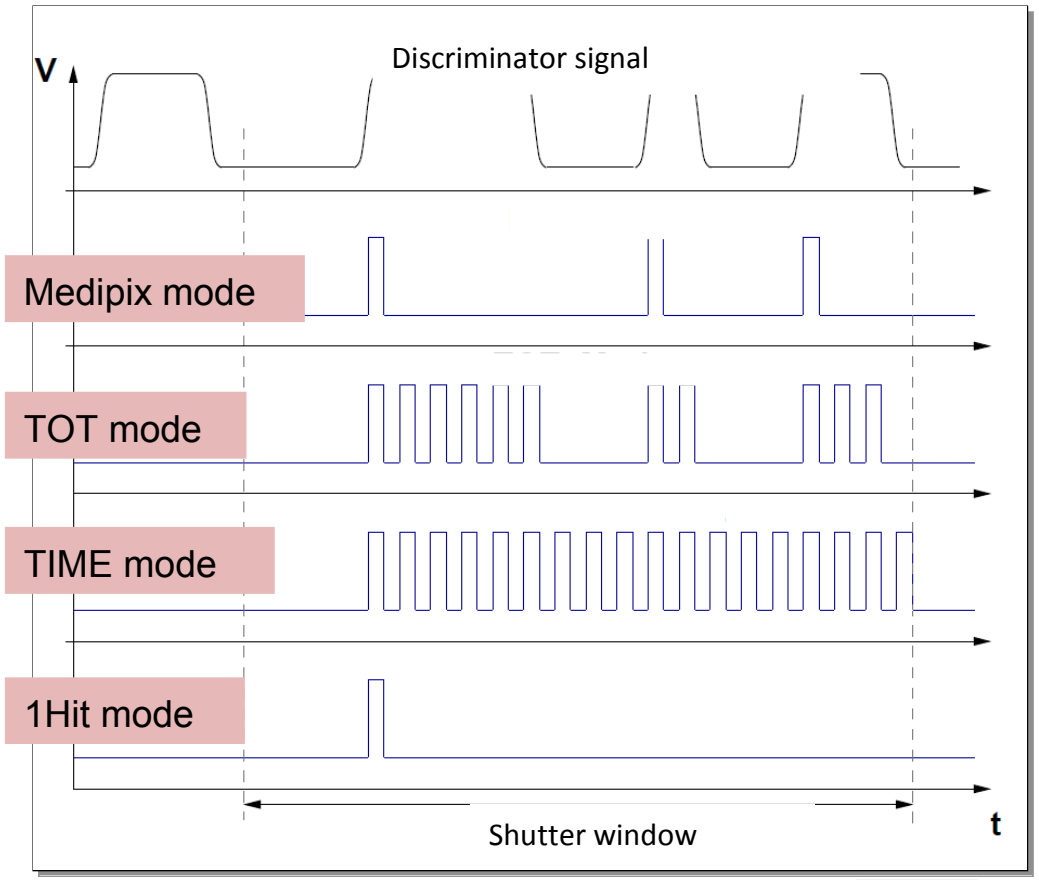
– Time:

Pixel hit when

→ time of arrival

– 1Hit:

Pixel hit in shutter window



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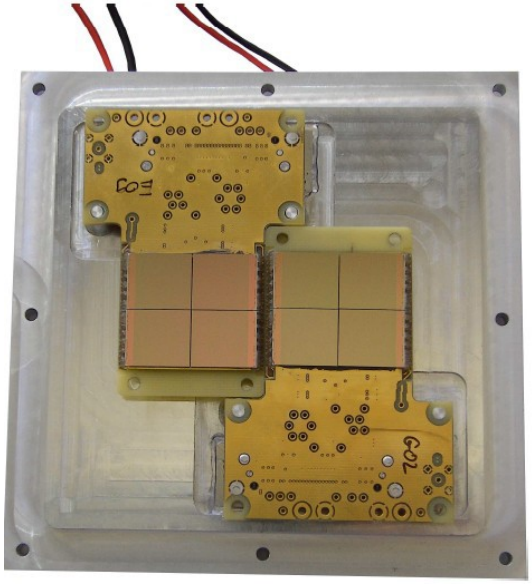
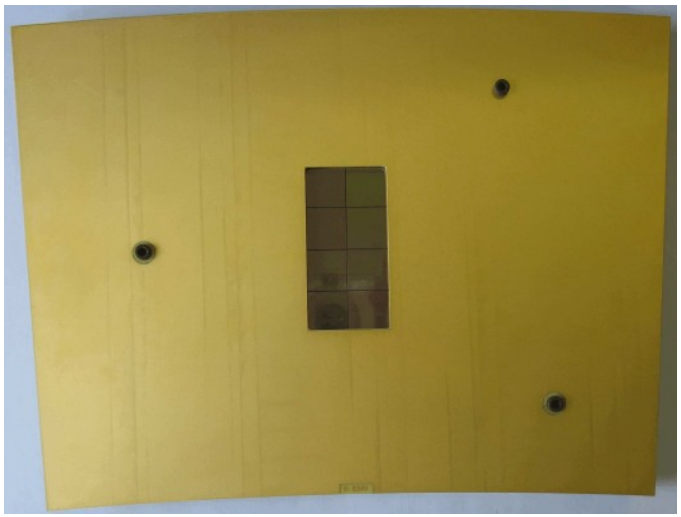
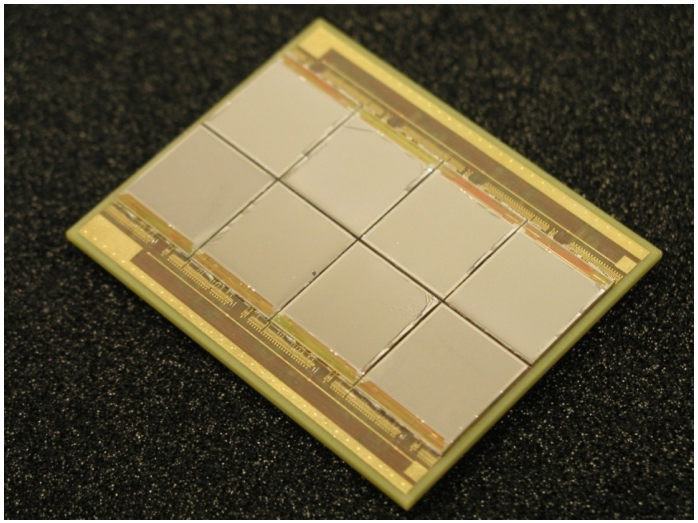
Pixellated endplate

- Until now: only few pixel chips for readout
- Bonn/NIKHEF: GEM + pixel
- CEA Saclay: Micromegas + pixel







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MUROS readout system

- MUROS v2.1:
  - successor of MUROS v1 (only Medipix1 chip)
  - designed at NIKHEF for Medipix2 and Timepix chip readout (new FPGA code)
  - serial readout for at most 8 Timepix chips
  - VHDCI cable <3 m to Timepix carrier board
  - VHDCI calbe to NI card in PC
  - Timepix readout: theo. < 50 frames/sec
    lowered by shutter lenght
  - adjustable readout frequency [<240MHz]
  - data acquisition on PC (Pixelman software)

http://www.nikhef.nl/pub/experiments/medipix/muros.html

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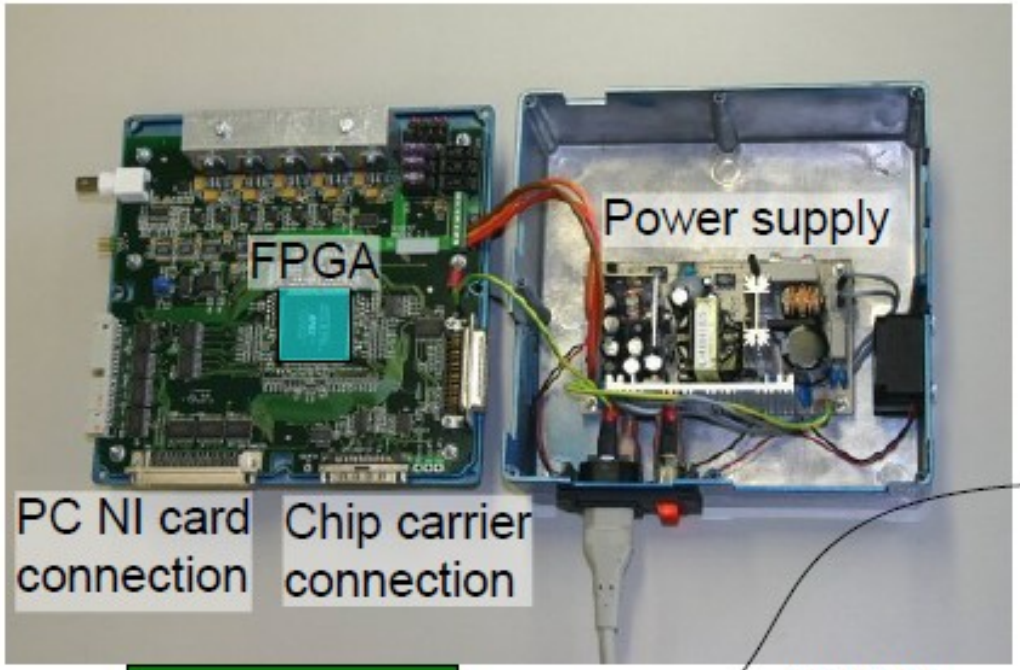
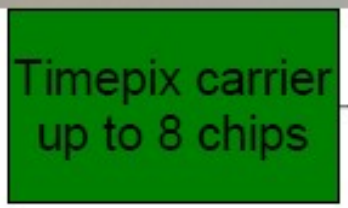
Readout status





VHDCI

MUROS 2.1

VHDCI

PC running Pixelman

NI card

- Problems with MUROS v2.1:
  - only limited availability, no production
  - NI card and driver out of date
  - read out at most 8 chips

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New readout system

- Goals:
  - ultimately read out ~100 chips
    → large area detector (e.g. full TPC endplate module)
  - modular system → use SRS (RD51)
  - ethernet based
  - use Virtex6 FPGA (will be used on next SRS FECs)
  - zero suppression
  - triggerable, integrate with slow control & calibration

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First steps

- Single chip readout (Uni Mainz)
  - Timepix chip on FR4 carrier
    - LVDS link
  - Adapter board
    - trigger
    - test pulses
    - power supply
  - Xilinx ML506 evaluation board (Virtex5)
    - Timepix control
    - ethernet (UDP) communication
  - PC software
    - command prompt based
    - Timepix control
    - data acquisition

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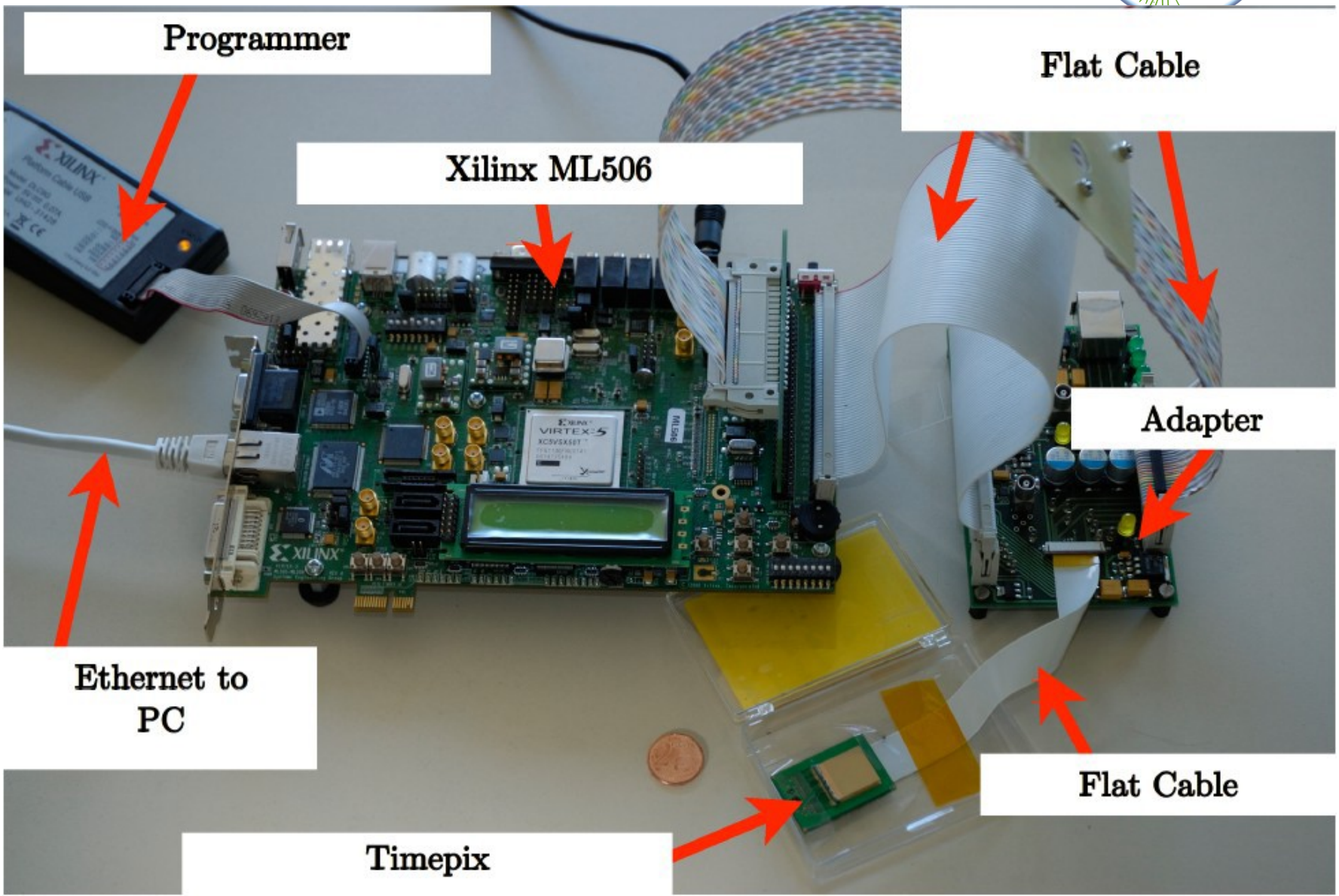
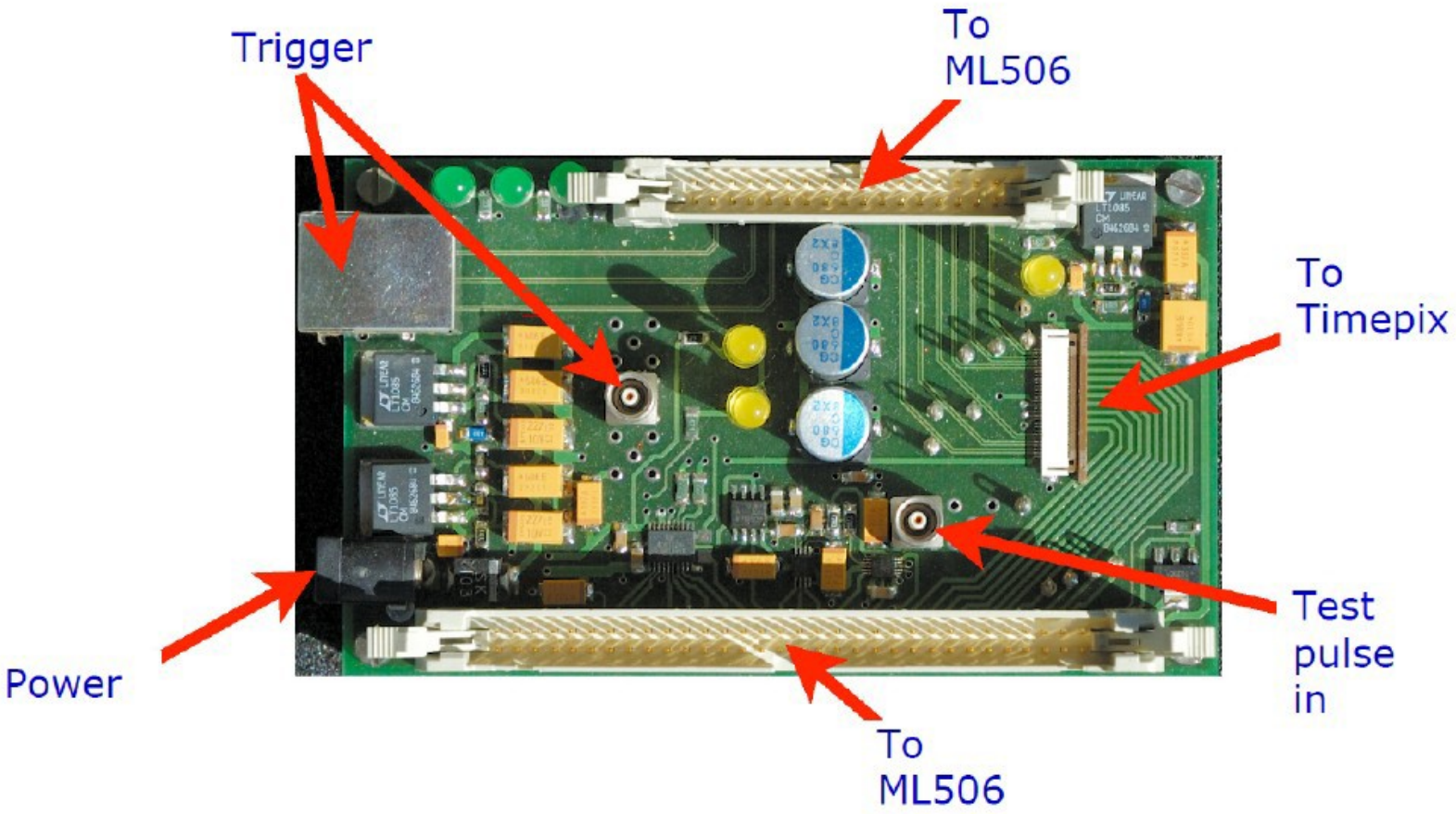
Mainz readout system



Adapter board for Xilinx kit



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FPGA

- On-chip Ethernet MAC (SGMII)
- On-board Gigabit Ethernet phy chip
  - 1000BASE-T
  - no embedded CPU
- Firmware
  - VHDL description
  - common clock for digitisation and data transfer, crystal based
  - serial/deserial interface to the Timepix bit-serial port
  - Timepix matrix data not buffered in FPGA
    → kept on Timepix while awaiting packet transmission
  - shutter with programmable delay and width
    - software control or
    - external trigger (TLU)
  - non-volatile storage of hardware description on CF card

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PC software

- C++ with Qt
- Command line interface, GUI will be developed (Mainz)
- Data pulled by computer (handshake)
- Minimal network protocol stack
  - ‹ethernet›‹IP›‹UPD›‹control›‹data›
  - standard ethernet/IP/UDP headers
- Functionality:
  - reset, setup (Timepix mode, matrix mask, DAC settings)
    shutter, readout, test pulse enable, choose trigger
  - start a run: set FSR, set matrix, readout matrix setup, DAQ
  - threshold adjustment under way

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Our activities so far:

- Setup of second Mainz system in Bonn
  - Xilinx ML506 board with Virtex5 FPGA + adapter board
  - single Timepix readout
- Re-target to Virtex6
  - Xilinx ML605 board with Virtex6 FPGA
  - firmware modifications to Virtex5 VHDL
    - new ethernet MAC, different clock and pin setup
    - implement Timepix control modules
  - hardware modifications
    - new adapter board for cabling
- Implement new features: at the moment: zero suppression

  → readout up to 4096 hits per frame with ≈85 Hz @ 100 MHz
- Sample data with Timepix outclock (Clock domain crossing)
- Ongoing: Implement second hit store BRAM on FPGA

  (record and transmit at same time)

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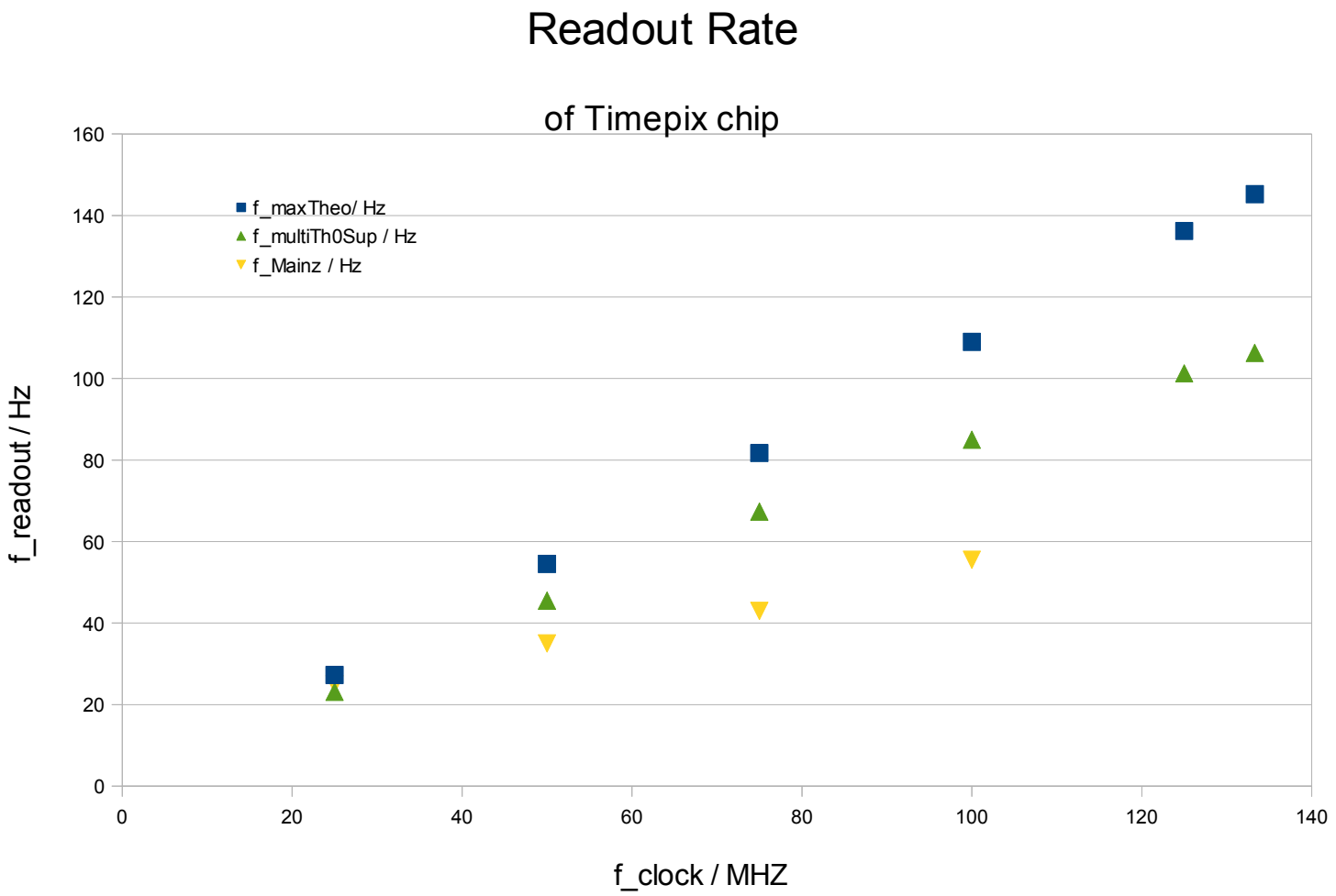
Readout rate improvement



Read out 4096 hits (maximum set in zero suppression) per frame, improvement on PC software (mulithreading of read and write).

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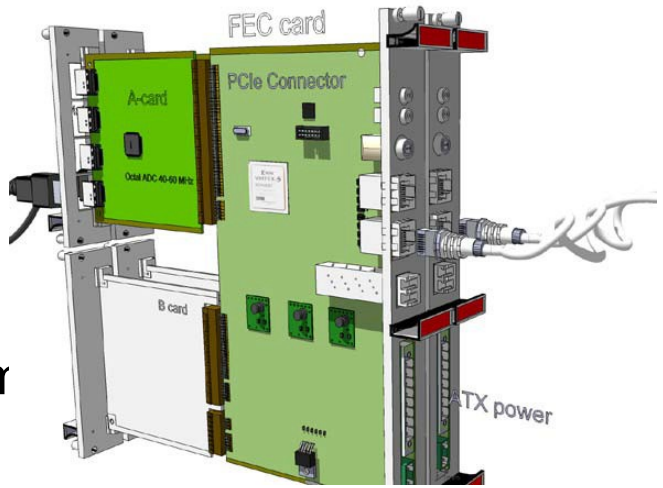
Our way to go

- Advancement of PC software (Full functionality as in Pixelman)
- Single chip readout with SRS → new adapter card designed
- Mechanics of box to house Readout card, including all connectors, supplies, switches and LEDs (Saclay)
- Modular system: Scalable Readout System SRS:
  - small set of modular components
  - performance at low cost
  - designed for scalability
    (e.g. 1 FEC for 8 chips x
    14 FEC/crate = 112 chips)
  - plugin-choice of frontend ASICs
  - open developer platform for physics algorithm
  - supported software made for physics
  - Developed at CERN for RD51



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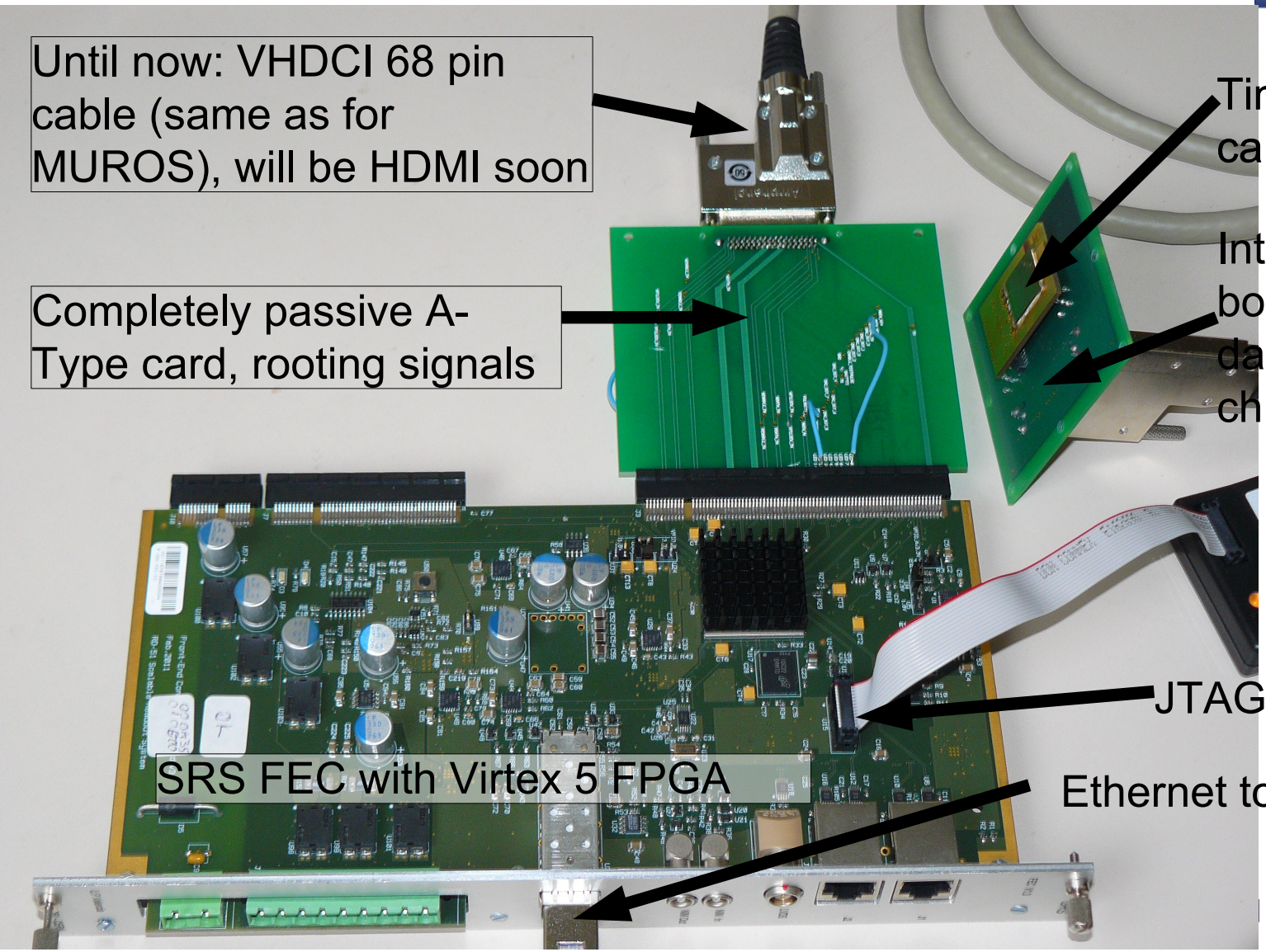
SRS with Timepix chip



Status of SRS + Timepix

- System set up for the first time last week on Monday
  - Error on A-Card detected, but could be solved
  - SRS uses different Ethernet compared to Xilinx Evaluation board:

    SRS: SFP ⟷ Xilinx board: SGMII
  - Connection to PC could not be established yet
  - Timepix operating FPGA firmware works on SRS (LEDs show correct behaviour)
- Todo: Get the ethernet working!

- Order SRS Crate at CERN shop

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Summery

Timepix chip (single, quad, octo) is used as readout structure in gaseous detector (prototypes)

- Current readout system (MUROS2) can handle up to 8 chips
- Largest area covered: 2.8 x 5.6 cm²
- New readout system under development
  - single chip readout realised on Virtex5 and 6 board
  - FPGA zero suppression almost realised
  - Hardware (chip carrier, Intermediate board, A-Card) for SRS ready
  - Migration of FPGA firmware to SRS ongoing
  - a scalable readout system to handle ~100 chips is aimed for
  - Readout for large area gaseous detector

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Motivation

Advanced European Infrastructures for Detectors at Accelerators
- 4 year EU FP 7 Research Infrastructures program project
- Started February 2011
- > 80 institutes from 23 European countries
- Budget: 27 million € (8 million € from the EU)
- Coordinated by CERN

Subtask 9.2.3 (Bonn, CEA, Mainz, NIKHEF):
Common readout systems for gaseous detectors. Auxiliary electronics for the read-out of pixellated front-end chips, aimed at highly granular pixel read-out of gas detectors, are to be developed.

→ New readout system for pixellated chip (Timepix chip)
→ Cover large area for TPC/inner tracker application

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People in AIDA Subtask 9.2.3

- Bonn:
  - Klaus Desch (Professor)
  - Jochen Kaminsky (PostDoc), new chip carrier, adapter card (SRS)
  - Michael Lupberger (PhD), FPGA firmware on Virtex6/SRS
- CEA:
  - Paul Colas (group leader)
  - Technicians at CEA, supporting hardware for chip carier
- Mainz:
  - Uli Schäfer (Dr.)
  - Christian Kahra in some time as PhD (?), PC software
  - Michael Zamrowski (gone), 1st version of FPGA on Virtex5
- NIKHEF
  -
- CERN: support from SRS group
  - Hans Müller (coordinater), Sorin, Jose (FEC design)

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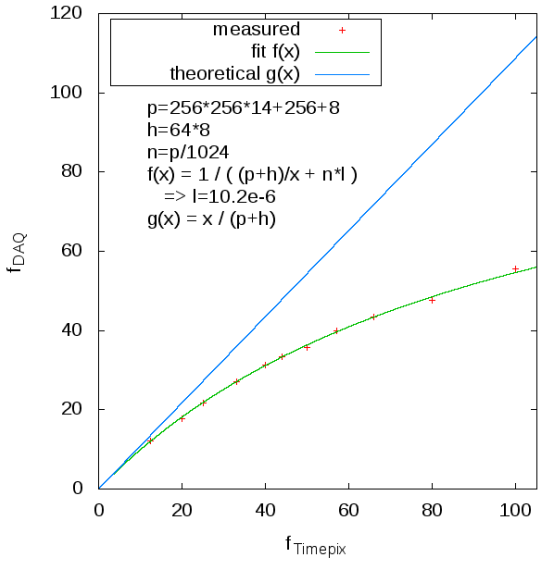
Tests and results

- Lab test in Mainz: Timepix readout
- Run with TPC in Bonn
  - event rate up to 55.5 Hz @ 100 MHz
  - improvement to MUROS2, but lower than expected
  - bare Timepix chip would be ≈ 100 Hz (using LVDS link)
  - data pipelined through FPGA, no noticeable latency, low packet overhead
  - bottleneck probably due to latency in Linux IP stack



$$\Rightarrow f_{\mathrm{DAQ}} = \left(n \cdot \left(\frac{\mathrm{payload} + \mathrm{header}}{f_{\mathrm{timepix}}} + \mathrm{latency} \right) \right)^{-1}$$

f_{timepix}: operating frequency (variable 12.5 - 100 MHz)

n: number of packets

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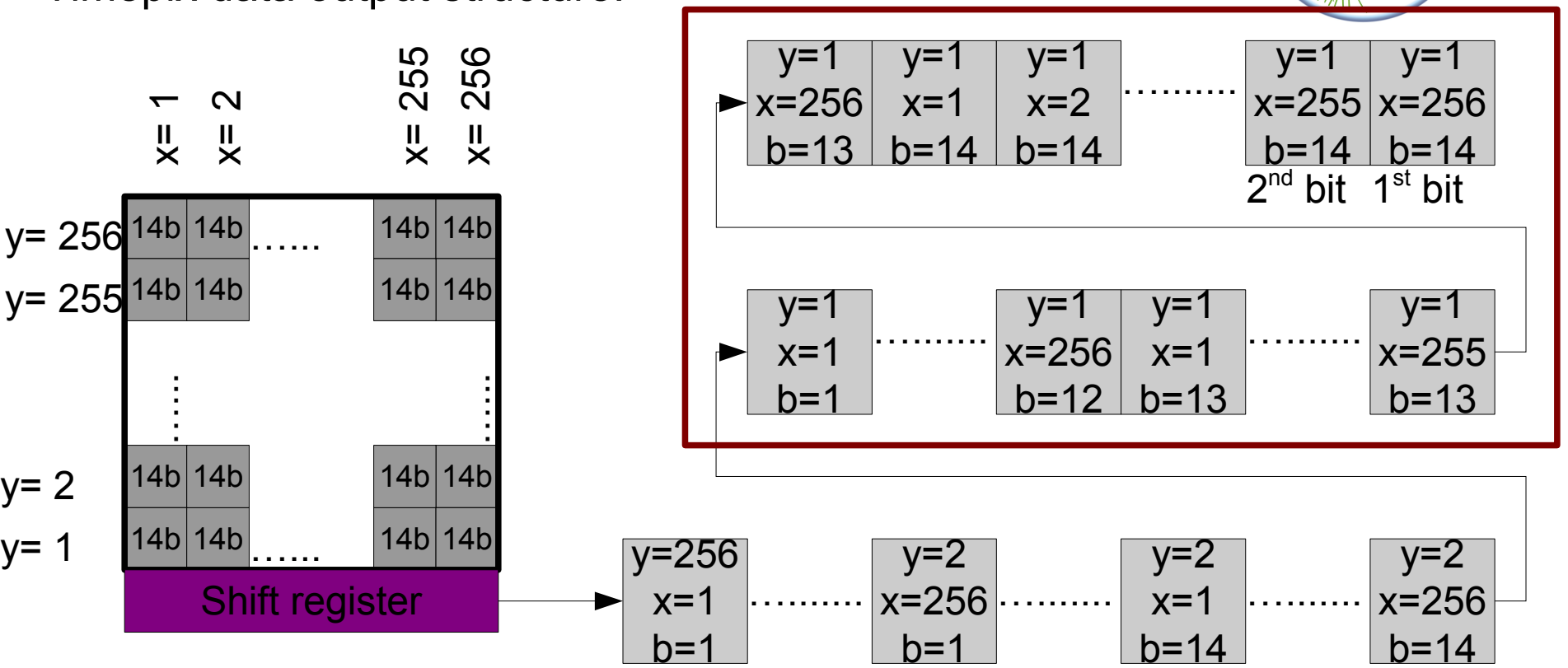
Current activities:

Timepix data output structure:



Each pixel: 14 bit pseudo random counter

→ zero suppression needs real counter value

→ need lookup table to convert to real value

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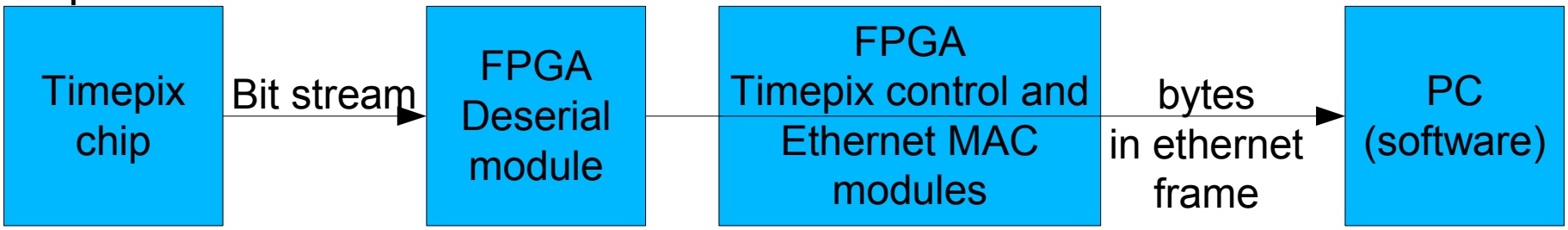
Current activities:

New readout procedure:

Aim: Zero suppression, lower data volume, higher readout rate

Old procedure:



Only pipeline data: Convert bit stream to bytes for ethernet

- PC software receives data from Chip (in byte packets)
- Sort data stream (x,y, bit position of counter of pixel(x,y))
- Get **pseudo random counter value** (x,y) and convert to **real counter value** using Lookup table
- Generate Matrix

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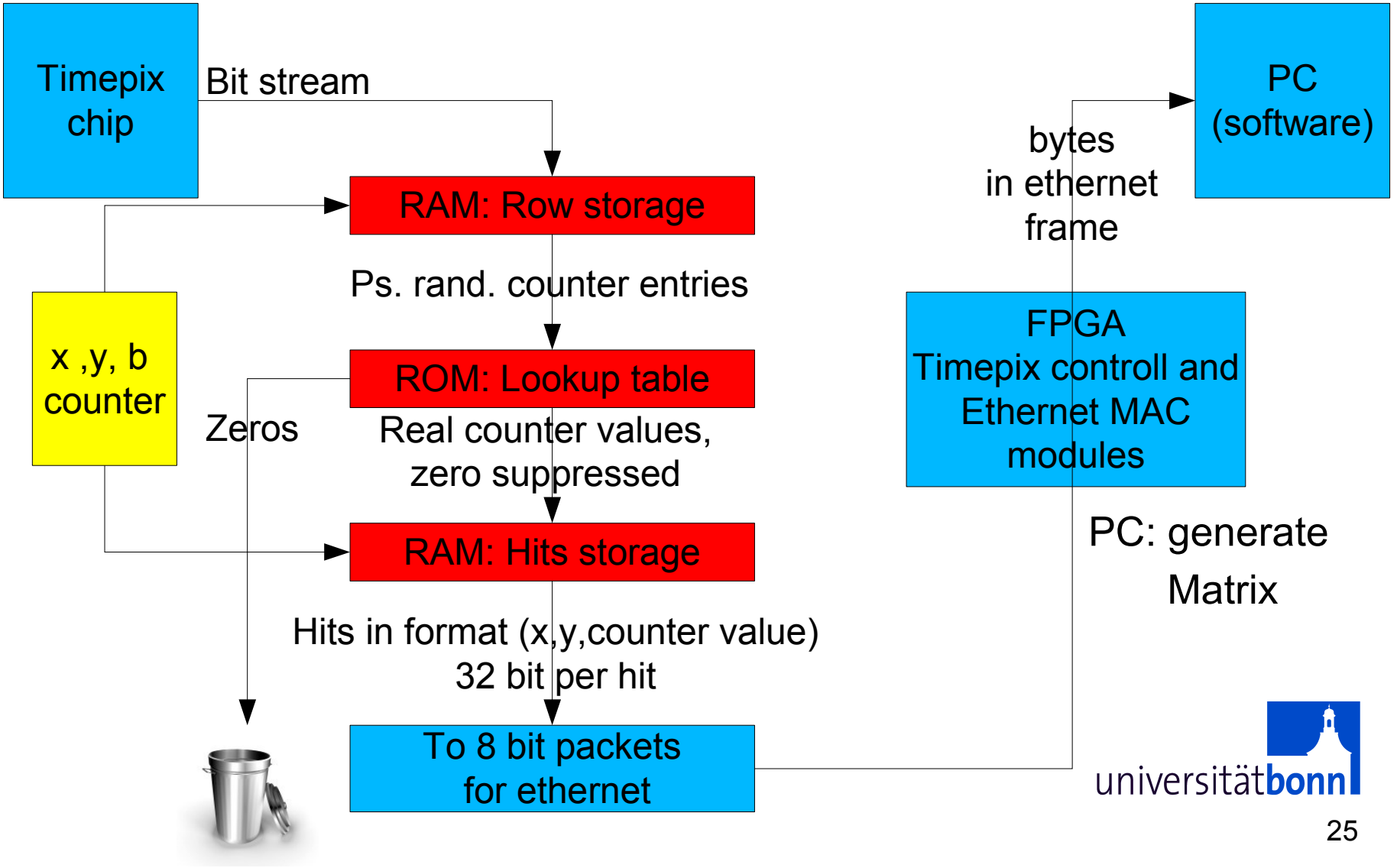
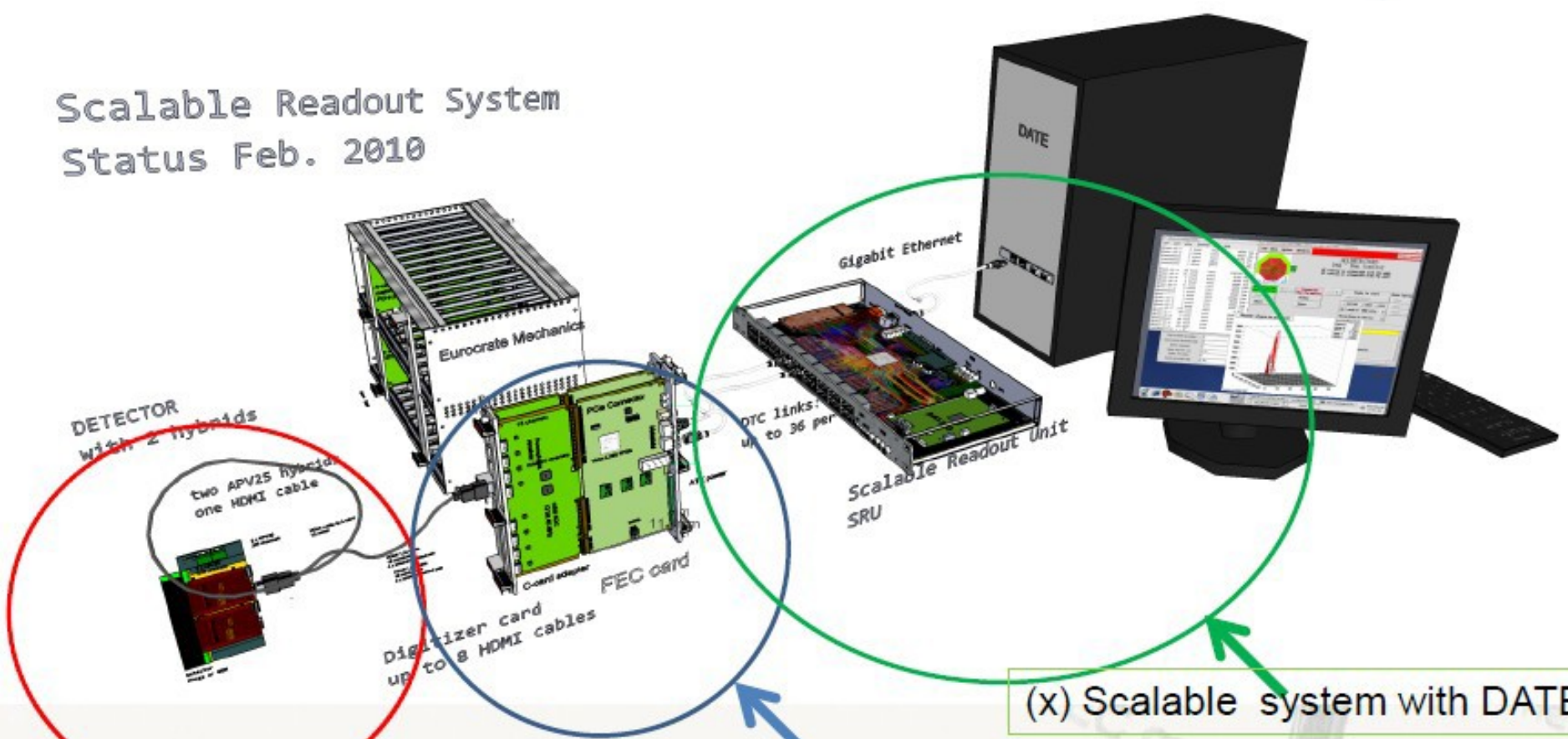
Current activities:

New procedure (additional):



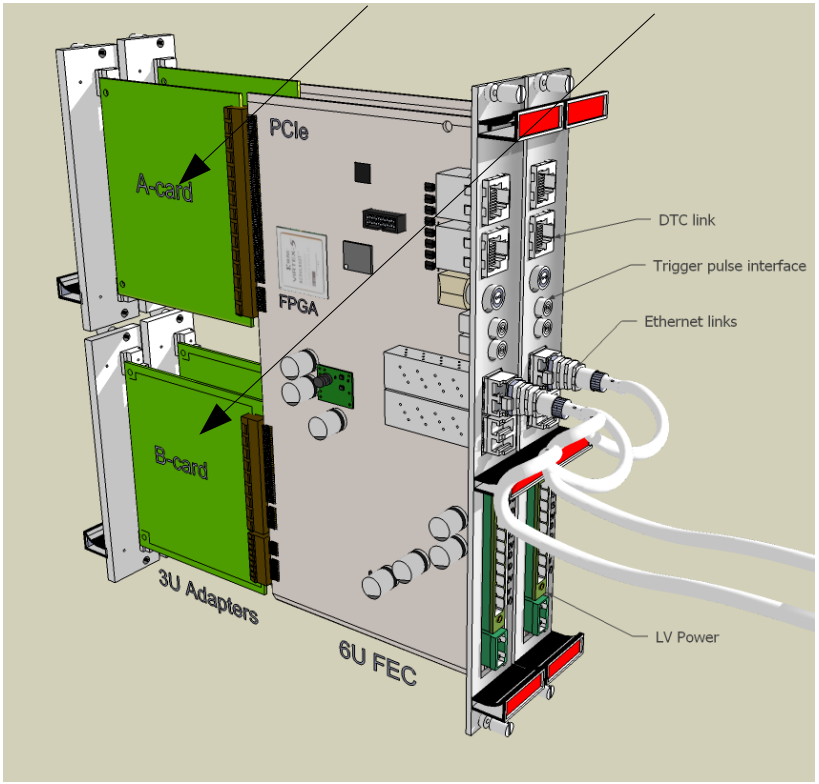
SRS physical overview



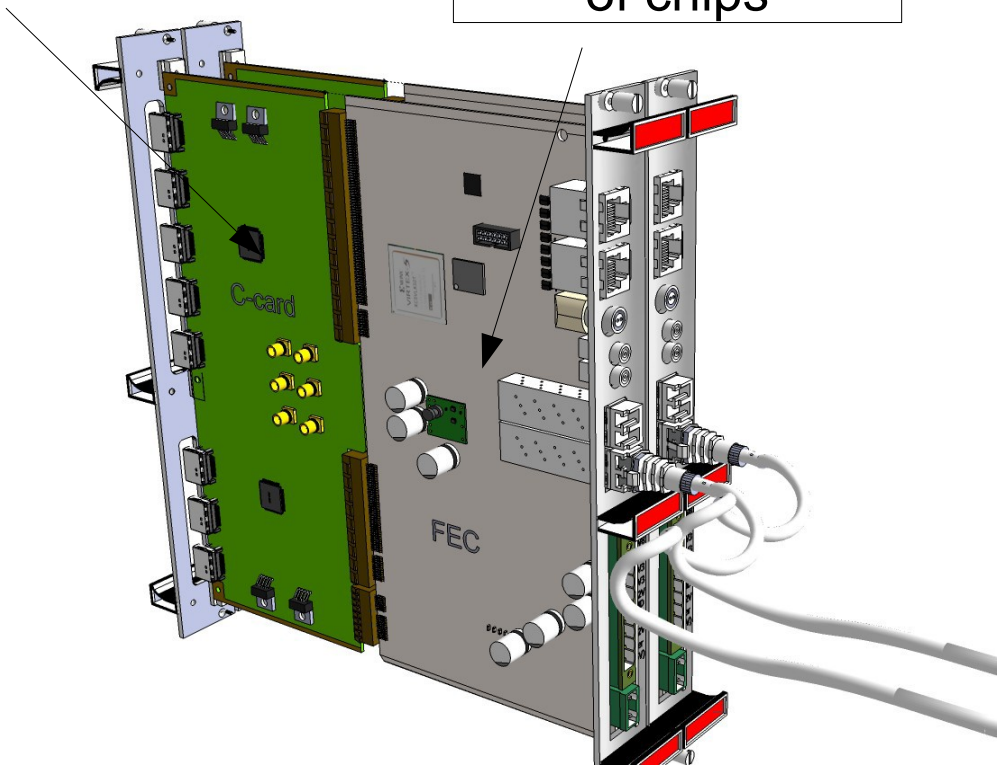
FEC and adapter cards

- A –Cards: 4 U (= 4 HDMI plugs)
- B –Cards: 4 U for miscellaneous extensions and LV-HV control
- C –Cards: 8 U

Adapter card
(Individual for each typ of chip)

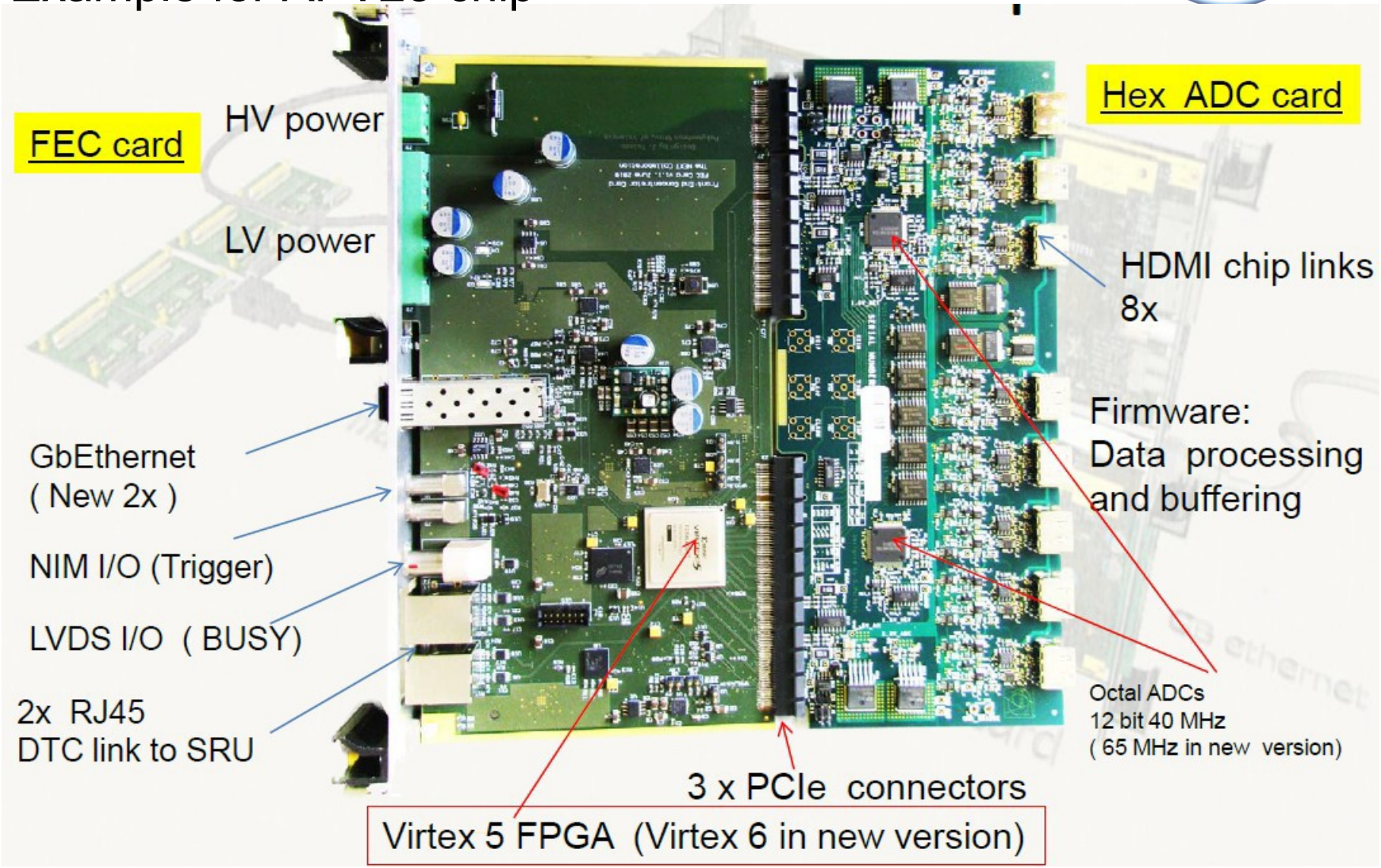


FEC
Common for all typ
of chips

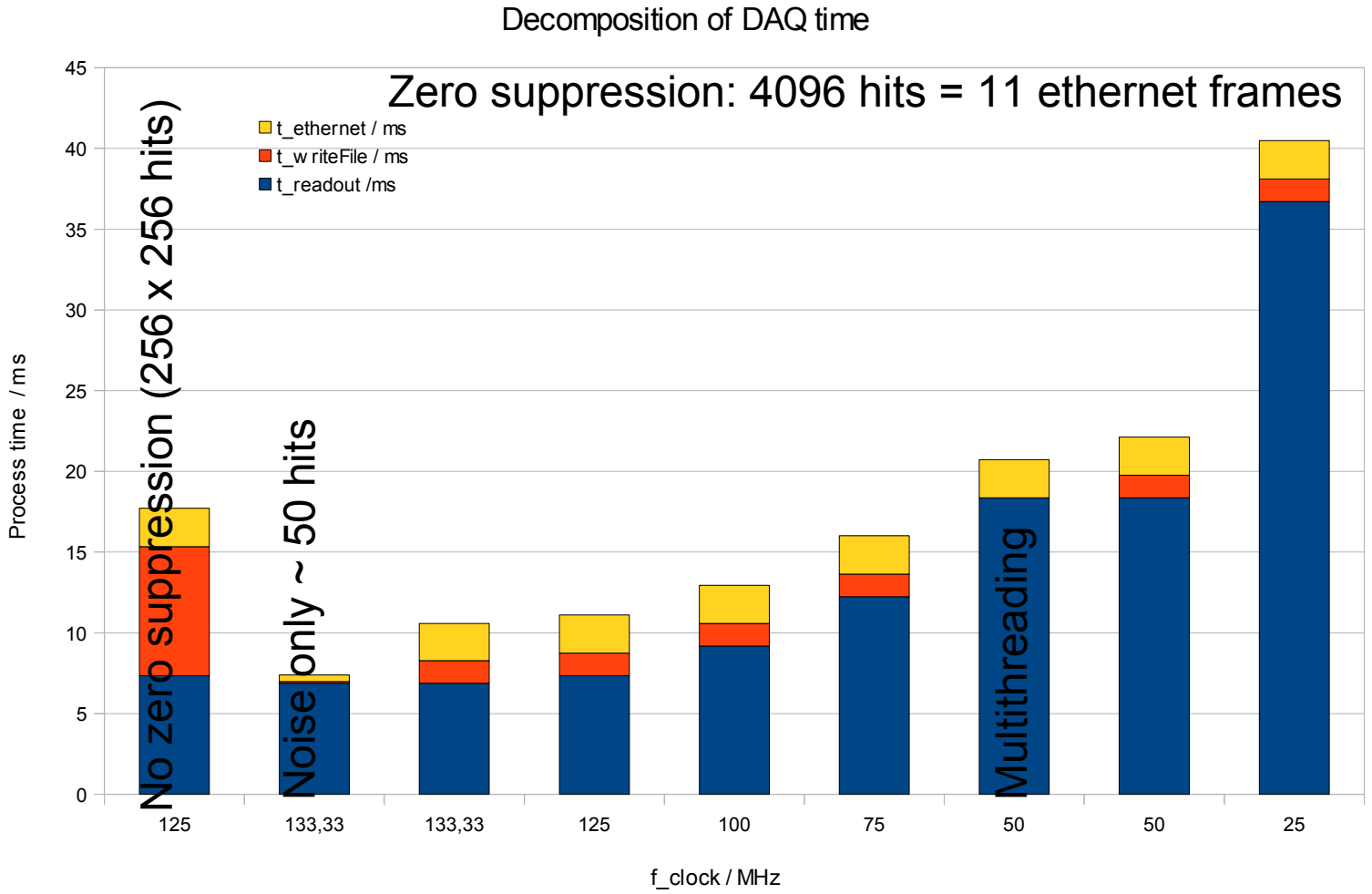


FEC and C-size ADC adapter

Example for APV25 chip



Readout time decomposition



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