MICROMEGAS Read-Out Chip and PCB: STATUS

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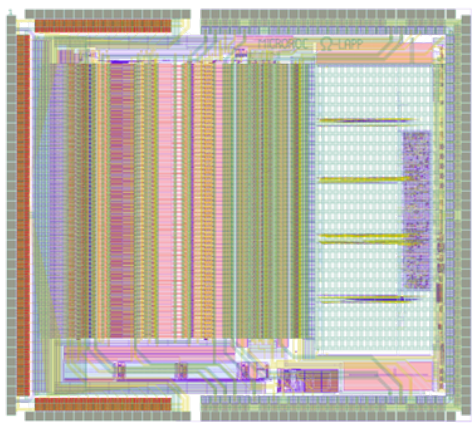
Introduction

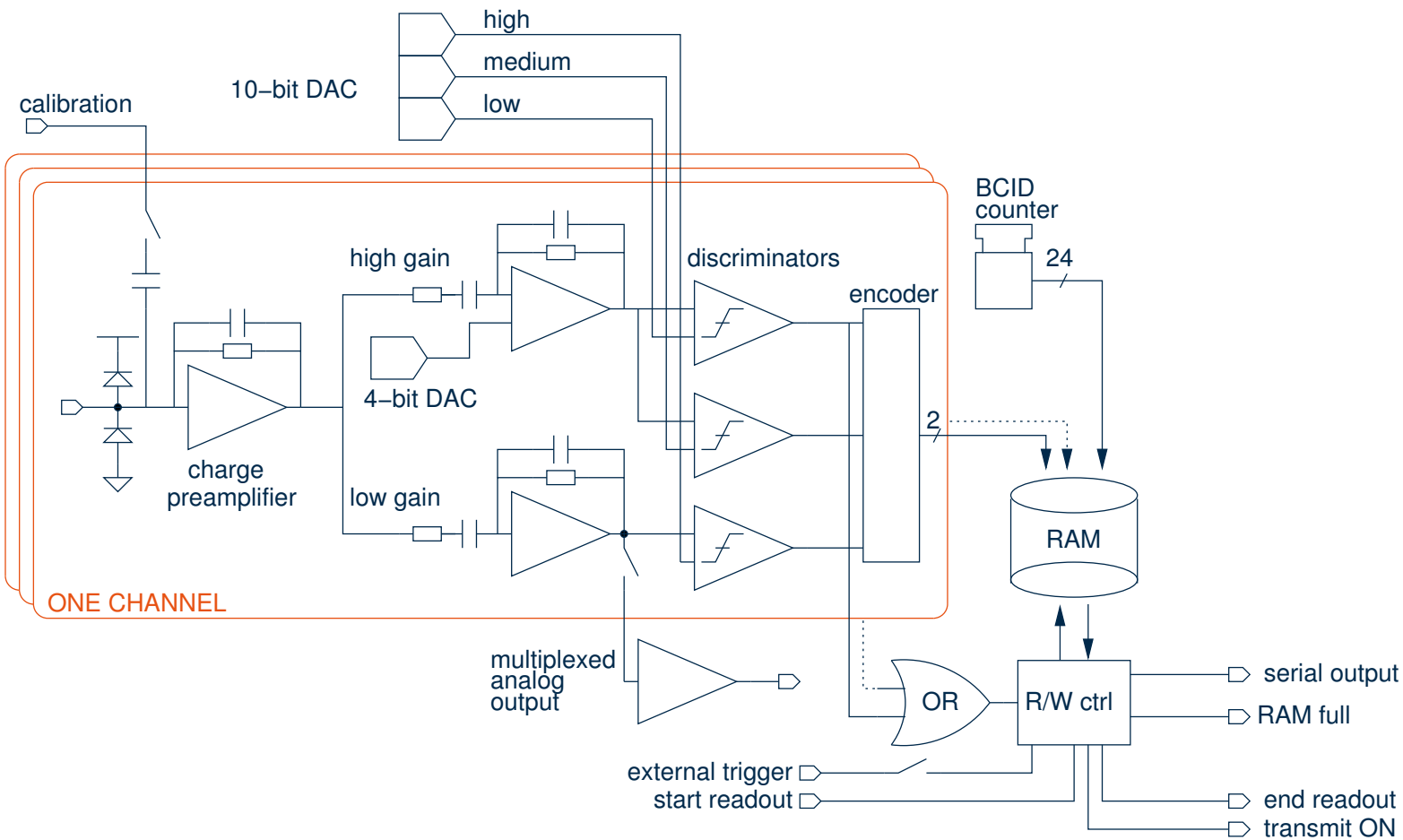
MICROROC is a 64 channels integrated circuit packaged in TQFP160 intended to be used with MPGD-based DHCAL (MICROMEGAS or GEM).

- MICROROC is a fruit of the collaboration between LAPP and LAL/OMEGA based on the experience of previous ASICs (DIRAC and HARDROC) and on multiple test beam results;
- Same Digital part as HARDROC2b, but charge preamplifier input stage + sparks protection [R. Gaglione] and slower shaping + 4-bit DAC offset correction per channel [N. Seguin]
- MICROROC is pin to pin compatible with the HARDROC2b to minimize board modifications.



Global architecture

Different path for low/medium and high thresholds + offset correction.

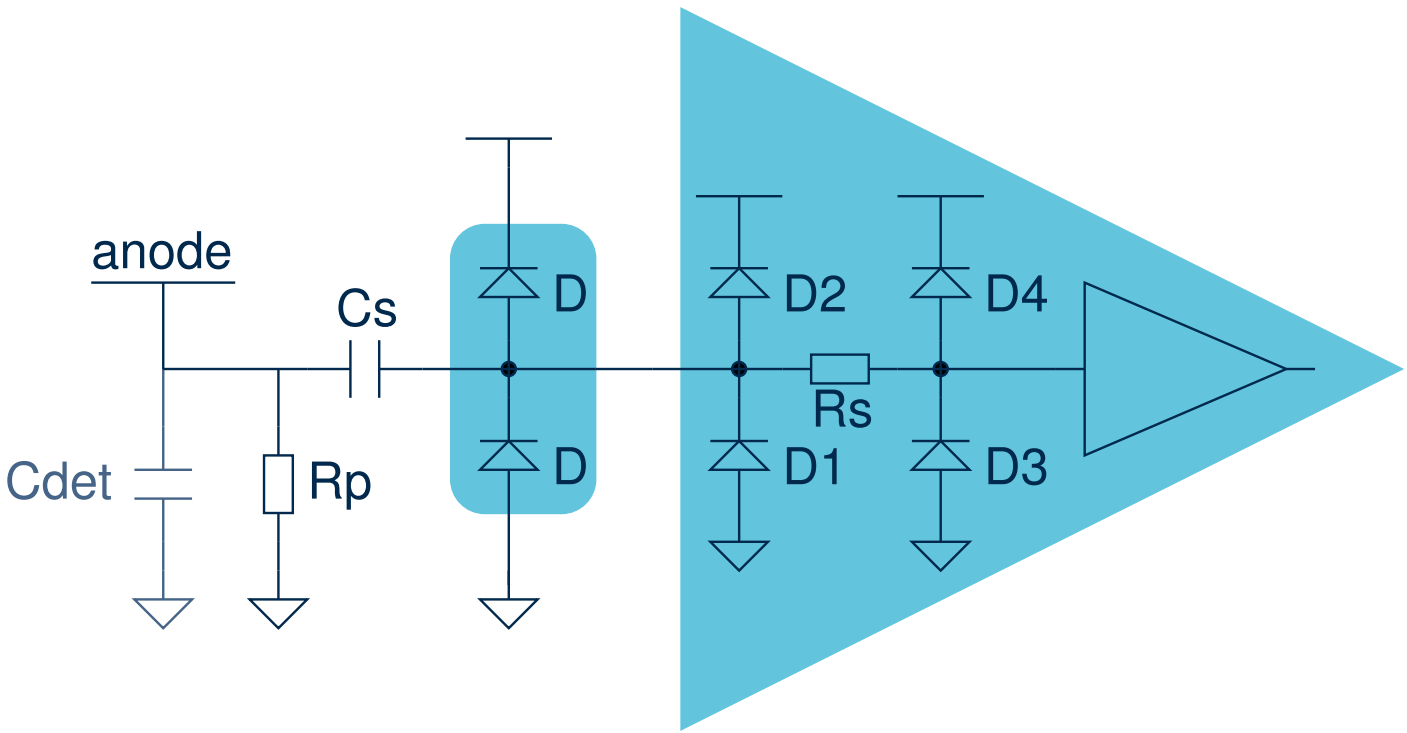


Main informations

- Technology: AustriaMicroSystem SiGe 0.35 µm
- Die size: 4.85×4.3 mm
- Dynamic range: 500 fC (200 fC for high gain path)
- Preamplifier gain: 2.38 mV/fC
- Noise rms: 1 fC at preamplifier output, 0.24 fC with 200 ns shaping (C_{det}=80 pF) (expected)
- Noise rms: 0.12 fC with 30 ns shaping (C_{det}=30 pF) (measured: see M. Chefdeville's talk)
- Peaking times: 30, 50, 100 and 200 ns
- Minimum threshold: ∼2 fC

Protection against sparks

New clamping diodes inside ASIC (see talk @ Freiburg): no dead channel so far... (but only 2 testbeam) !



Rp=1 MΩ, Rs=10 Ω, Cs=470 pF, D are ON-Semiconductor NUP 4114.

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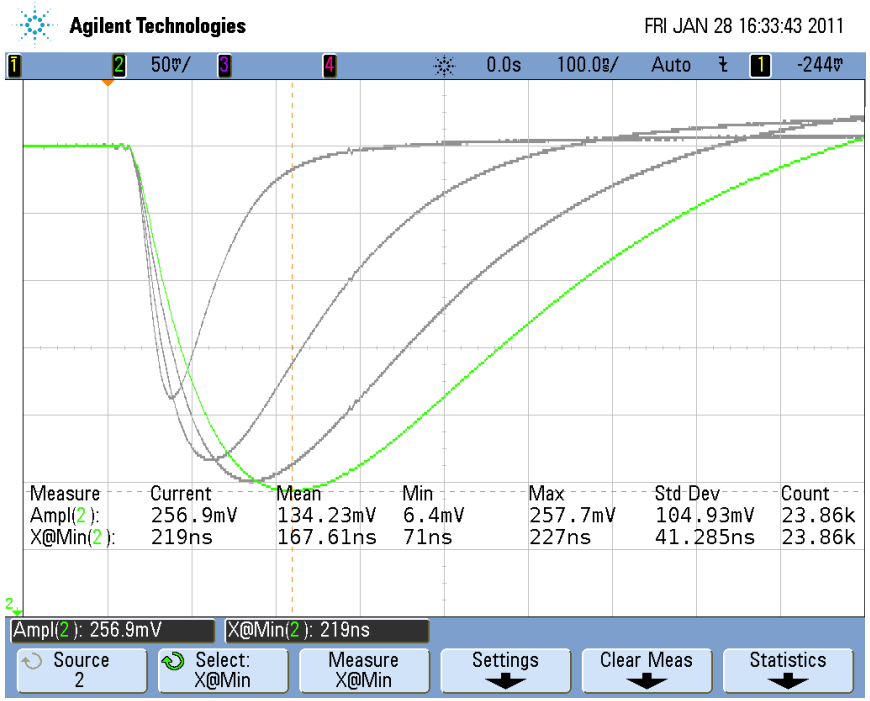
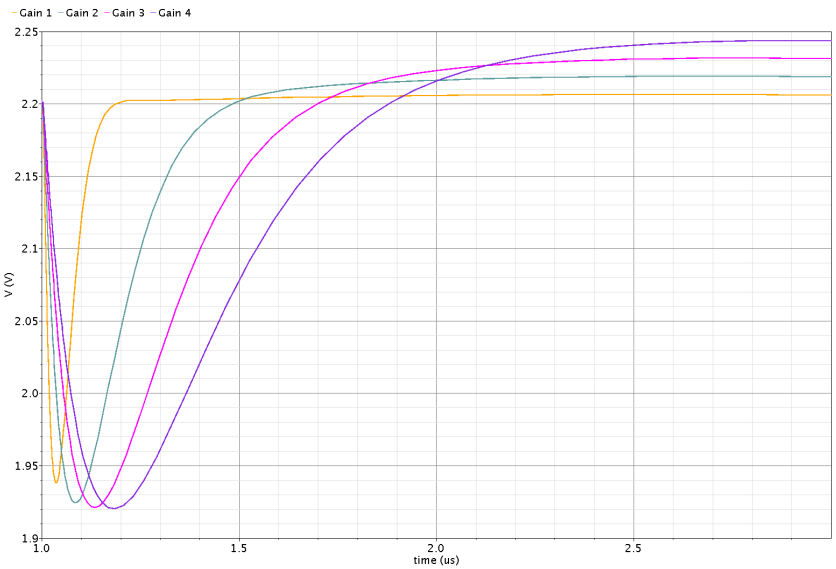
Waveforms

This is the output of high gain shaper, for the for settings (measure against simulation), with 25 fC charge injection (MIP-MPPV):

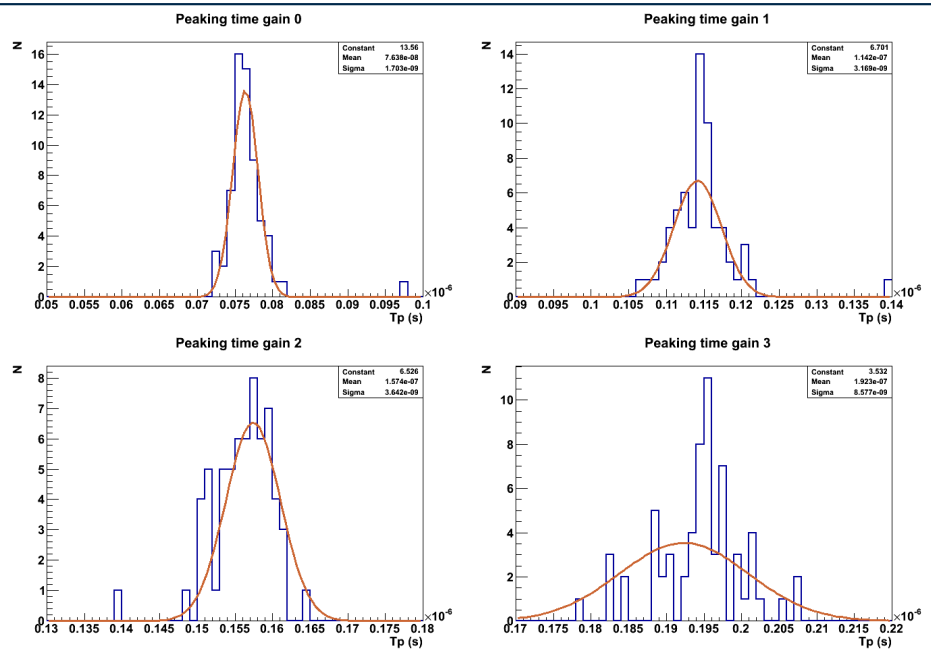




Good agreement between simulation and real behaviour.

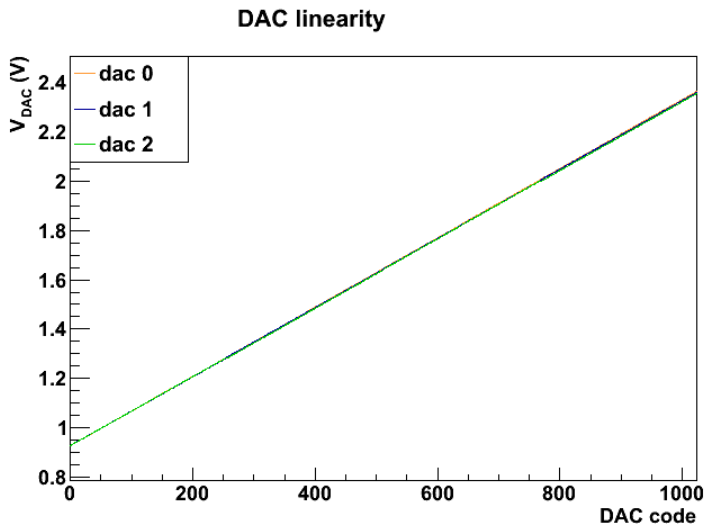
Shapers

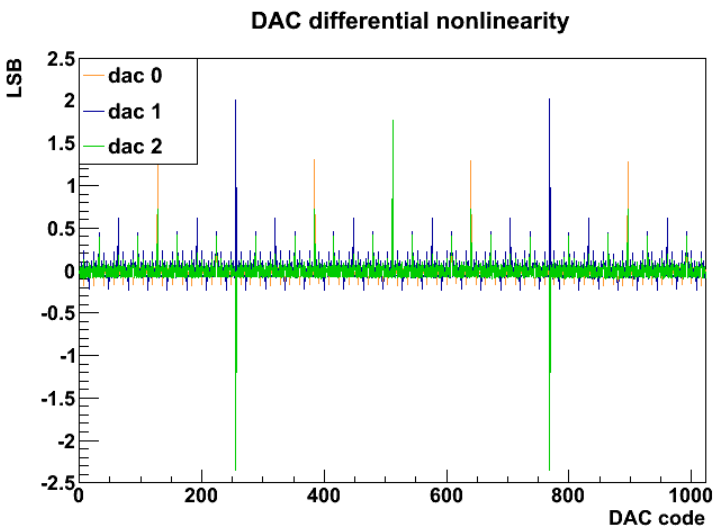
Setting	Measure Gain (mV/fC)	Measure Tp (ns)	Simulation Gain (mV/fC)	Simulation Tp (ns)
00	7.6	76.3	10.5	30
01	9.7	114.2	11.0	100
10	9.8	157.4	11.1	150
11	10.2	192.3	11.2	200

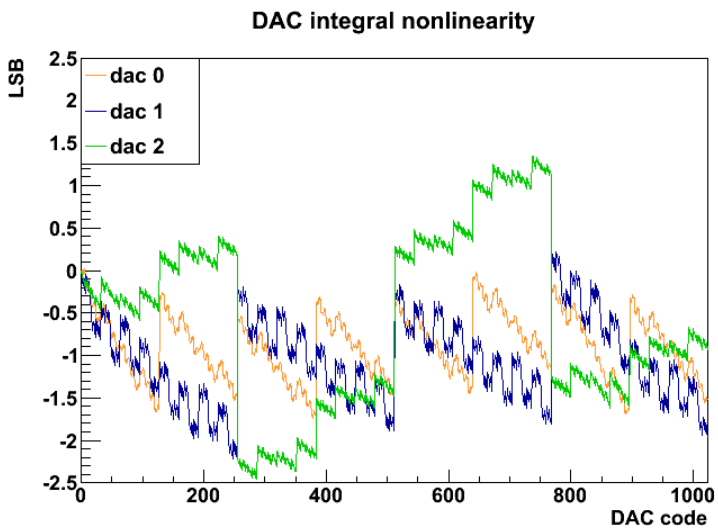


Good agreement between simulation and real behaviour, excepted for fastest shaping

Thresholds DAC

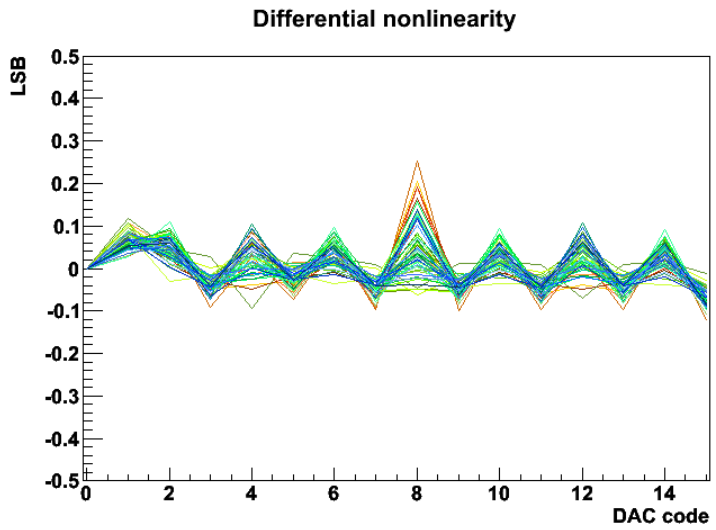


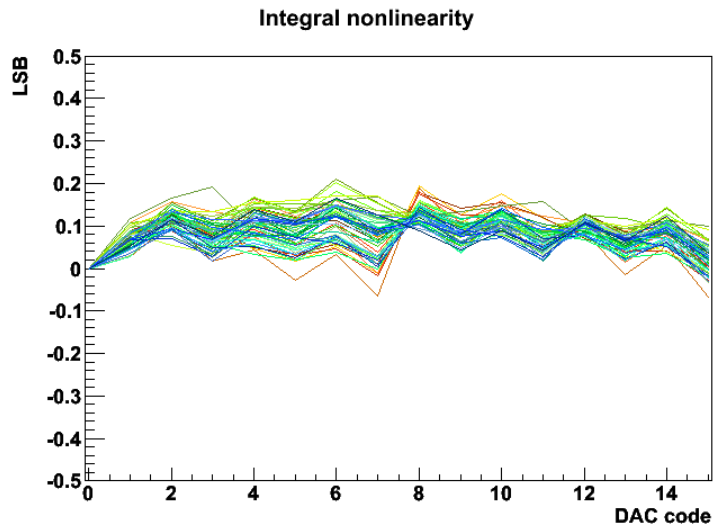


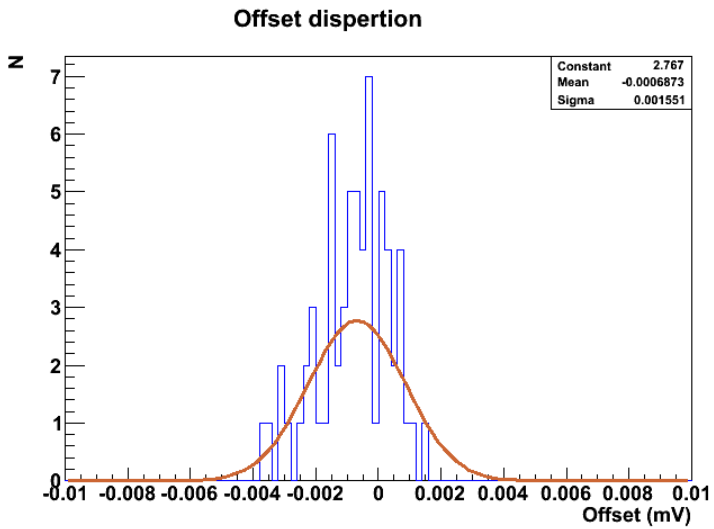


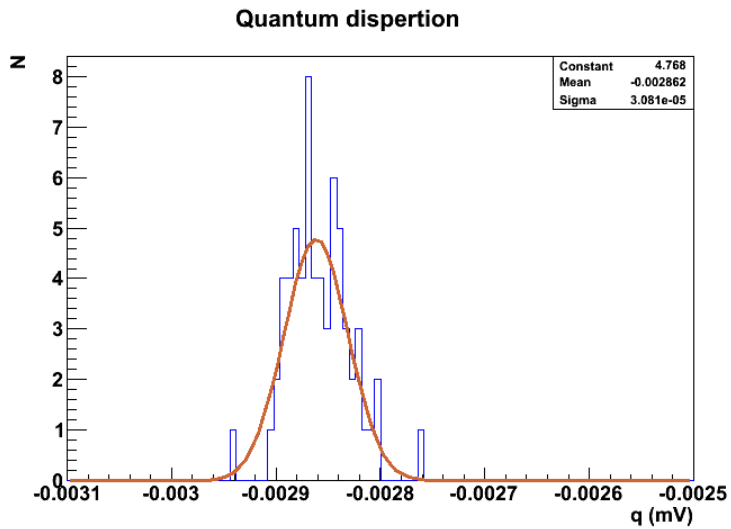
For each DAC, the linearity is about 3 DACU.

Offset correction DAC









The linearity is better than 1 DACU and q=2.8 mV.

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Test procedure

For each channel of each chip (peaking time: 200 ns, pedestal DAC @7):

- Test input bondings (inject to all channels at the same time with an external capacitor);
- Measure pedestals;
- Inject 22.5 fC with internal C_{test} *vs.* threshold.

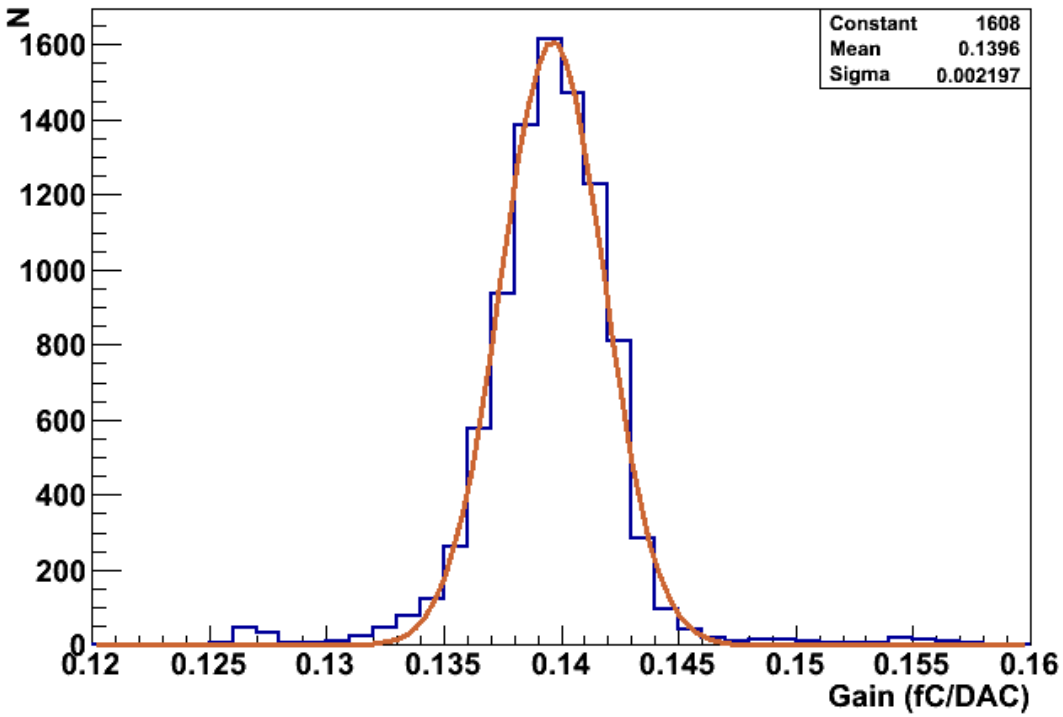
Then, analyze data off line with MICROMEGAS data analysis framework:

- Verify bonding of each input;
- Plot S-Curve for each charge, for each channel;
- Plot inflexion point of S-Curves *vs.* input charge;
- Verify gain for each channel.

341 chips have been tested.

Gain dispersion

Gain dispersion, for all channels of 144 chips, @ T_p=200 ns:



Mean: 0.14 fC/DAC Sigma: 0.002 fC/DAC.
Threshold dispertion: 5 DACU peak-peak per chip (without correction). 2× better with offset correction.

Test results

For 195 chips analyzed:

- 6 faulty chips (configuration errors);
- 11 with a packaging problem;
- 12 with bad gain;
- 2 to be retested;
- 312 OK;

Yield: 91.5%. Enough to equip 12 PCB (24 ASIC each, to build 2 square meter) + 1 test PCB.

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ASU novelty

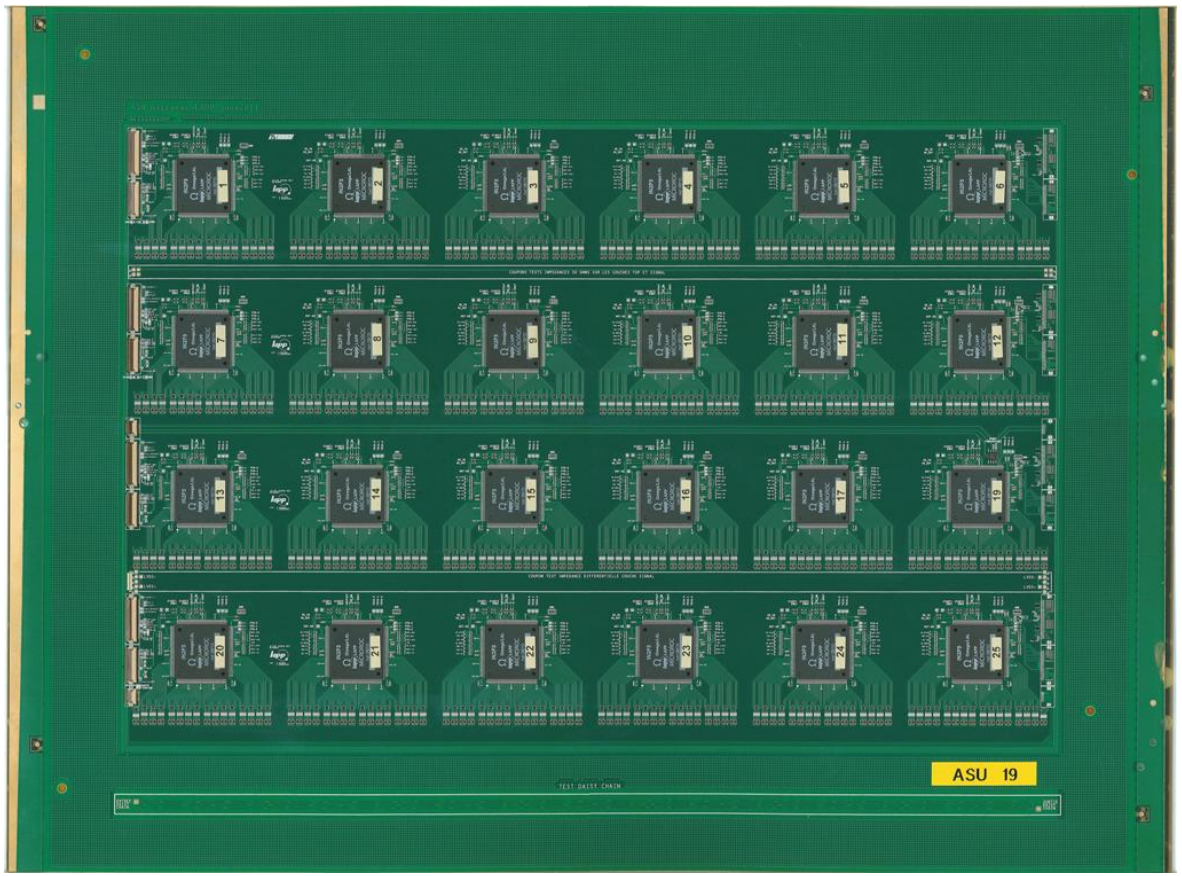
Apart minor bug correction, some novelties on the new Active Sensor Unit PCBs:

- Temperature sensors;
- Independent lines for configuration and readout (4× faster, and reliability increased), with line by-pass capability on the inter-DIF;
- Improved sparks protection arrays for inputs;
- ESD protection on data lines;
- Hatched ground plane below pads (reduce C_{det} by 30%);
- Passive calibration path.

13 ASUs have been received and cabled, with no bug nor error !

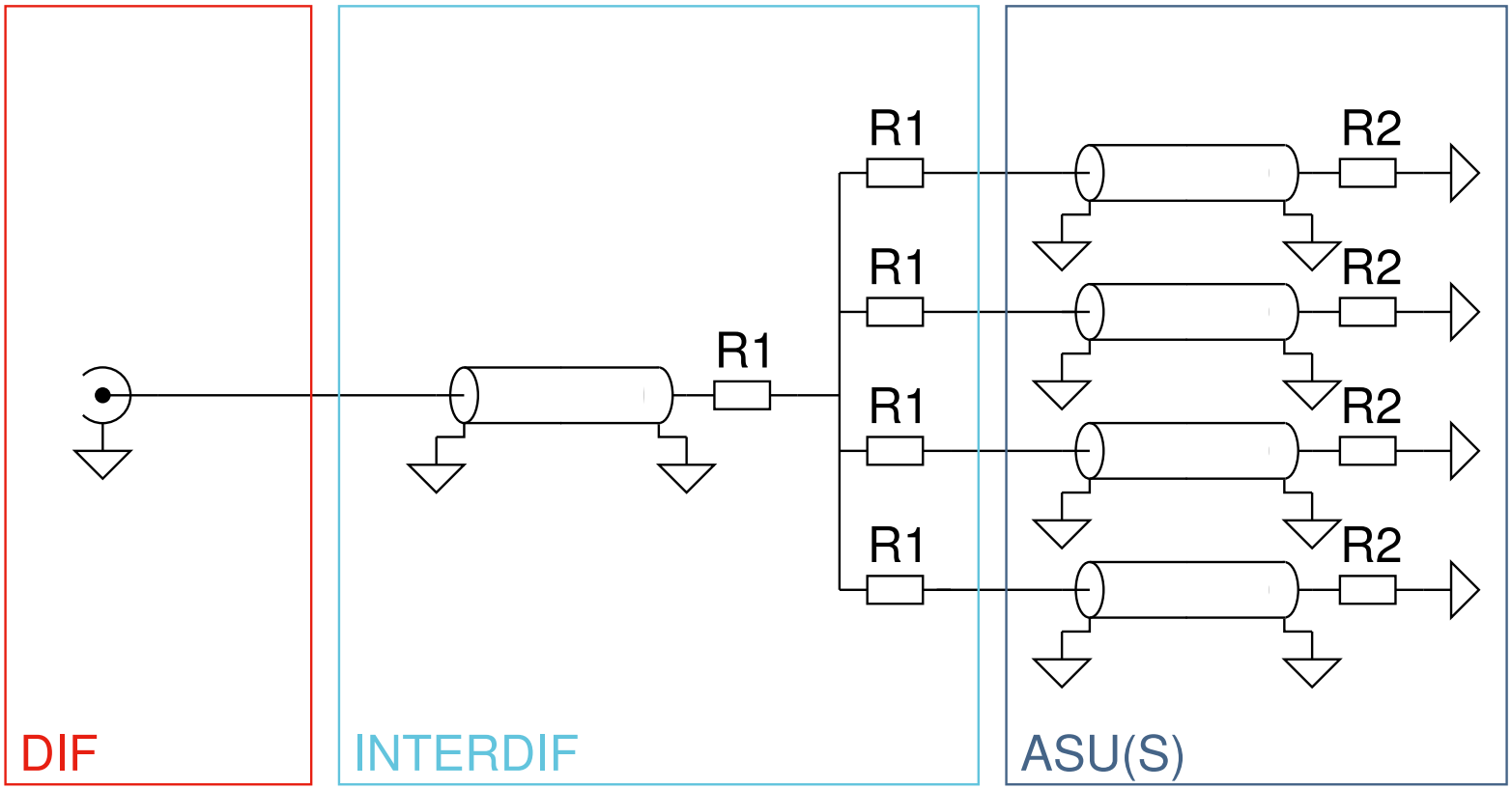
ASU photography

Cabled PCB, before mesh lamination and cut at final dimensions (32 cm×48 cm).



Reminder: 1536 pads of 1 cm^2 on the other side.

Calibration path



Strips are 50 Ω, R2=50 Ω and R1=30 Ω.
Pulse amplitude is divided by 4.

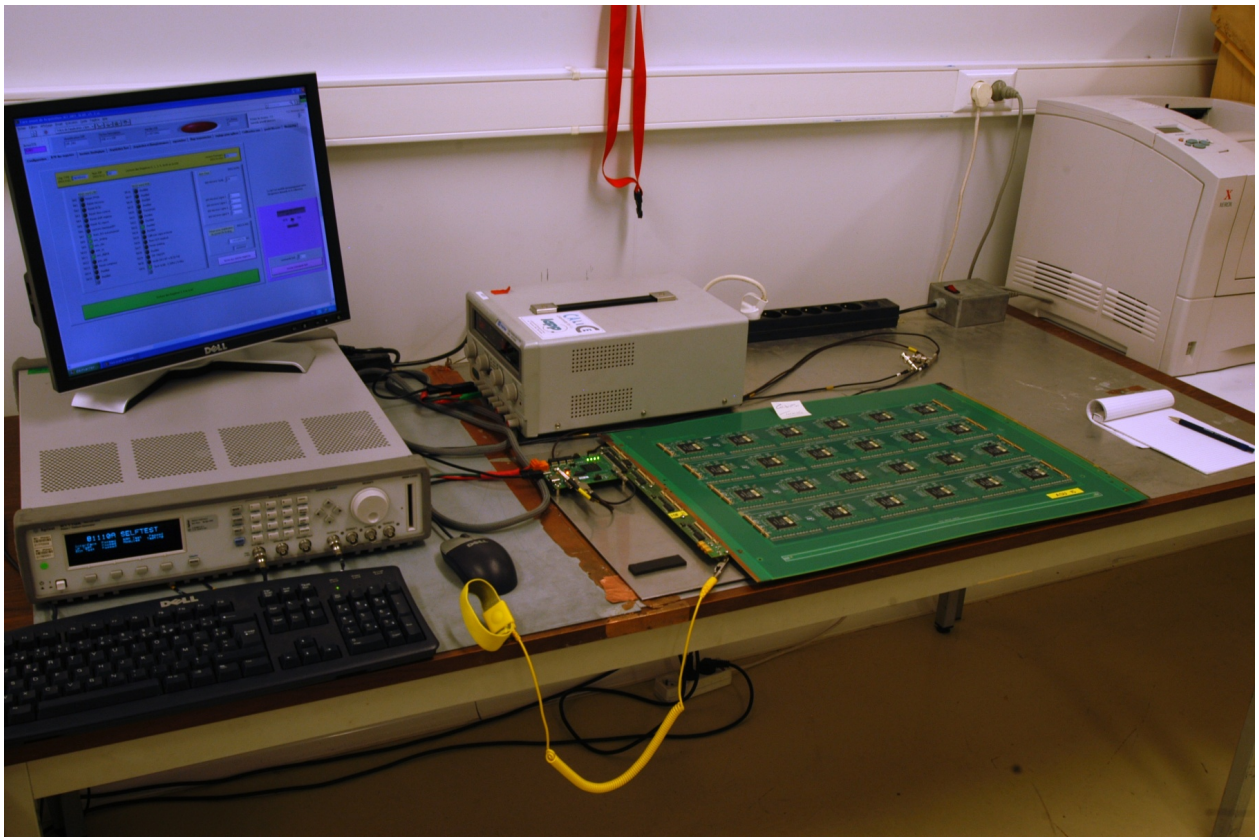
Calibration path tests

100 mV test pulse seen with 1 GHz active probe (left: begining of line, right: end of line).

Attenuation of line length has been measured and is corrected during inter-calibration.
Line mismatch is also taken into account.

ASU tests

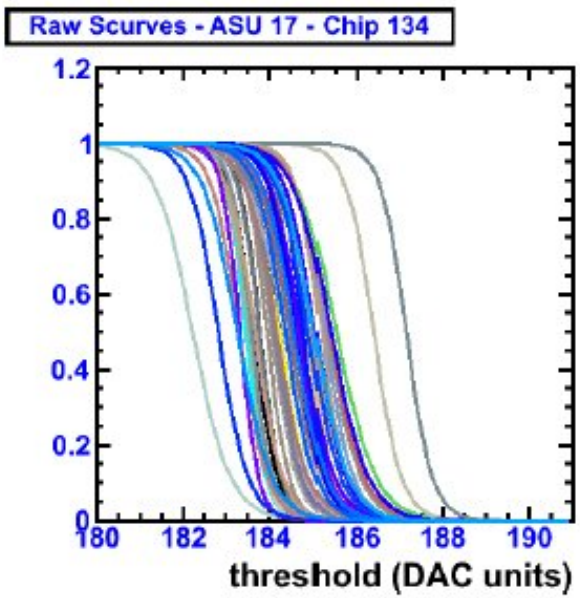
A detailed test procedure has been established and a quality form is filled in a database after each step.

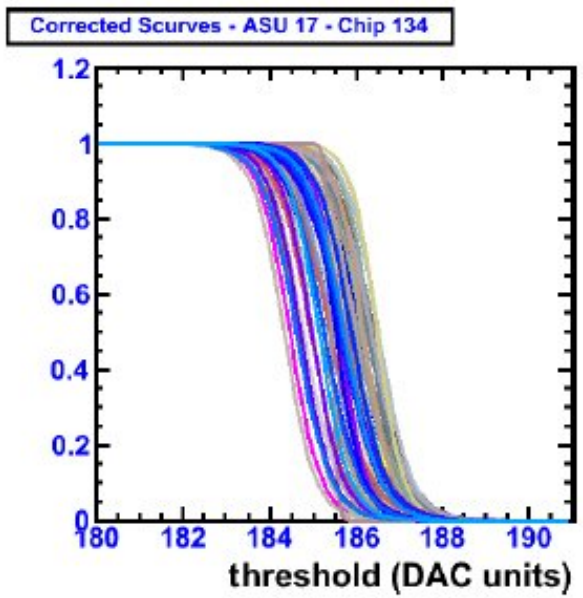


Different grounding tests have been performed to select the best grounding method.

Threshold alignment

The lowest thresholds are aligned for all channels.

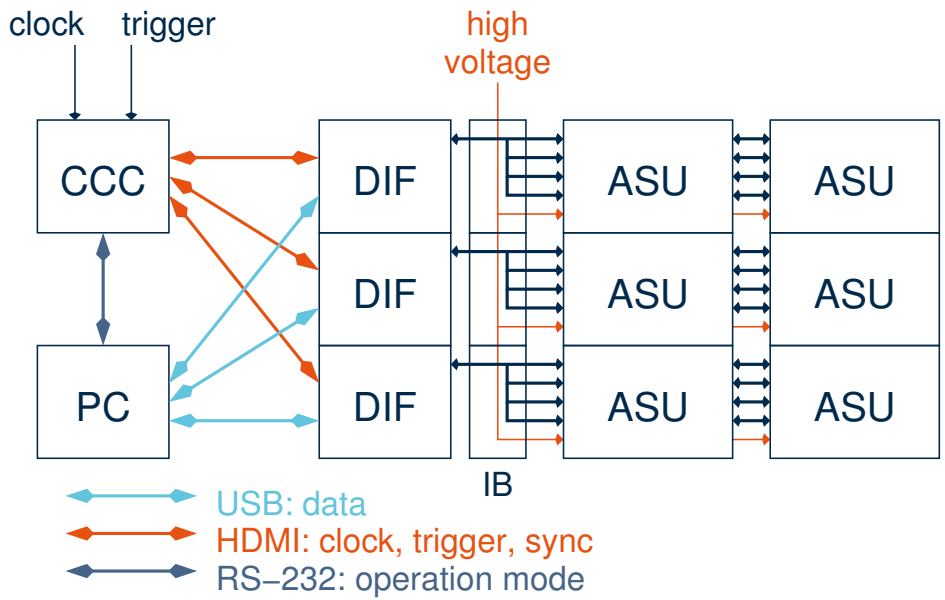




ASU Readout (I)

Now, each line is read independently:

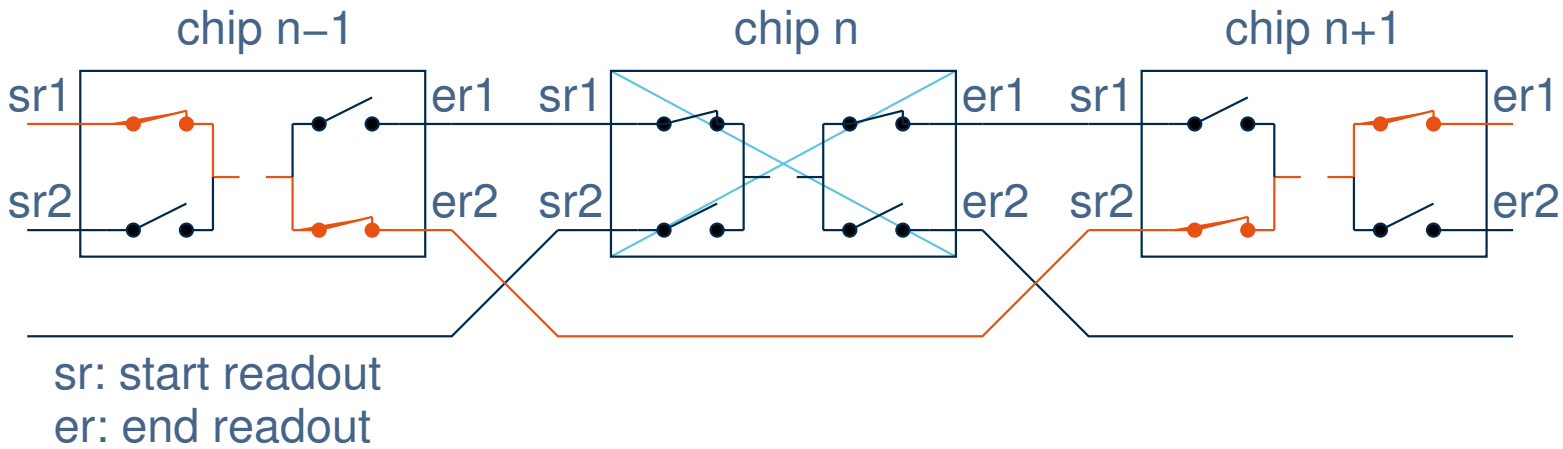
- faster readout;
- easier debug;
- by-pass off entire individual line now possible (not happened !)



As the CALICE DAQ is still not stable, acquisition are still perfromed with USB link. . .

ASU Readout (II)

The readout is serial, with daisy-chained token for starting data output.
The data output is open collector: only one wire is needed.



In case of daisy-chain failure, both token line and readout line are duplicated and selectable via configuration register.

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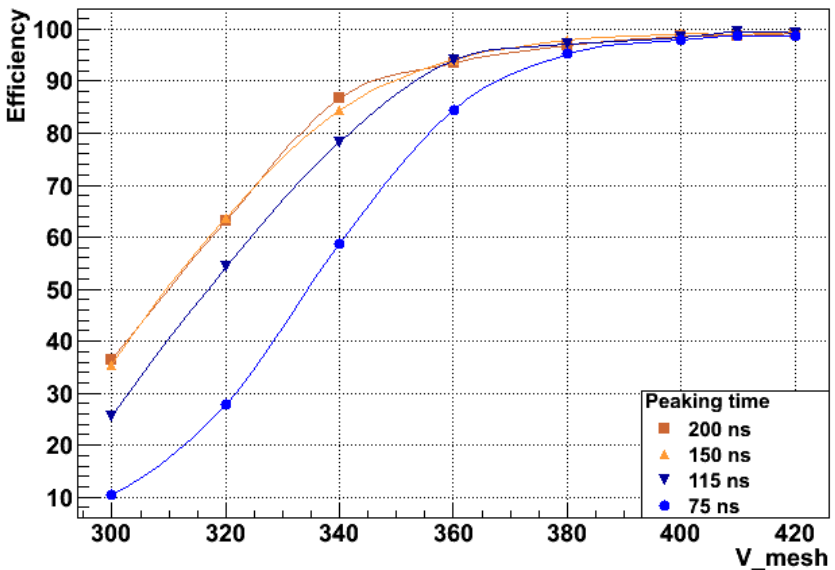
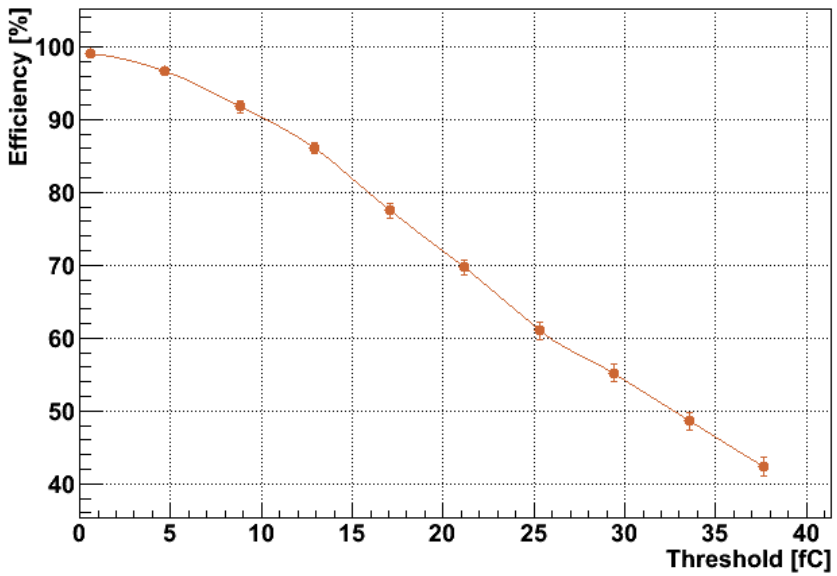
Efficiency

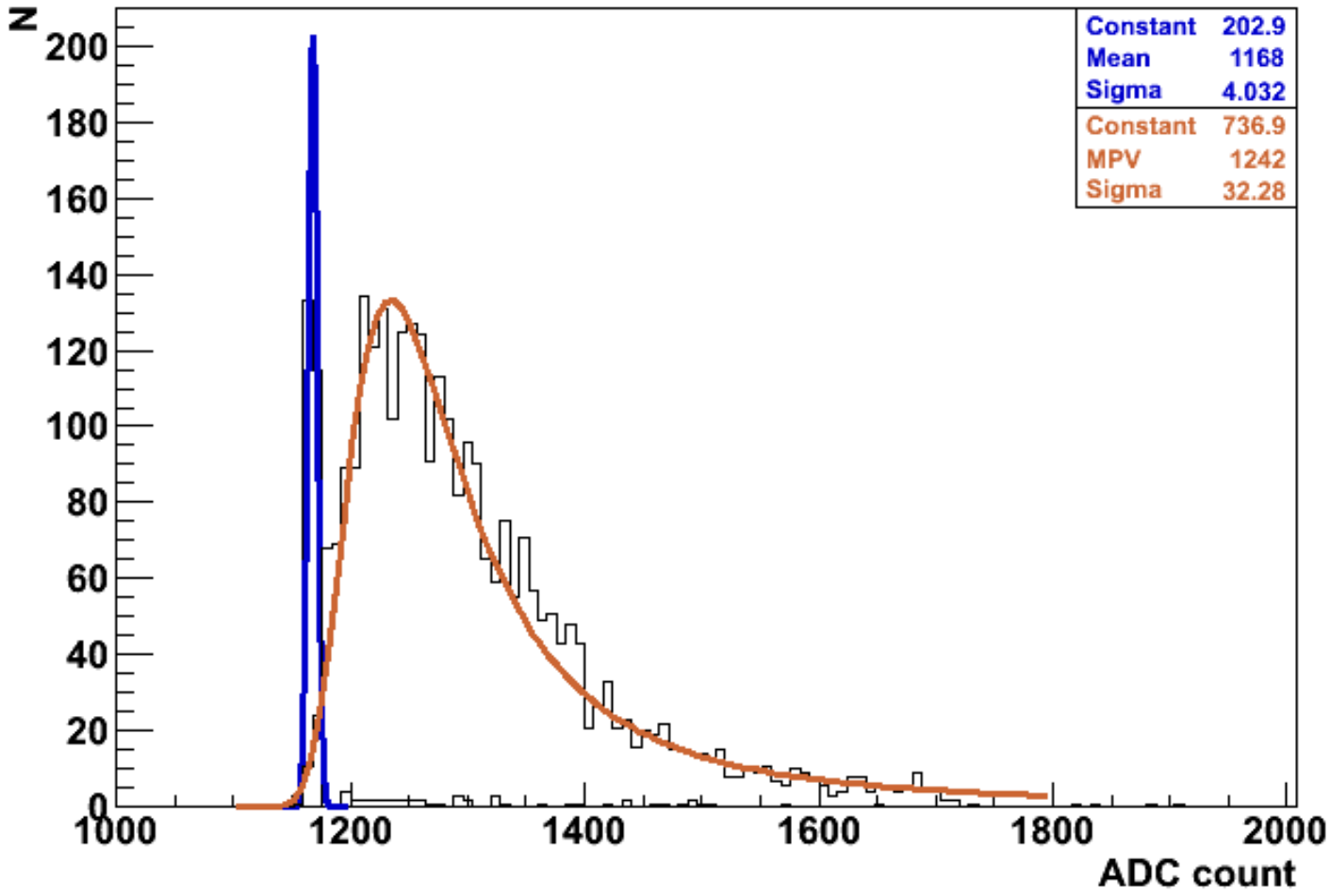
The efficiency has been verified, and is in very good agreement with our Gassiplex readout prototypes.
Morover, the optimum shaping time is determined as a function of MM gain.





Analog readout

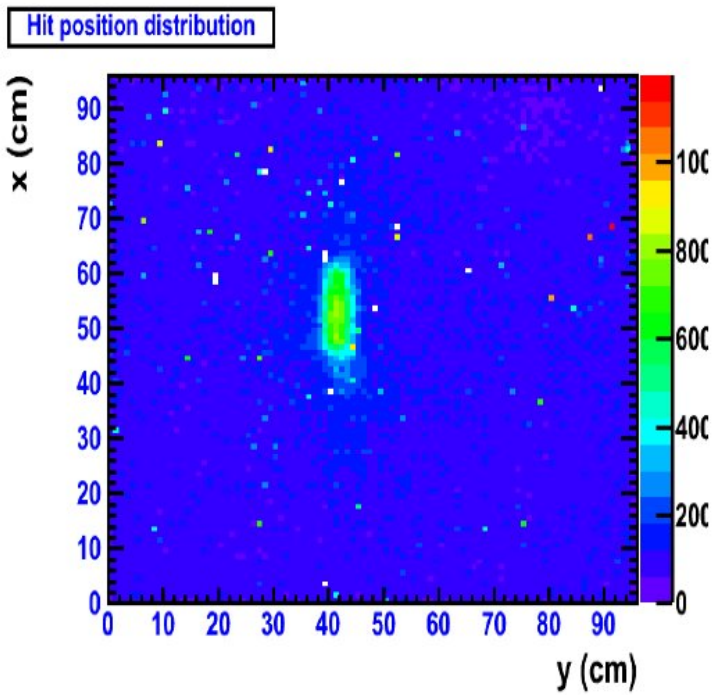
Preliminary plot, with analog multiplexed readout for one pad (external 12-bit ADC).



A clean expected Landau fit is obtained. Usefull in DHCAL to fix and

RAMFULL mode

Beam profile, in trigger less mode (ILC operation):



- Pedestal alignment w.r.t. low threshold such that average channel noise rate is 0.1 Hz;
- Less than 10 noisy channels over 9216 during whole test beam;
- Threshold of about 0.7 fC from pedestal;
- RAMFULL time is $127 \times 0.1 \,/\, 64 \approx 20$ s (beam @200 Hz)

Conclusions

The MICROROC-based 1st square meter has been succesfully tested in beam at SPS this summer!

- 2nd square meter just been finished;
- 600 chip will be ordered very soon (4 planes);
- A test ASIC with clamping circuit has been submited to foundry to remove external protection;
- A resistive ASU is under design.