Progress with GEMROC front-end and fast DAQ (part 1)

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Outline

1. Requirements for readout electronics
2. GEMROC architecture
3. Ethernet based DAQ system
4. Test setup
5. Measurements results
   - ASICs electronic tests
   - Test with small 10x10 cm^2 GEM detector
6. Conclusions

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Specification for the readout electronics

Determined by readout of large area $30x30\,cm^2$ 2-D GEM detector in the PRR

- Input signals - short current pulses with duration time of 40 ns
- Input charge from 0 to 500 fC with the most probable value of 50 fC
- Noise defined as the Equivalent Noise Charge (ENC) below 0.5 fC for timing and 0.43 fC for energy sub-channel (strip capacitance of 60 pF)
- Minimum discrimination threshold 6 fC input equivalent
- Self-triggering
- Expected particle flux $\sim 10^6\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ (10^5 pulses/s per readout channel appearing randomly in time)
- The maximum rate is limited by the time resolution of signals recorded from X and Y strips - required time resolution better then 100 ns p-p
- To be implemented as a multichannel Application Specific Integrated Circuit (ASIC)

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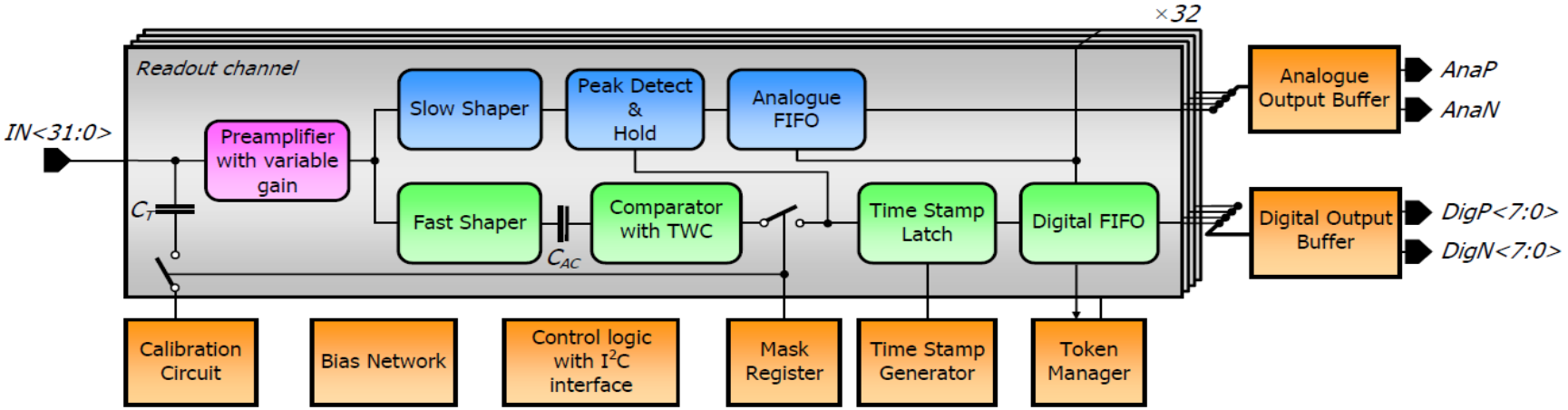
GEMROC architecture



- Each channel is split into: slow (energy) and fast (timing) sub-channels
- Switchable gain and signal polarity selection
- Derandomization of data and zero suppression in the token-based readout
- Self triggering mode - readout initiated by the input signals
- Internal testability functions
- 32 channels in one ASIC
- 0.35 μm CMOS process

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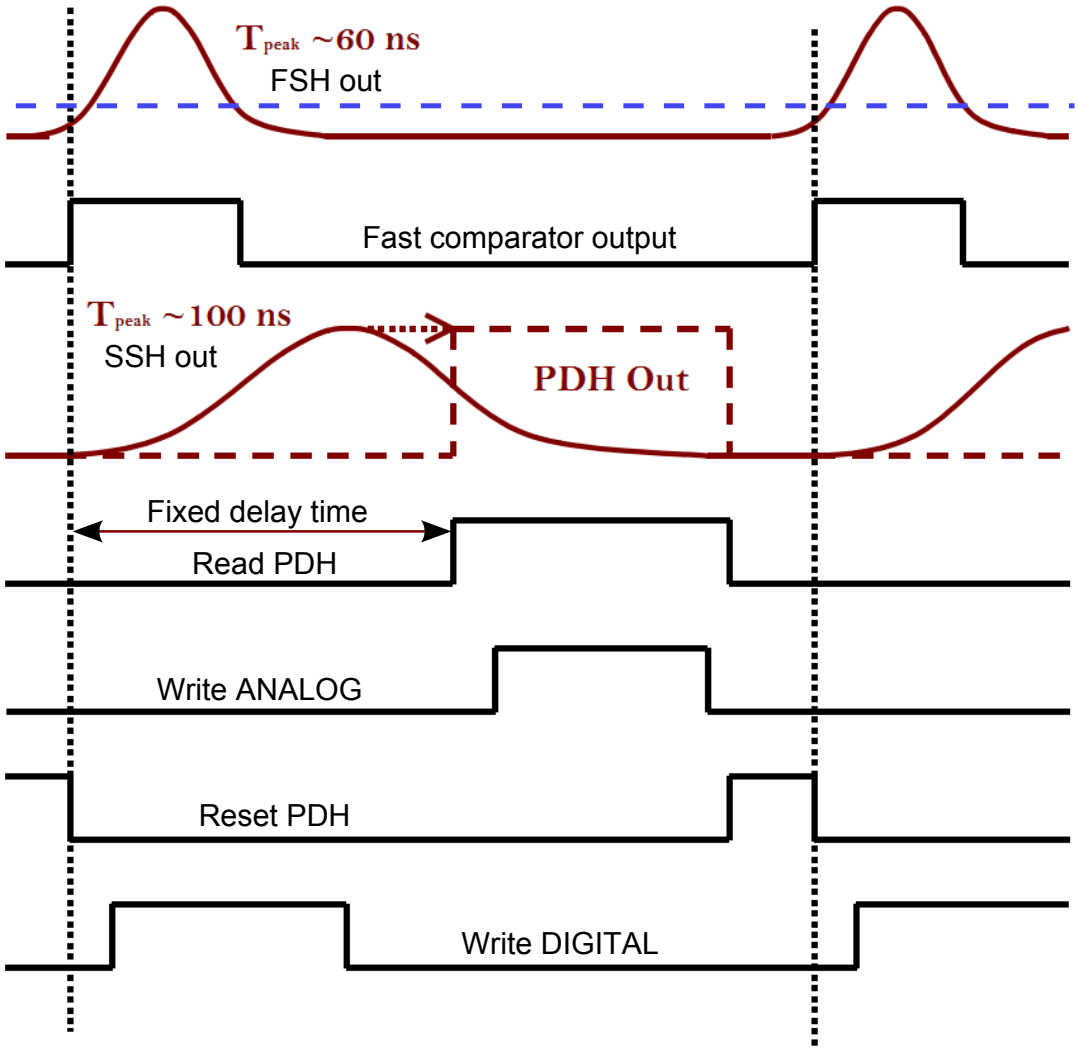
Signal timing



- Timing diagram for important internal ASIC signals
- Comparator output generated according to FSH output
- Store SSH output to PDH
- Write signals for FIFOs and reset PDH

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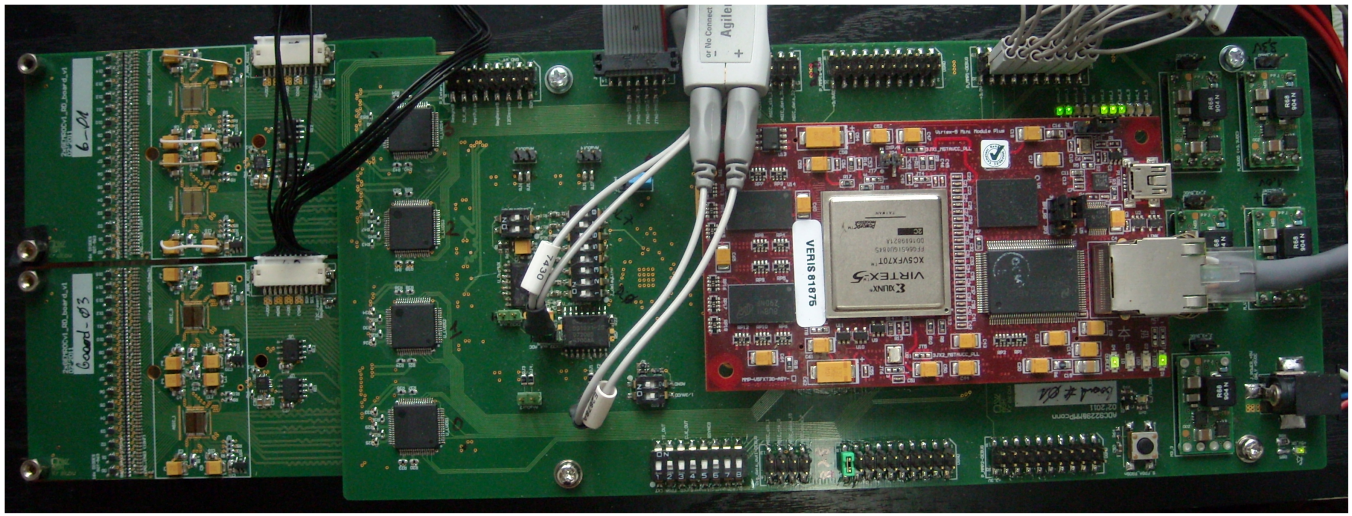
DAQ system



- Custom ADC board hosting Virtex 5 FXT70 FPGA Mini Module Plus
- Capable to read out 4 ASIC with full speed
- Mater/slave board connection for simultaneous X and Y coordinates readout
- Generates clock, reset and test pulse signals for ASICs
- Provides the I2C slow control
- Output throughput up to 1 Gb/s using standard Ethernet link

DAQ system details

- Parallel processing of up to four ASICs
- Degraying ASICs' time stamps and channel IDs
- Reading out digitized analogue amplitudes using AD9229, quad 12-Bit, 65 MSPS ADC
- Adding course time stamp to let it run for a day before overflow
- Combining above to create 64bit frame of raw hit
- Queuing data into FIFO's for each ASIC before sending via Ethernet link
- Apart of the measurement data clocks present signal and I2C status are sent to PC
- Processing incoming frames to control the board and ASICs using Picoblaze micro-CPU

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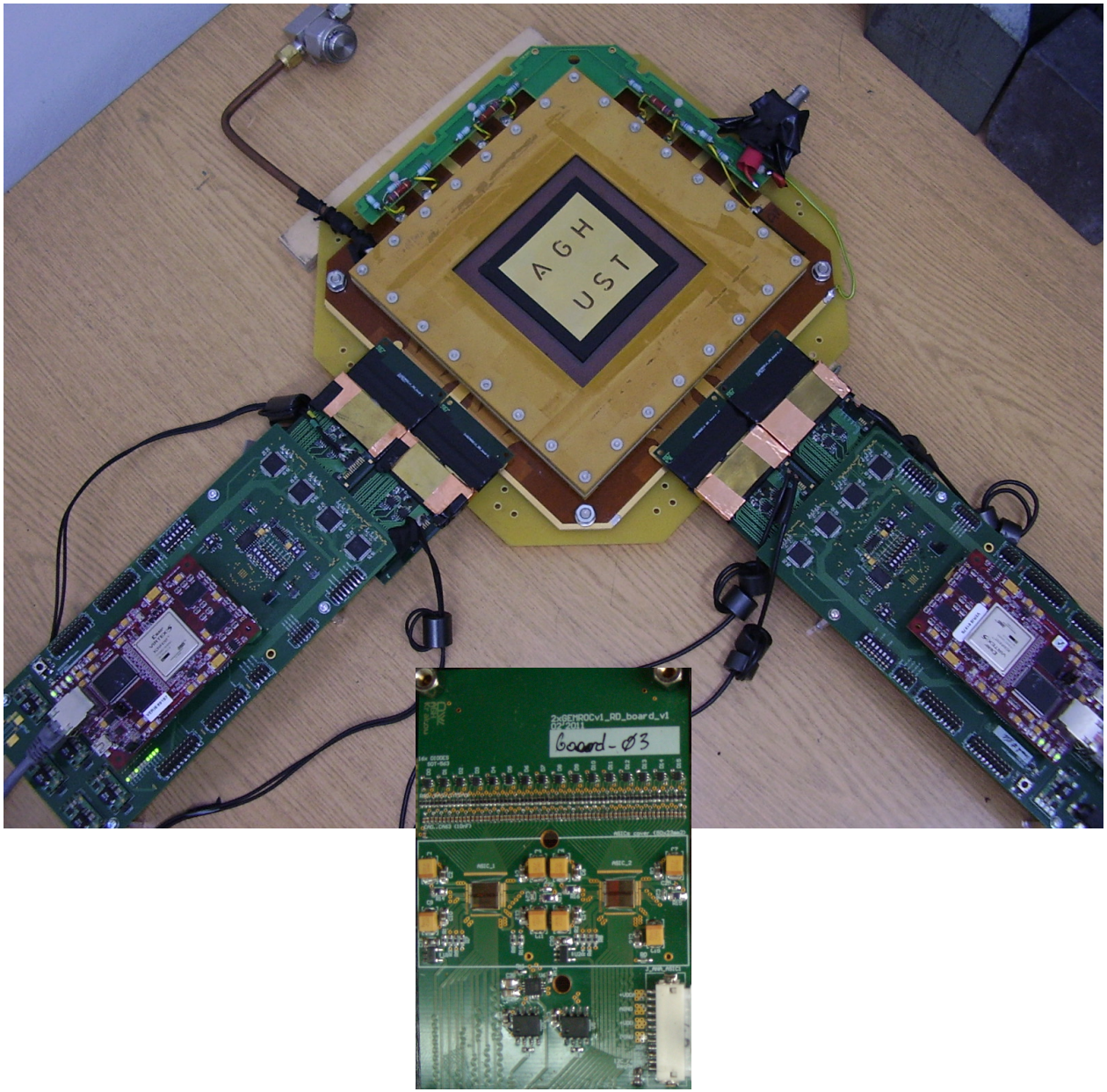
Test bench with triple-GEM chamber



- Custom designed DAQ boards with Ethernet output protocol
- Four ASIC boards each one comprising 2 GEMROCs
- Two modules in order to read X and Y planes
- Triple-GEM chamber with 128x128 readout strips (pitch of readout strips is 800μm)

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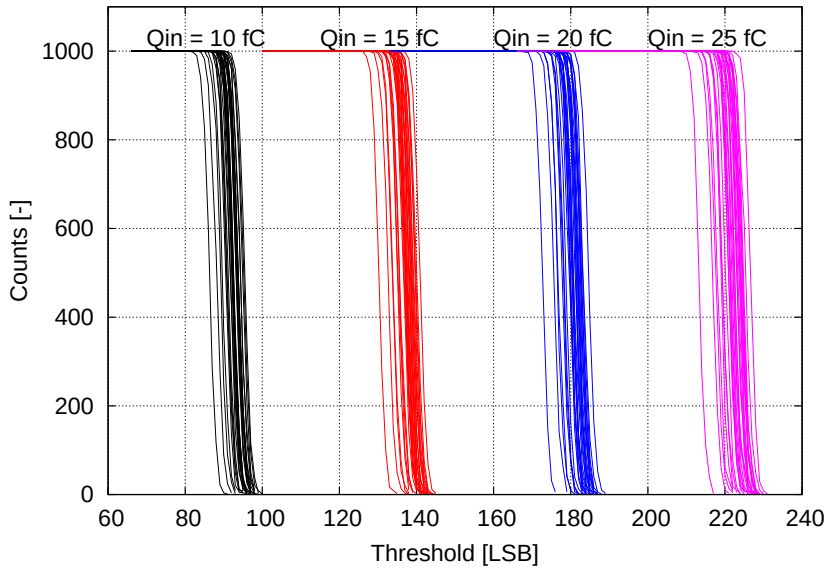
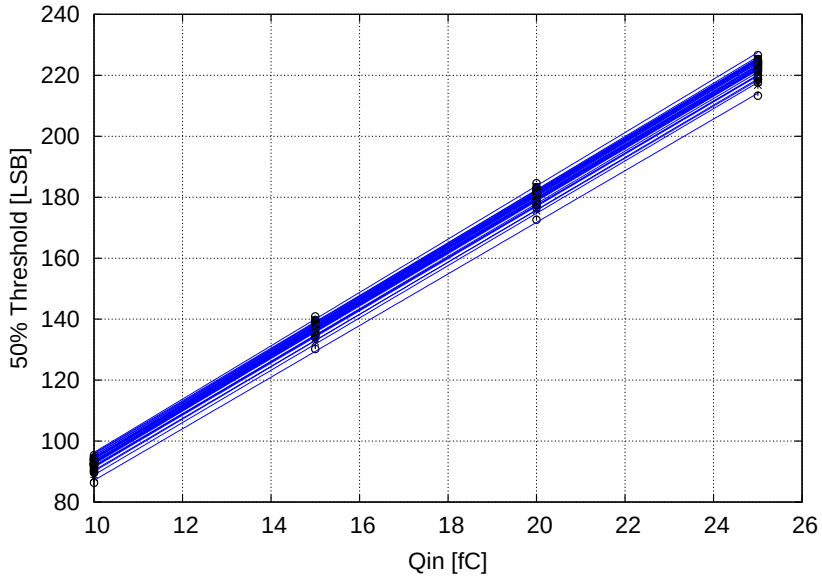
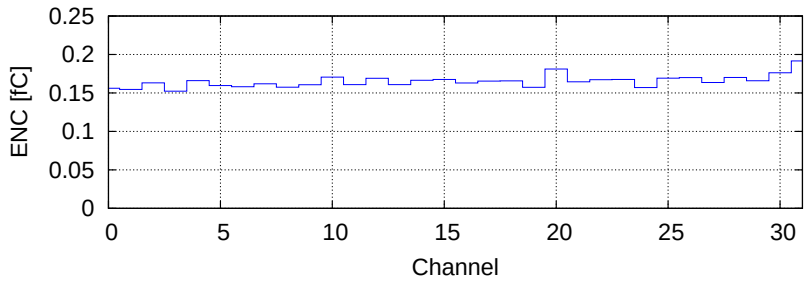
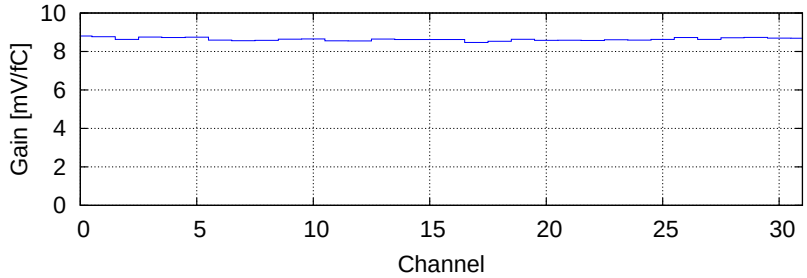
Timing sub-channel test results

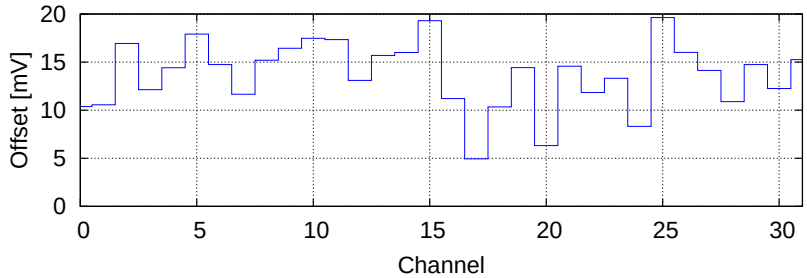




- Using ASICs' internal testability function







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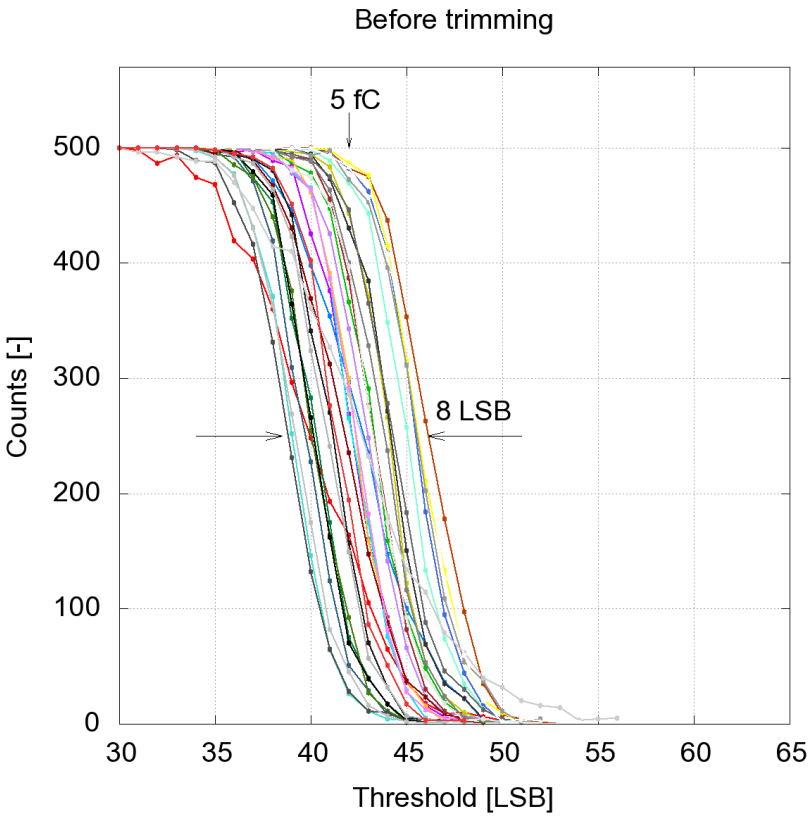
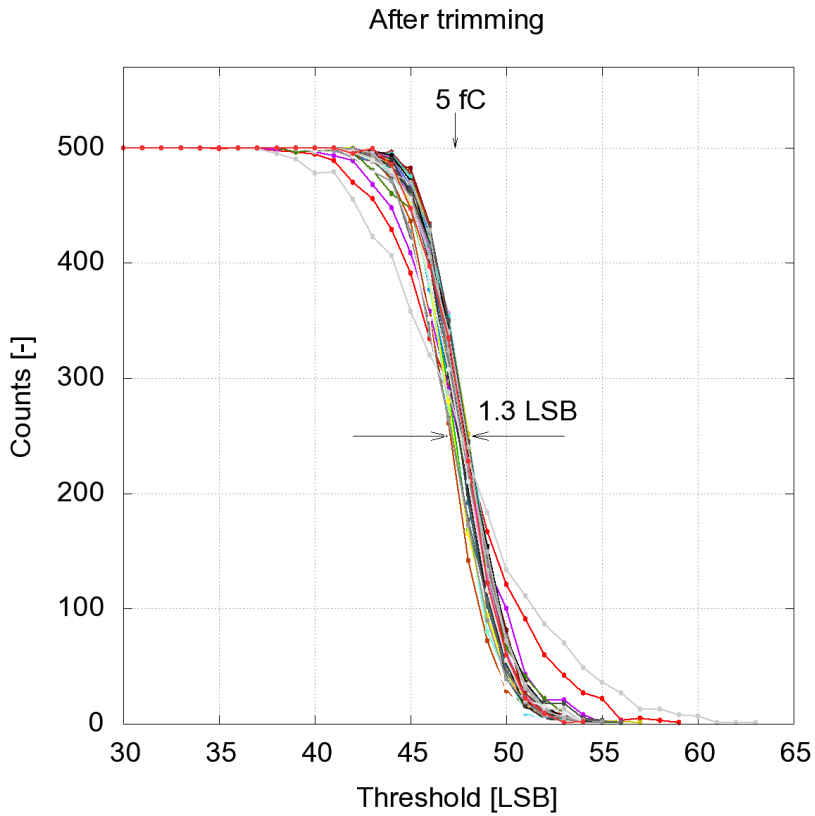
Trimming procedure

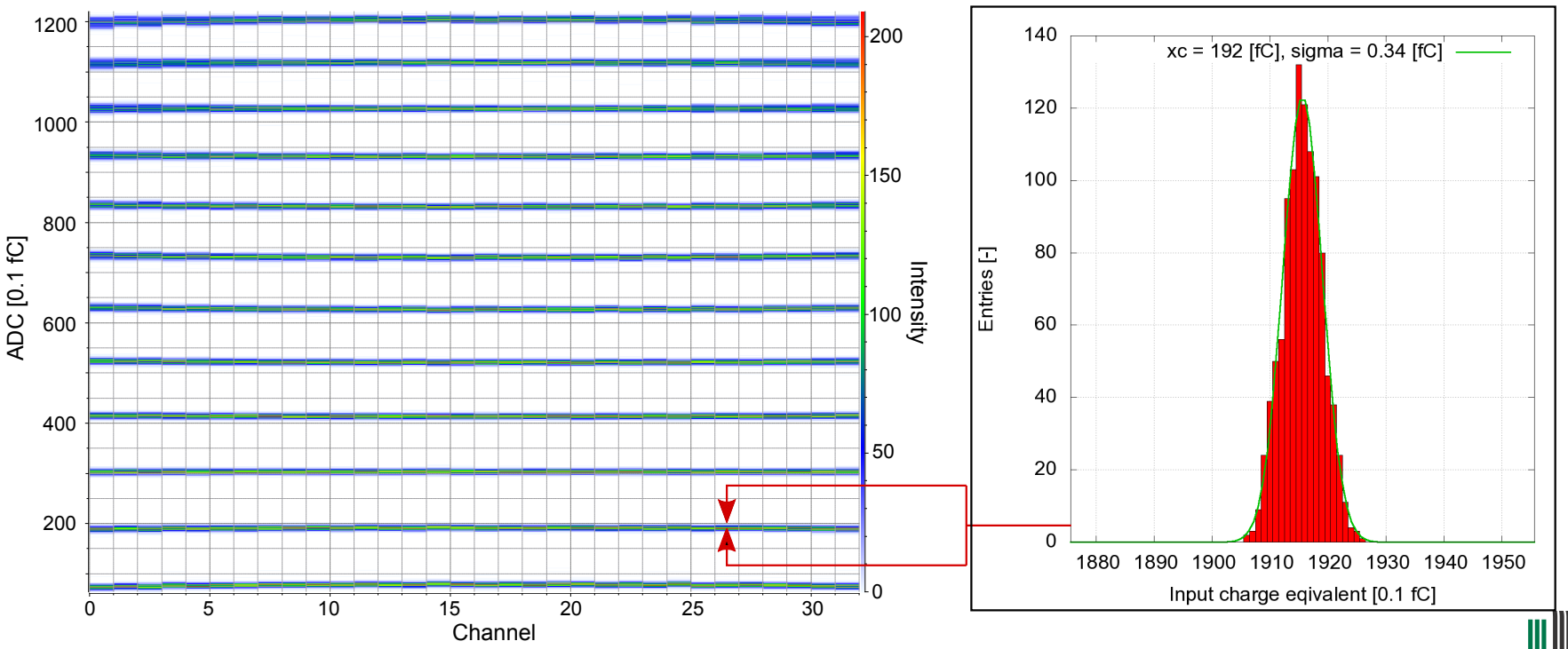
- Performed in order to get the same threshold level for all the ASICs' channels
- 5-bit trimming DAC implemented in each channel
- The channel-to-channel threshold spread reduced to 1.3 LSB (1 $Th_{LSB} \approx 0.1$ fC)





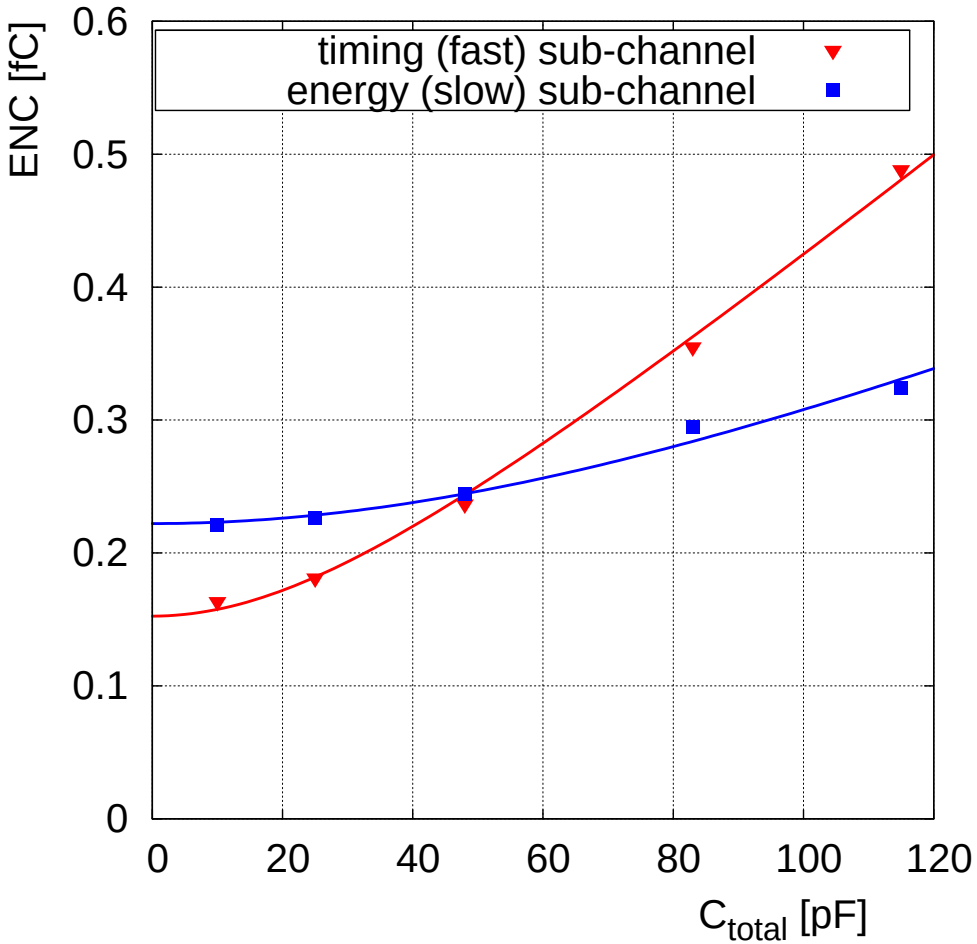
Energy sub-channel test results

- ADC responses of one ASIC for input signals from 15 fC to 125 fC (after software pedestal correction) using internal test pulses



Noise test results

- Measurements performed with external capacitors connected to randomly chosen channels



$$ENC = \sqrt{aT_pF_i + \frac{b}{T_p}F_vC_{tot}{}^2}$$

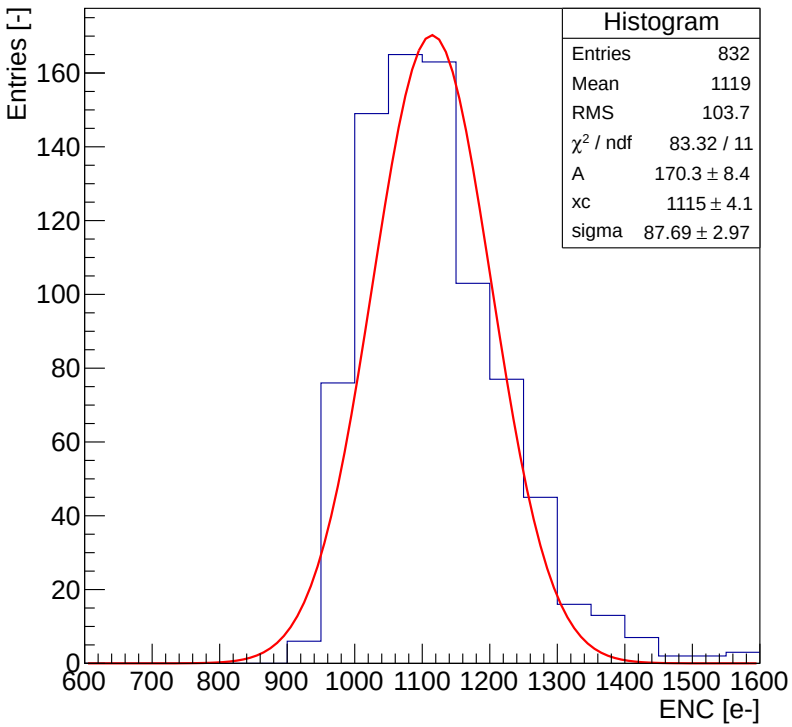
a, b - spectral densities of the equivalent current and voltage input noise respectively,
F_i, F_v - constants specific for the shaping circuits,
T_p - the peaking time,
$C_{total} = C_{det} + C_{in}$ - total capacitance at the input.

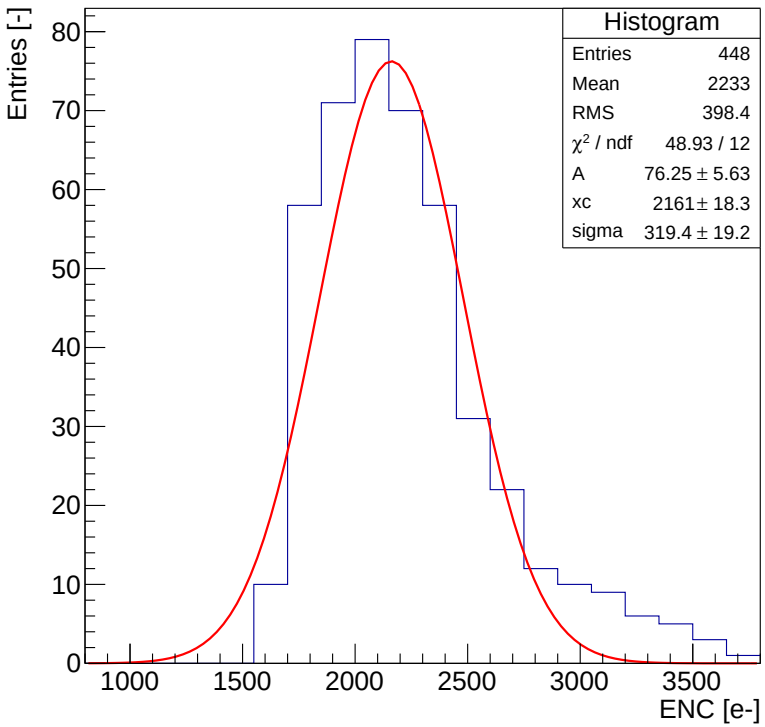
Noise distributions (for almost all tested ASICs)

- ASICs not connected to GEM detector

- Timing sub-channel noise distribution for 26 ASICs
- Average is 1120 e^-

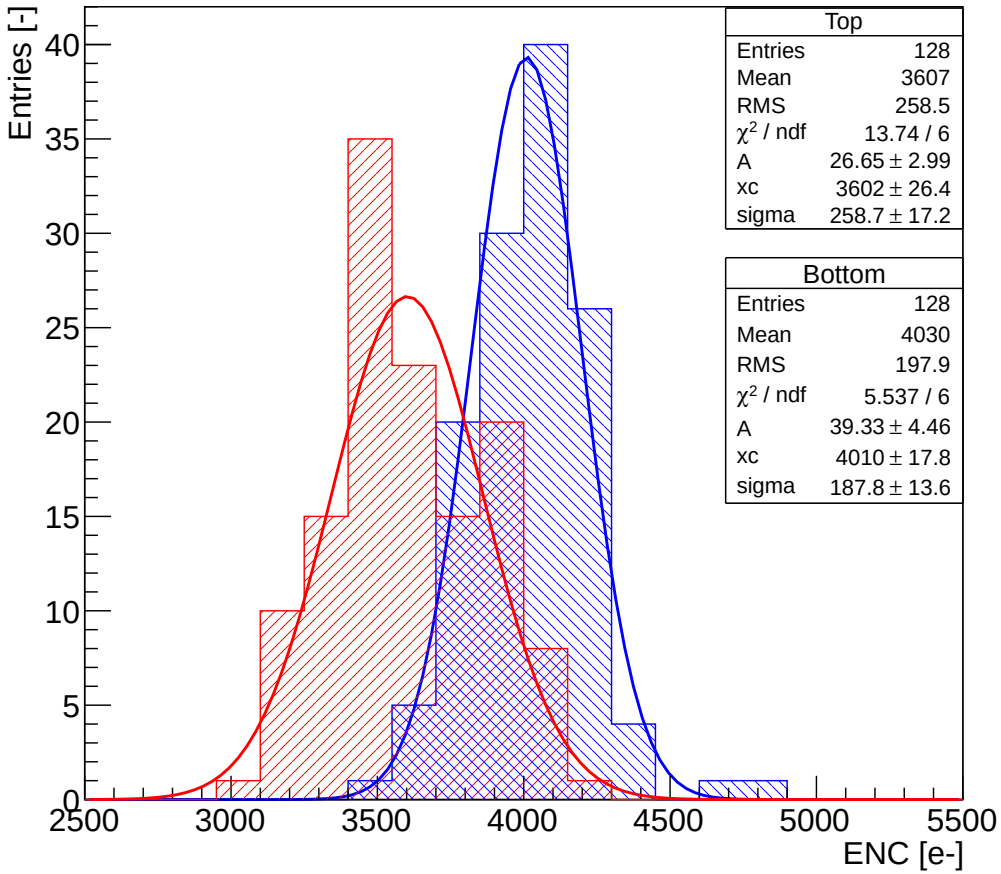
- Energy sub-channel noise distribution for 14 ASICs
- Average is 2230 e^-





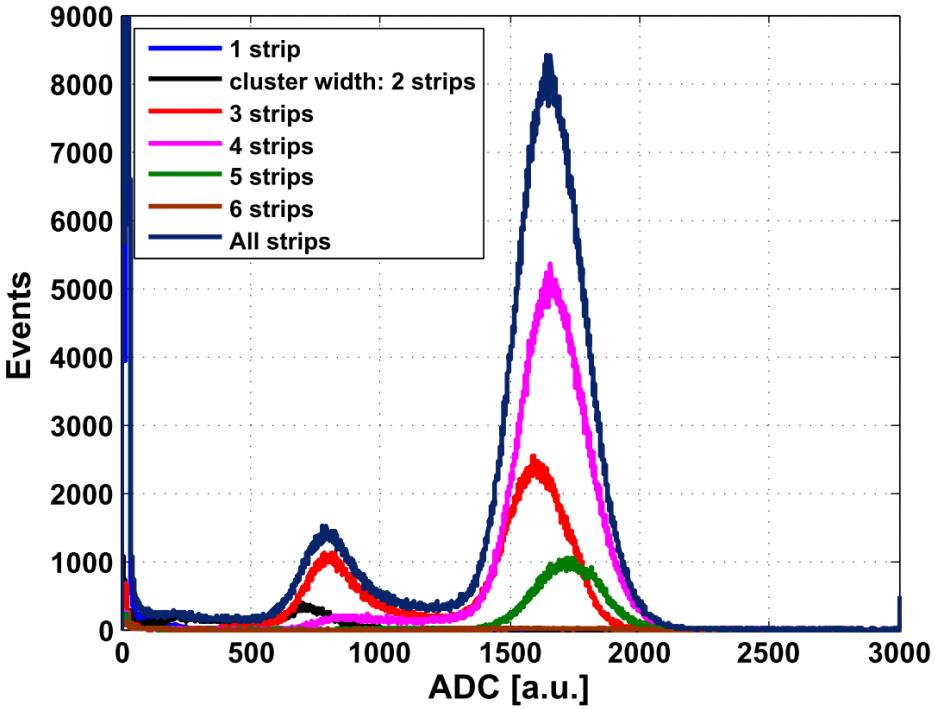
Timing sub-channel noise distribution

- Measured with 10x10 cm^2 GEM detector
- Top and bottom plans of detector measured separately
- $ENC_{TOP} \approx 3600\ e^-$, $ENC_{BOTTOM} \approx 4000\ e^-$

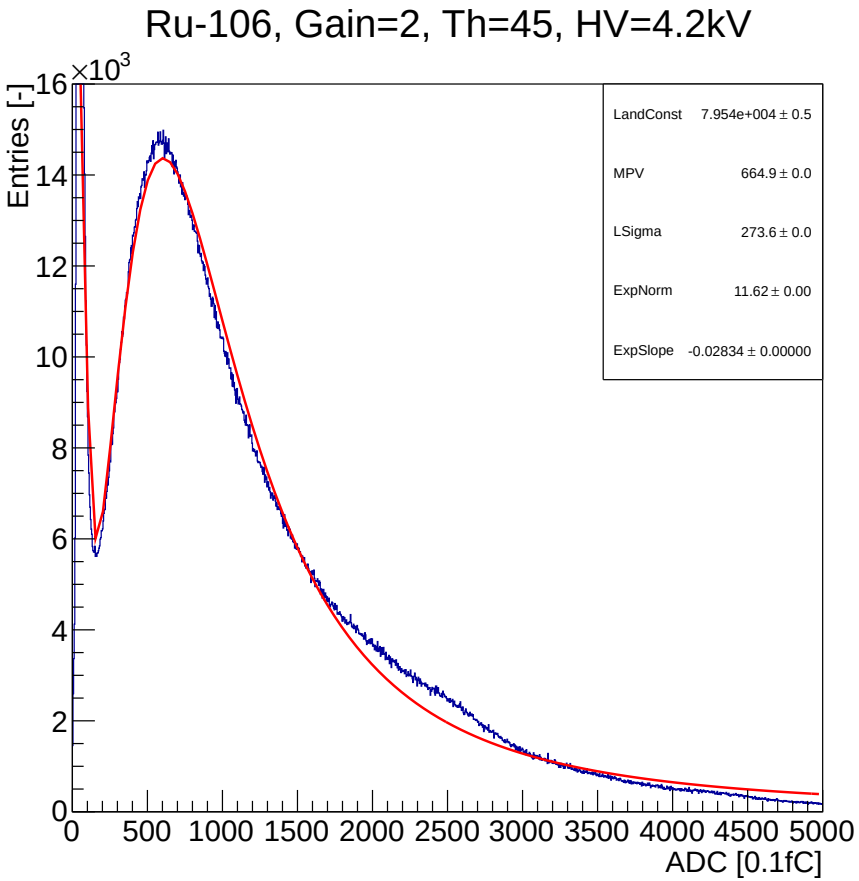


X-ray and β^- measurements

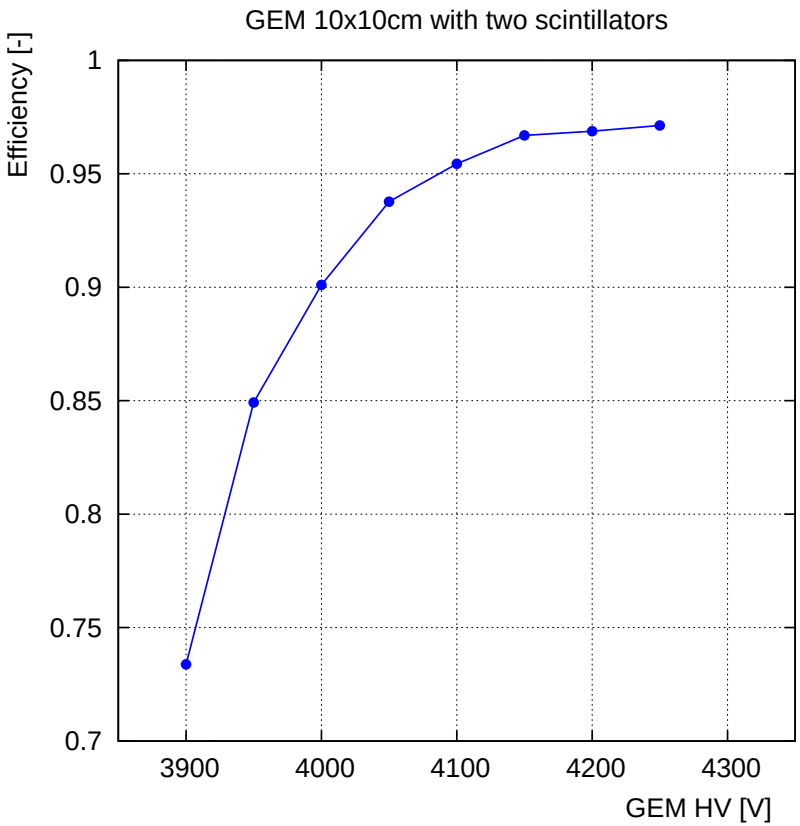
- ^{55}Fe amplitude distribution
- Main peak FWHM = 19%
- Total energy distribution and clusters of hits



- ^{106}Ru amplitude distribution
- Landau fit



Detection efficiency



- Measurement done with 10x10 cm^2 GEM
- Two scintillators above and below the GEM detector were used
- Time stamp of a coincidence signal from scintillators was used to find corresponding hits in GEM detector

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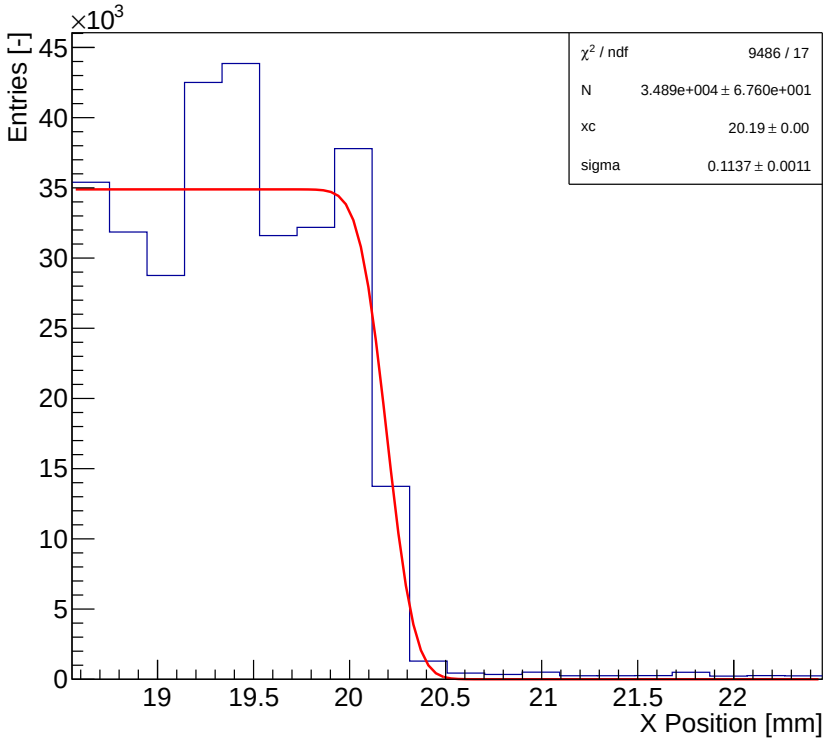
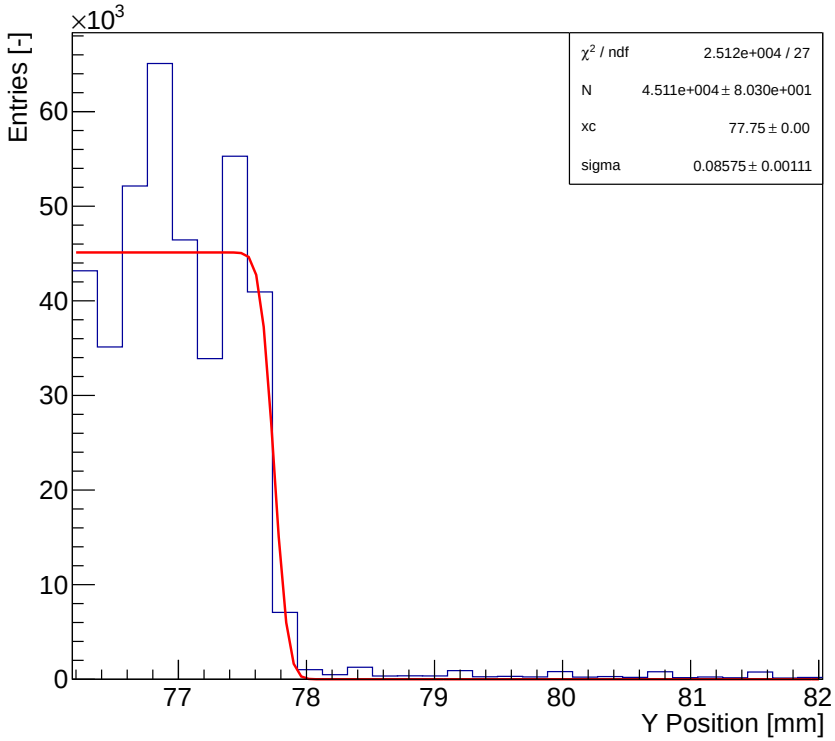
Spatial resolution (very preliminary)

- The edge image with collimated X-ray beam

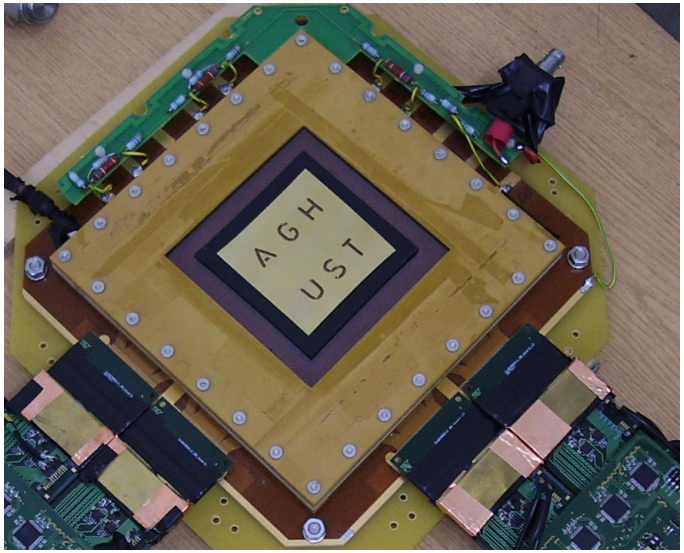


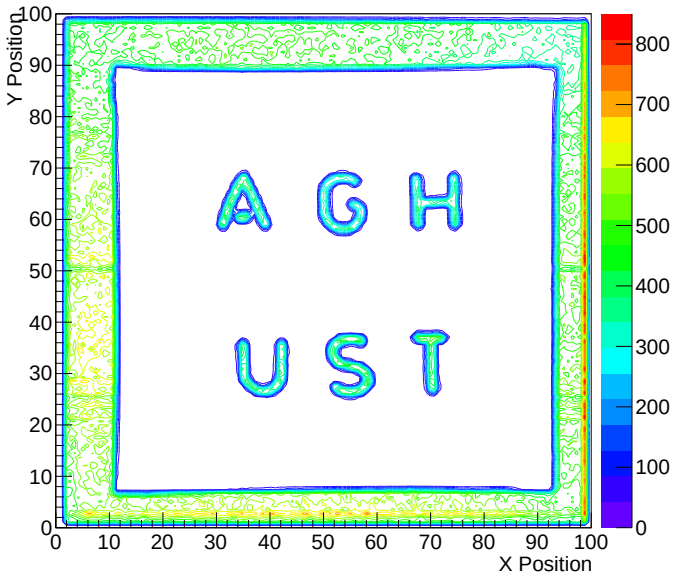


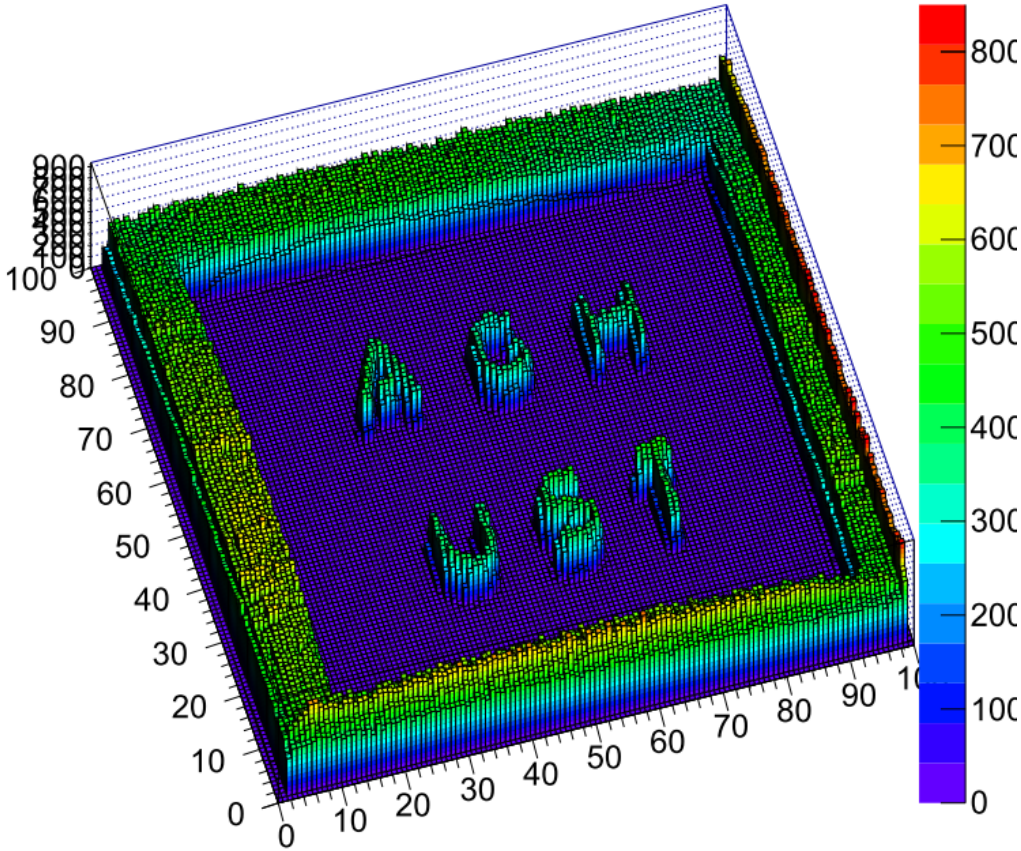
$\sigma_{\mathrm{BOTTOM}} \approx 114\mu m$

$\sigma_{\mathrm{TOP}} \approx 84\mu m$

2-D imaging



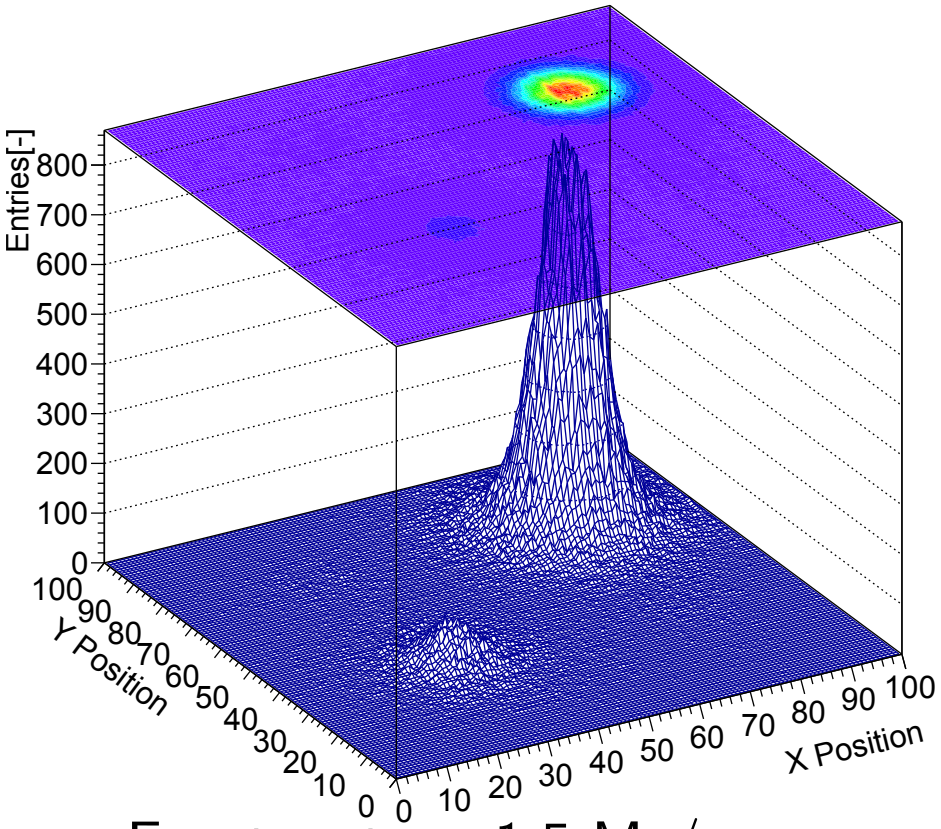


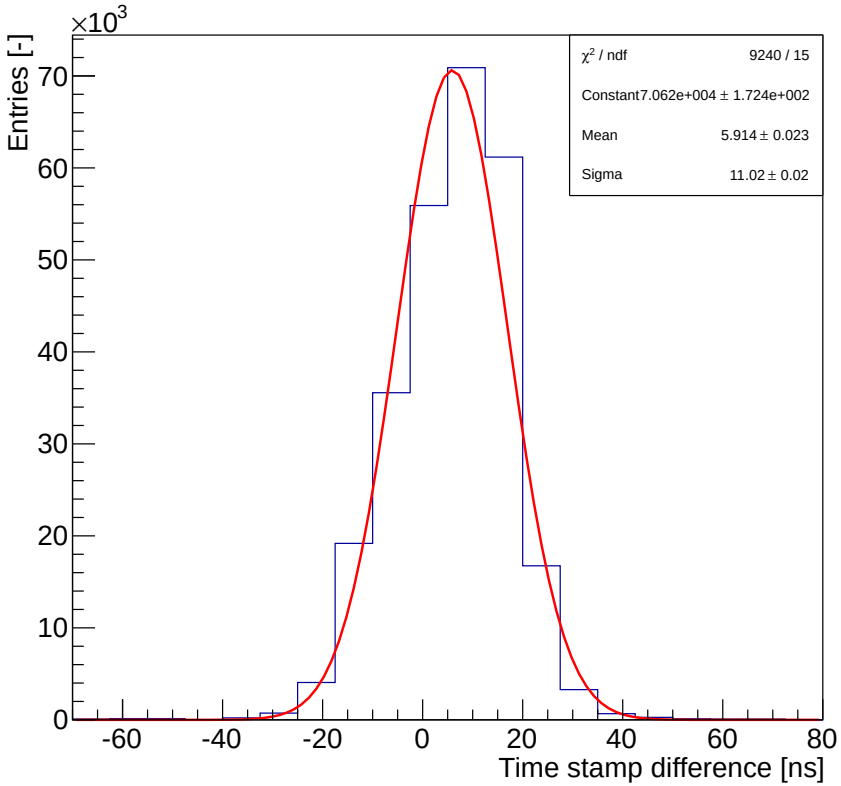


- ^{55}Fe X-ray source
- 50 ns coincidence time window
- Threshold about 6 fC

High count rate – time resolution

- Two sources measured simultainously ^{55}Fe and ^{109}Cd





- Events rate $\sim$ 1.5 Me/s
- Hits rate $\sim$ 5.6 Mh/s
- Practically no ghosts reconstructed (below $3x10^{-3}$)

- Time resolution $\sigma_t \sim$ 12 ns
- Determined by the jitter of the input signals

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Conlusions

- First prototype GEMROC ASIC with a novel architecture has been designed and manufactured successfully
- Analogue parameters, gain, noise and offset spreads are as expected
- Time resolution of 12 ns rms has been achieved at input clock frequency of 125 MHz
- The electrical tests as well as the measurements performed for a test bench module have confirmed
  - correct functionality of all building blocks
  - compliance of the ASIC's parameters with the design specification
- Prototype Ethernet readout boards successfully implemented
  - Compact and easy to use solution
  - Provide up to 2 Gb/s data transfer rate

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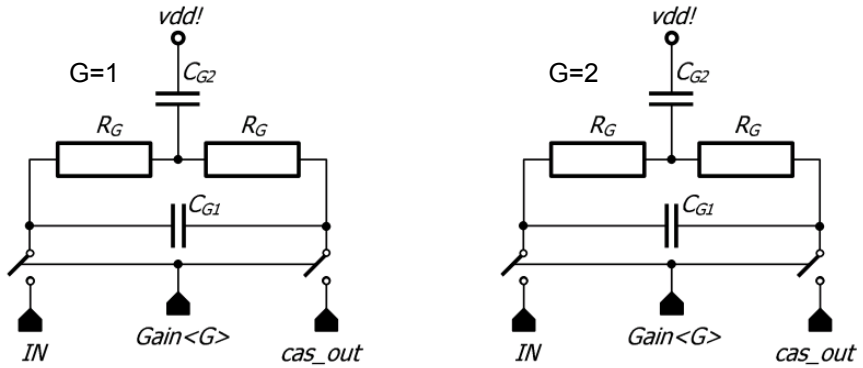
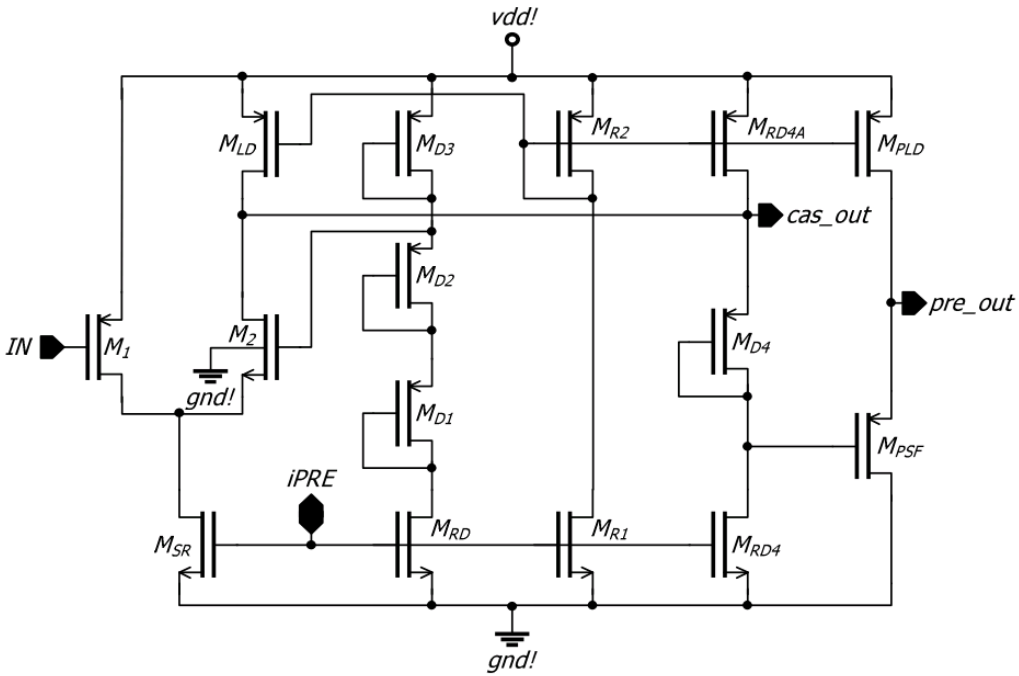
Thank you for your attention!

Preamplifier architecture

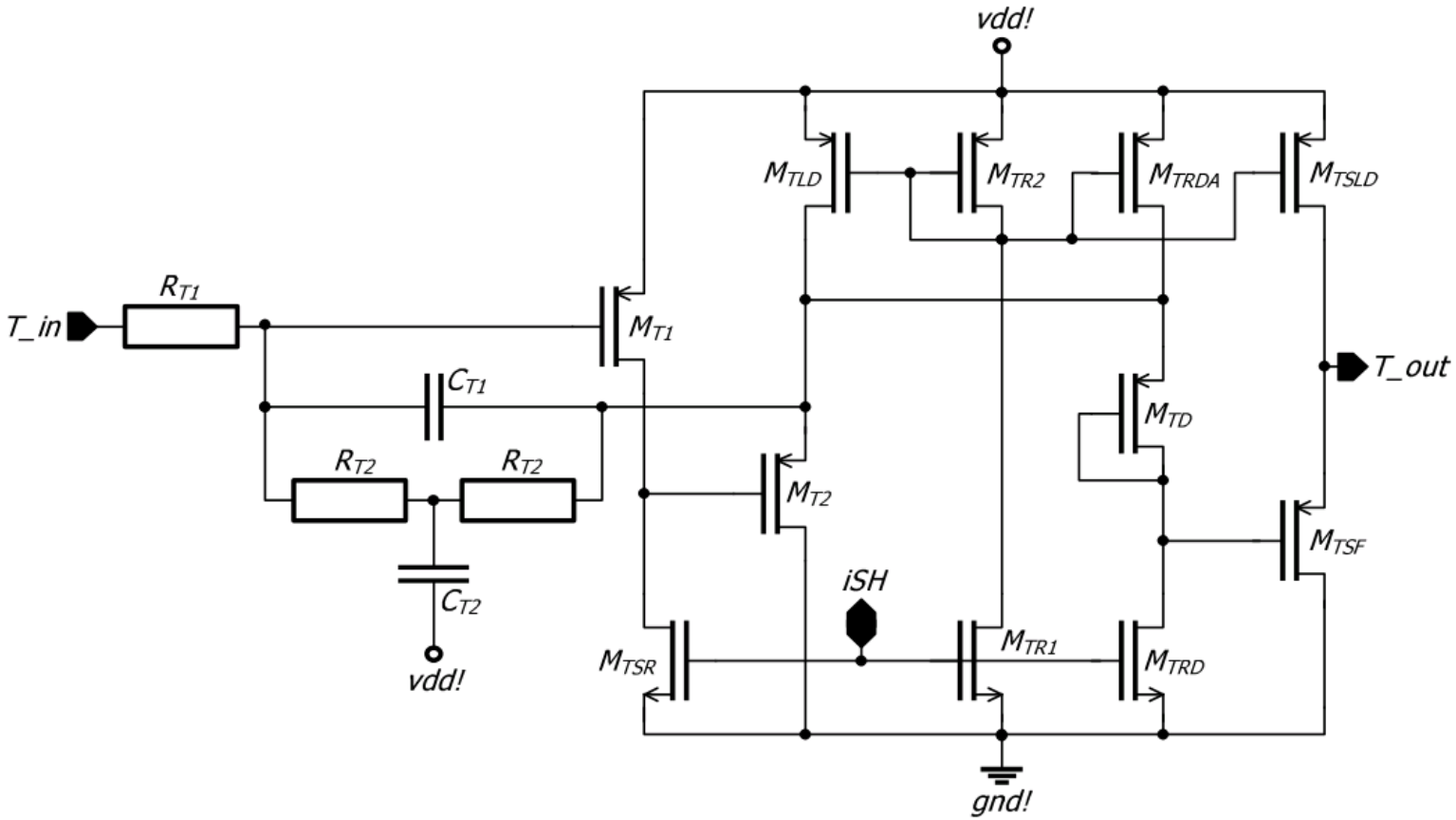
- Transimpedance preamplifier with T-type filter switchable feedback loop





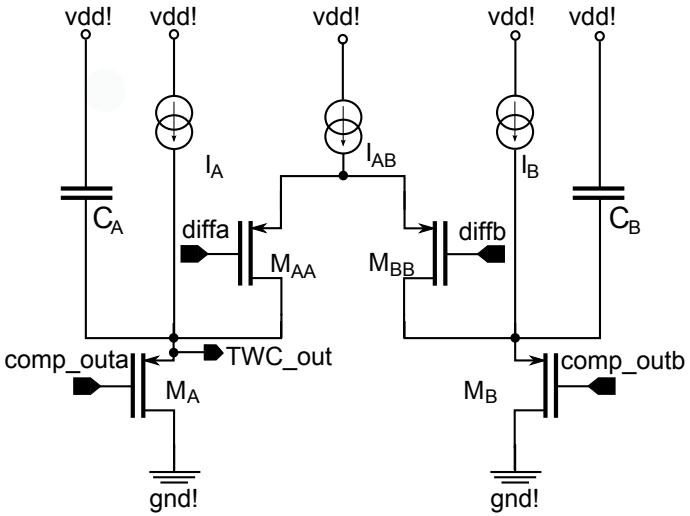
Shapers (SH) architecture

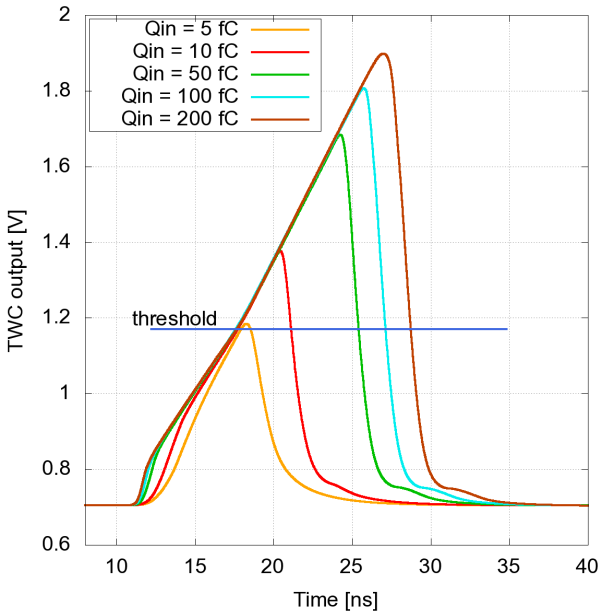
- FSH - one section ($T_p = 60ns$)
- SSH - two sections ($T_p = 100ns$)



Single section schematic view

Time Walk Compensation (TWC) Circuit





- Slows down the comparator output signals proportionally to the amplitudes of input pulses
- TWC output signals have almost the same slopes independently on the input signals
- Time-walk effect is reduced to few ns
- Currents I_A, I_B and I_{AB} are controlled by 6-bit DACs

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Peak Detect and Hold (PDH) Circuit

- The Peak Detect and Hold (PDH) circuit detects the peak of incoming signal and holds its value for a given period of time