A C-Card for Use with the BNL Peak-Finding ASIC

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Status

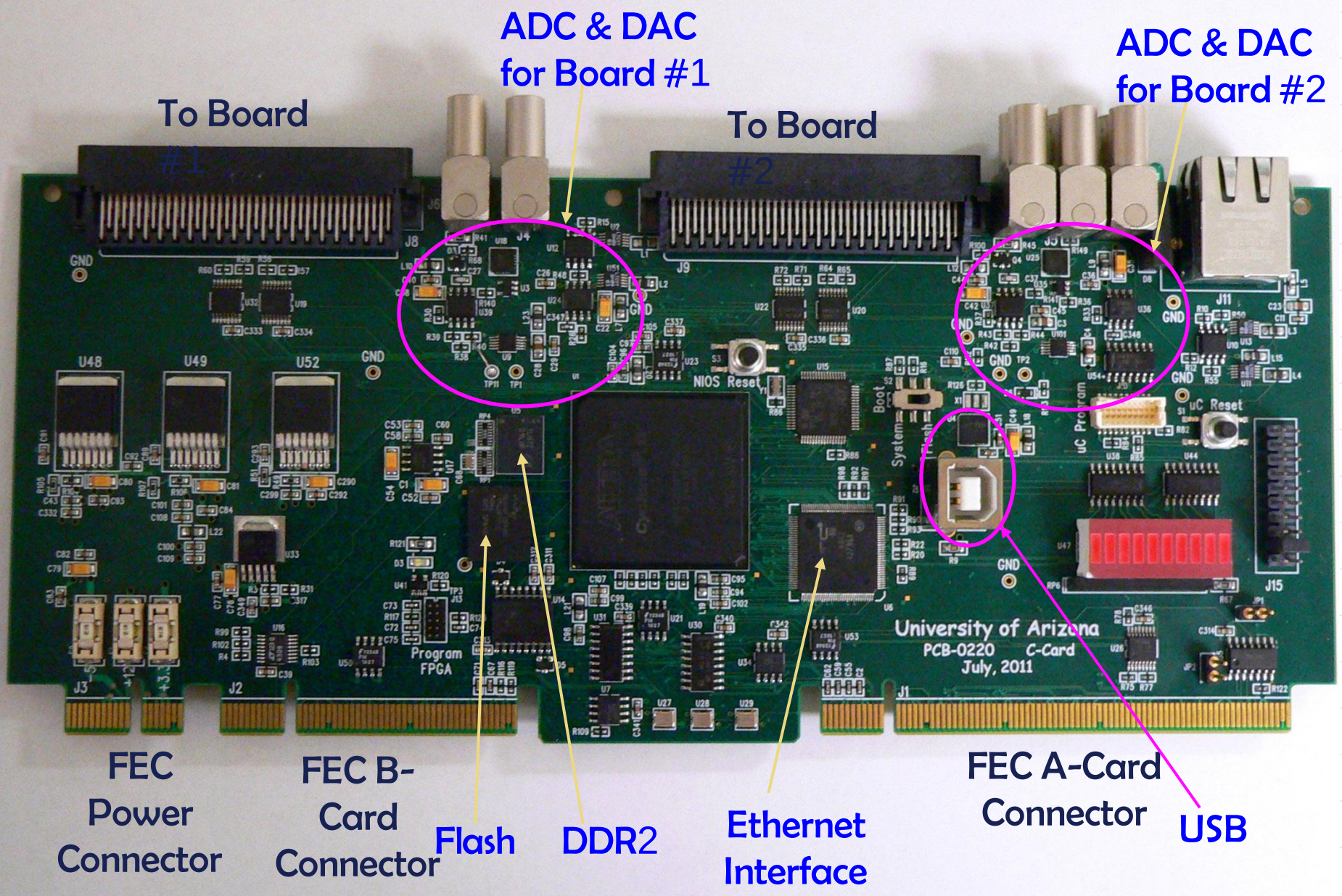
- A C-Card has been developed for use with both versions (V1 and V2) of the BNL peak-finding ASIC
- Communication with the FEC card to the MAMMA DAQ program has been successfully tested
- Communication with the V1 ASIC on its present front-end card is in progress
- Design of a front-end card for full-size Micromegas using V2 of the ASIC is in progress

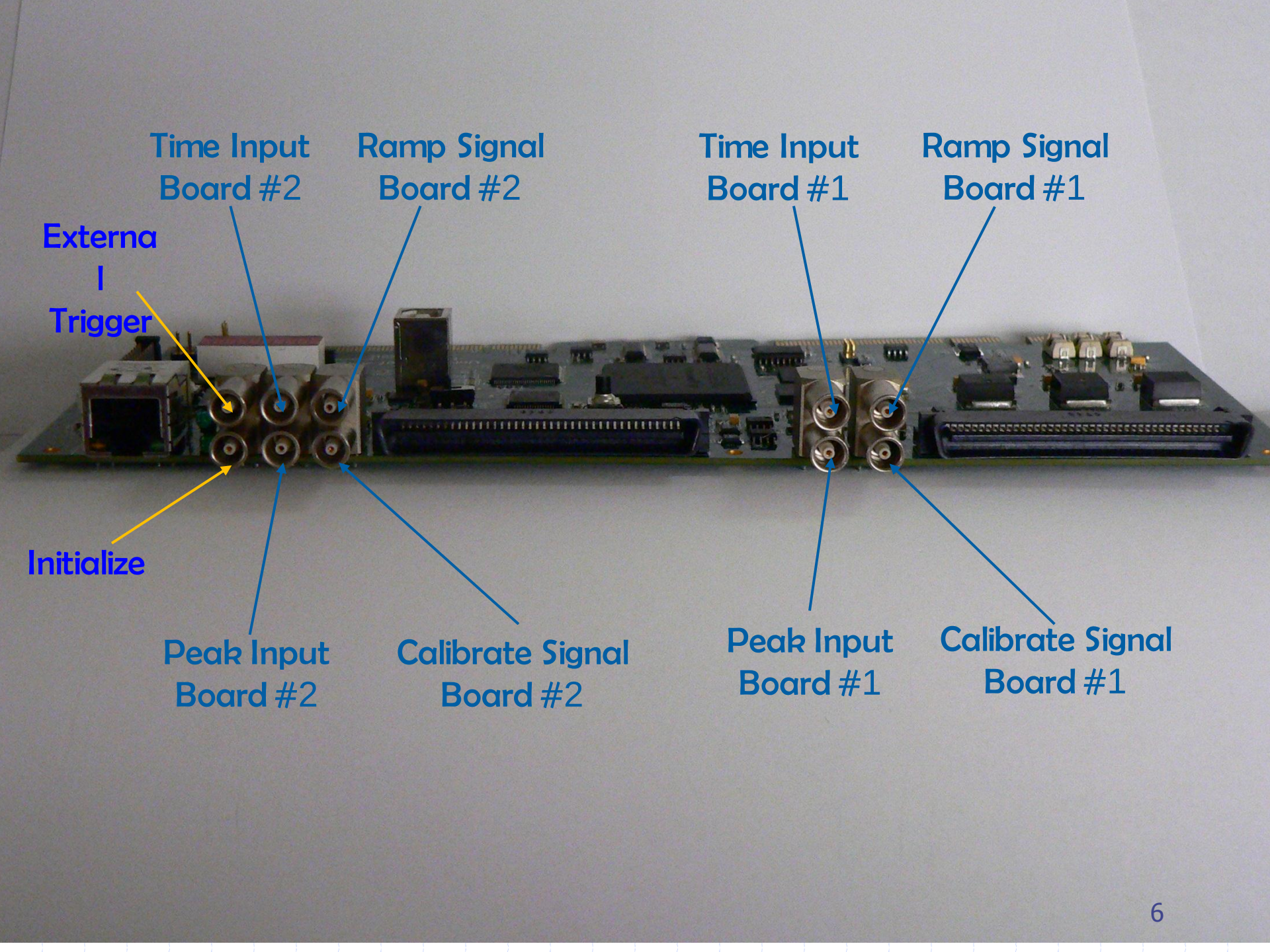
Features

- Connections to two BNL front-end cards via 2x80 pin ribbon cables
  - 8 LVDS inputs to C-Card
  - 16 LVDS I/O ports
- Connection to FEC card via card edge connectors
  - 4 LVDS inputs to C-Card
  - 21 LVDS outputs
  - 3 LVDS clocks to C-Card
  - 2 3.125 Gbps transceivers

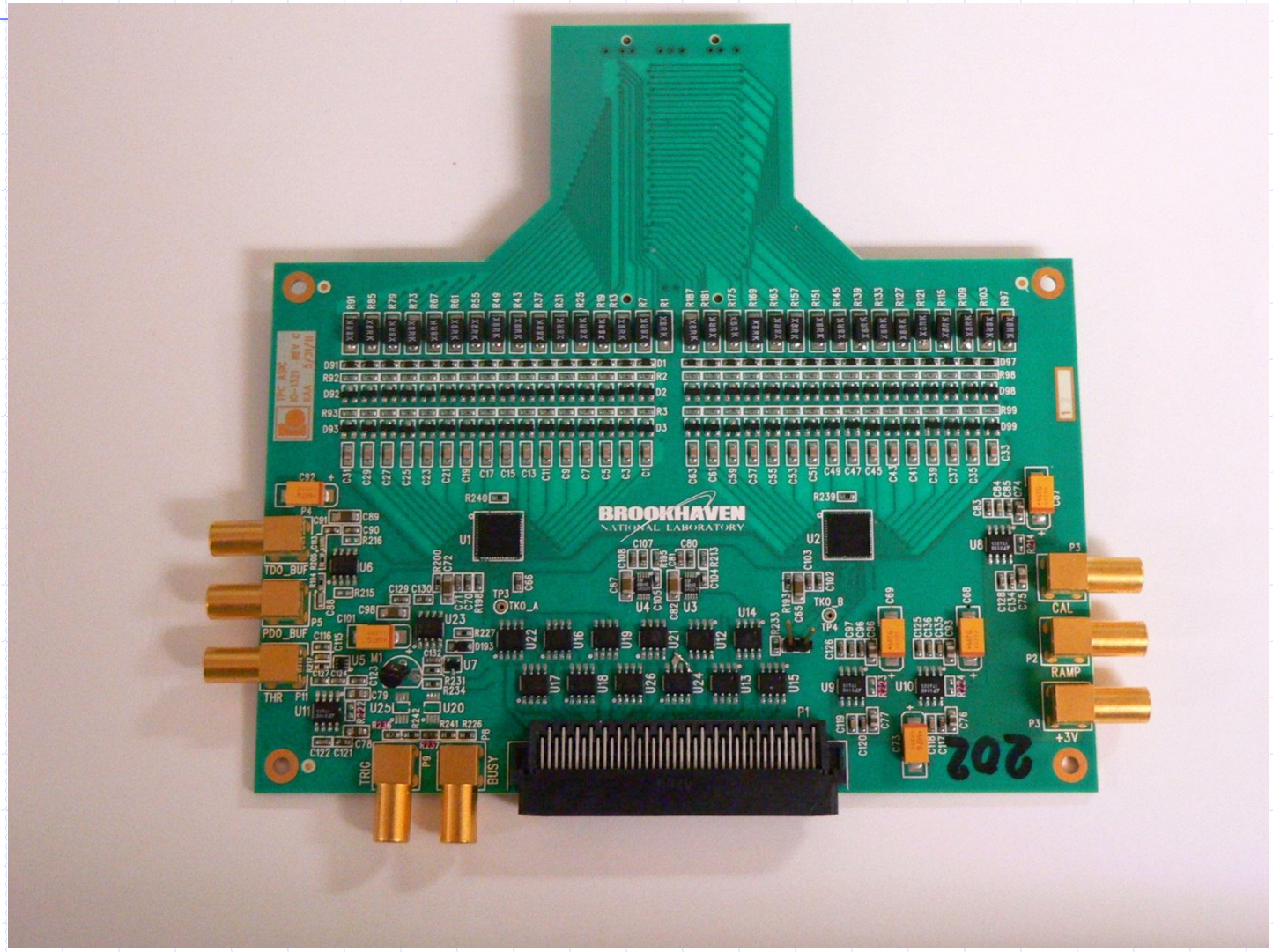
Features

- 10/100 Ethernet and USB connections
- 4 12 bit ADC's
- 4 16 bit DAC's
- 2 calibration pulse generators
- 2 ramp generators
- 2 FPGA clock regions from on-board oscillators or FEC


ADC & DAC
for Board #1
ADC & DAC
for Board #2
To Board
#1
To Board
#2
FEC
Power
Connector
FEC B-
Card
Connector
Flash
DDR2
Ethernet
Interface
FEC A-Card
Connector
USB
University of Arizona
PCB-0220 C-Card
July, 2011
NIOS Reset
uC Reset
Program
FPGA
J1
J2
J3


Time Input Board #2
Ramp Signal Board #2
Time Input Board #1
Ramp Signal Board #1
External Trigger
Initialize
Peak Input Board #2
Calibrate Signal Board #2
Peak Input Board #1
Calibrate Signal Board #1

Front-End Card with V1 BNL ASICS



Testing With FEC

Testing with FEC

- Preprogrammed events of varying lengths and time intervals were sent to the FEC
- Sorin Martoiu wrote FEC firmware for FIFO receive and UDP packet creation
- Validated with MAMMA DAQ program using simple event prints

Future Work

- Continue commissioning of C-Card with V1 BNL ASIC
- Prepare for commissioning of C-Card with V2 BNL ASIC
- Continue design of front-end card for full-size MM with V2 BNL ASIC