The VMM1 Front End IC for the ATLAS Muon Phase1 Upgrade

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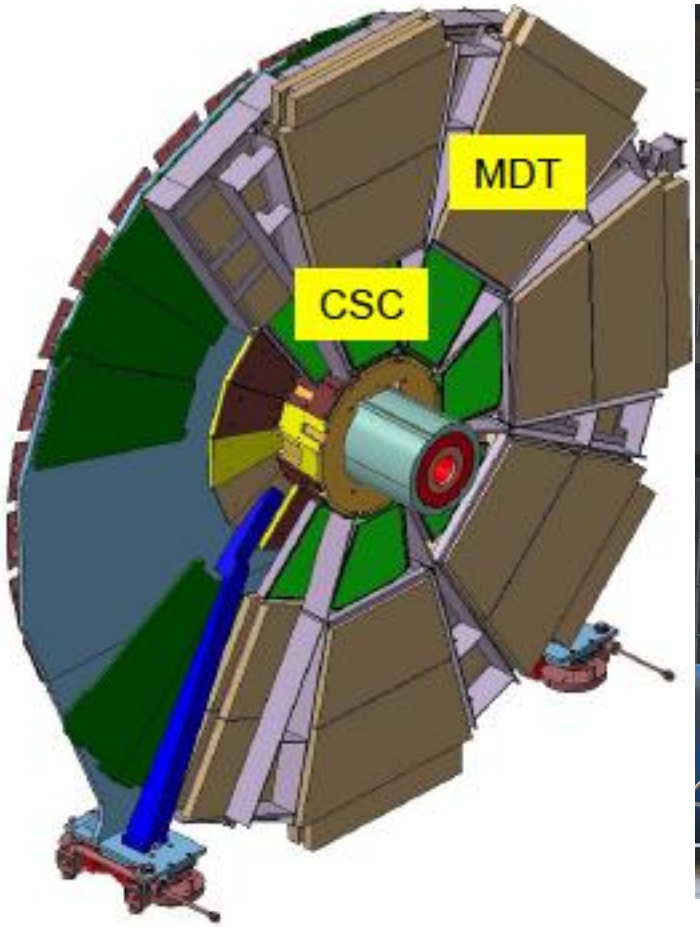
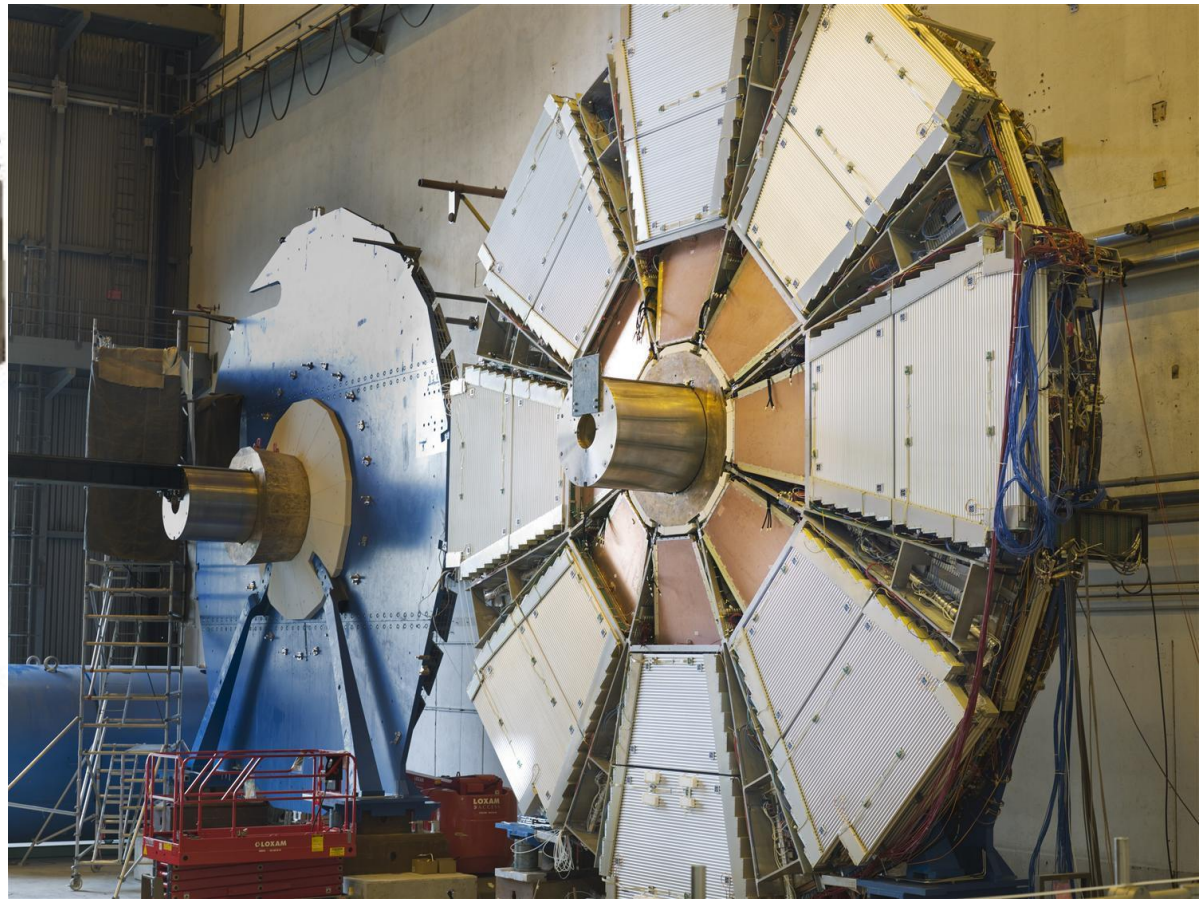
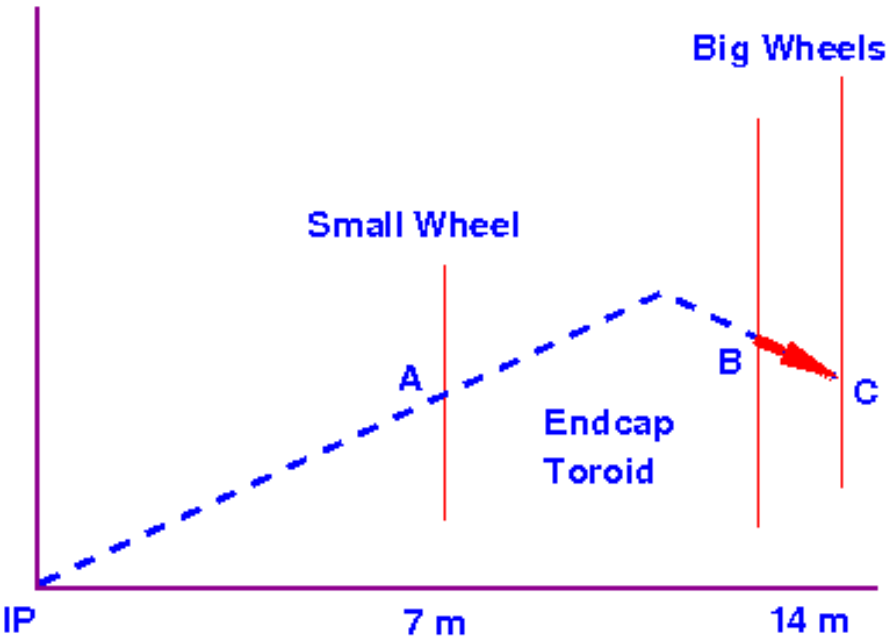
The Present "Small Wheels" (9m Diameter)

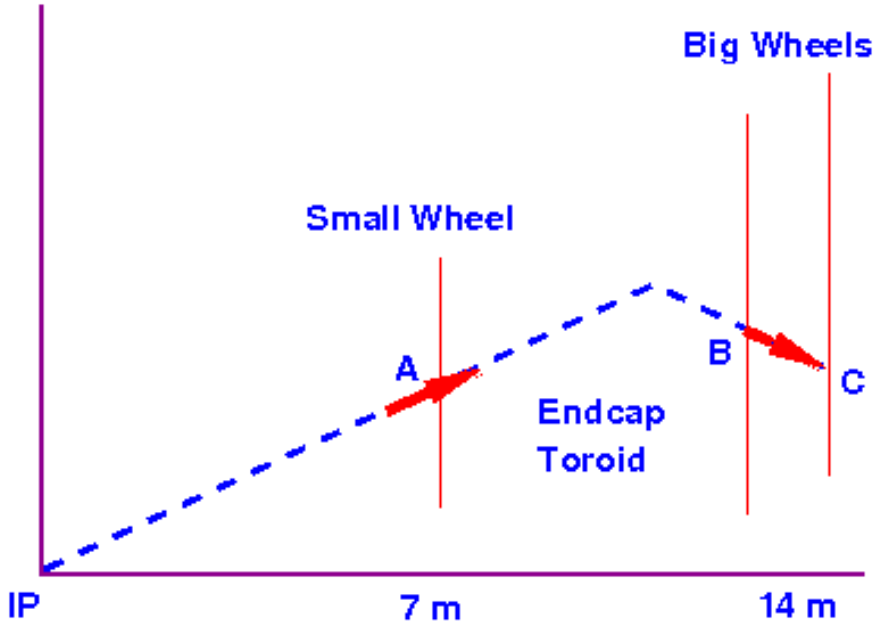




- Need New Detectors that participate in the Level1 Trigger by providing a vector with ~1 mrad resolution
- Need to handle considerably higher rates at L = 5x10e34

The Problem with High pT Triggers





Current Endcap Trigger

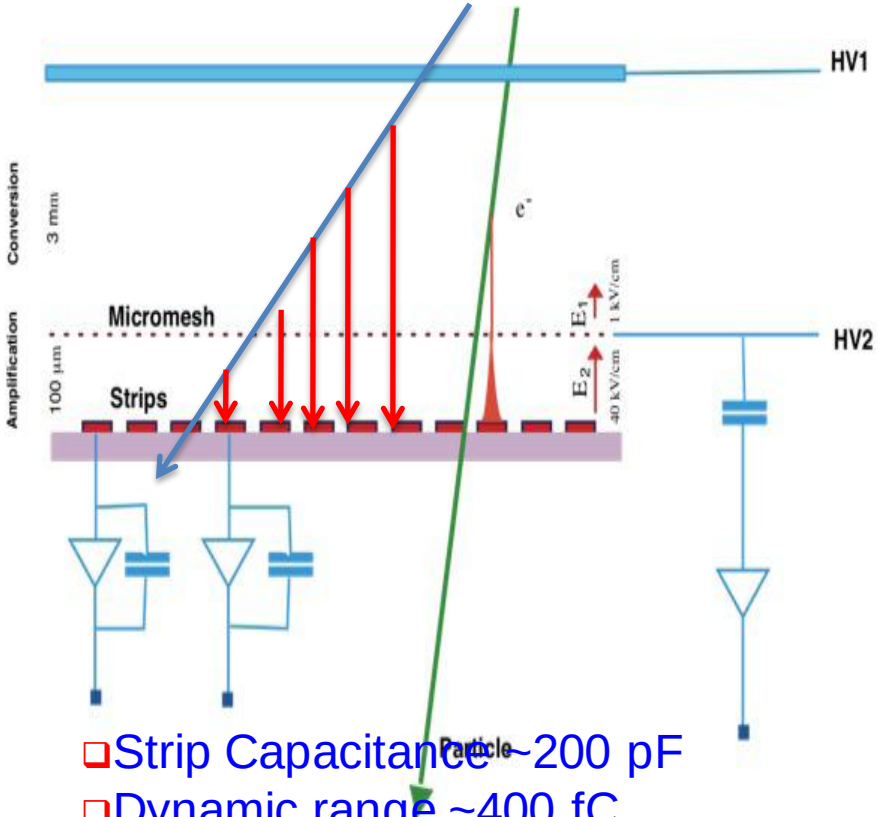
- Only a vector BC at the Big Wheels is measured
- Momentum defined by implicit assumption that track originated at IP
- Random background tracks can easily fake this

Proposed Trigger

- Provide vector A at Small Wheel
- Powerful constraint for real tracks
- With pointing resolution of 1 mrad it will also improve pT resolution
- Currently 96% of High pT triggers have no track associated with them

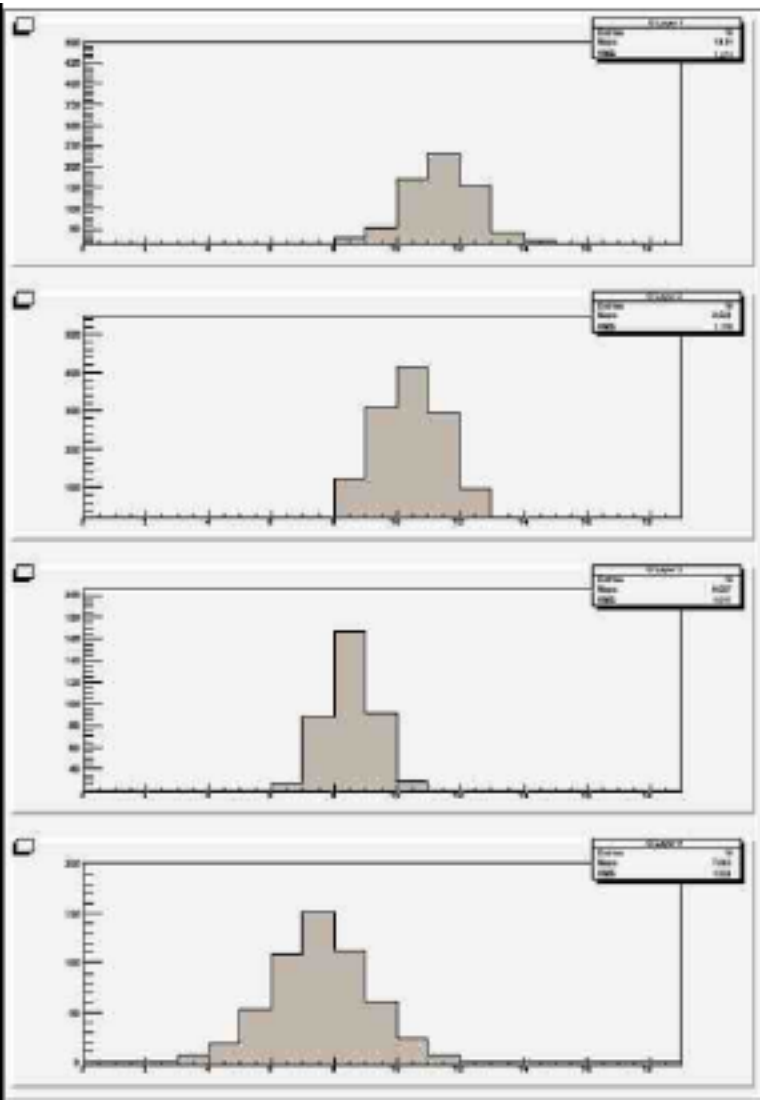
The Micromegas Option and what is required from the Front End

- Operation in" micro-TPC mode"
  - Precision for near normal tracks can be achieved by charge interpolation
  - Resolution degrades ~tanΘ
  - Larger incidence angle tracks are reconstructed using time measutements
- Signal Processing requirements
  - Charge measurement for precision charge interpolation (a la CSC)
  - Time measurement with resolution of ~2 ns for the micro-TPC mode appropriate for large incidence angles
  - At Trigger level use address of earliest arrival of charge above a set threshold



- Strip Capacitance ~200 pF
- Dynamic range ~400 fC
- Integration Time 50-100 ns
- Amplitude and time measurement
- Trigger

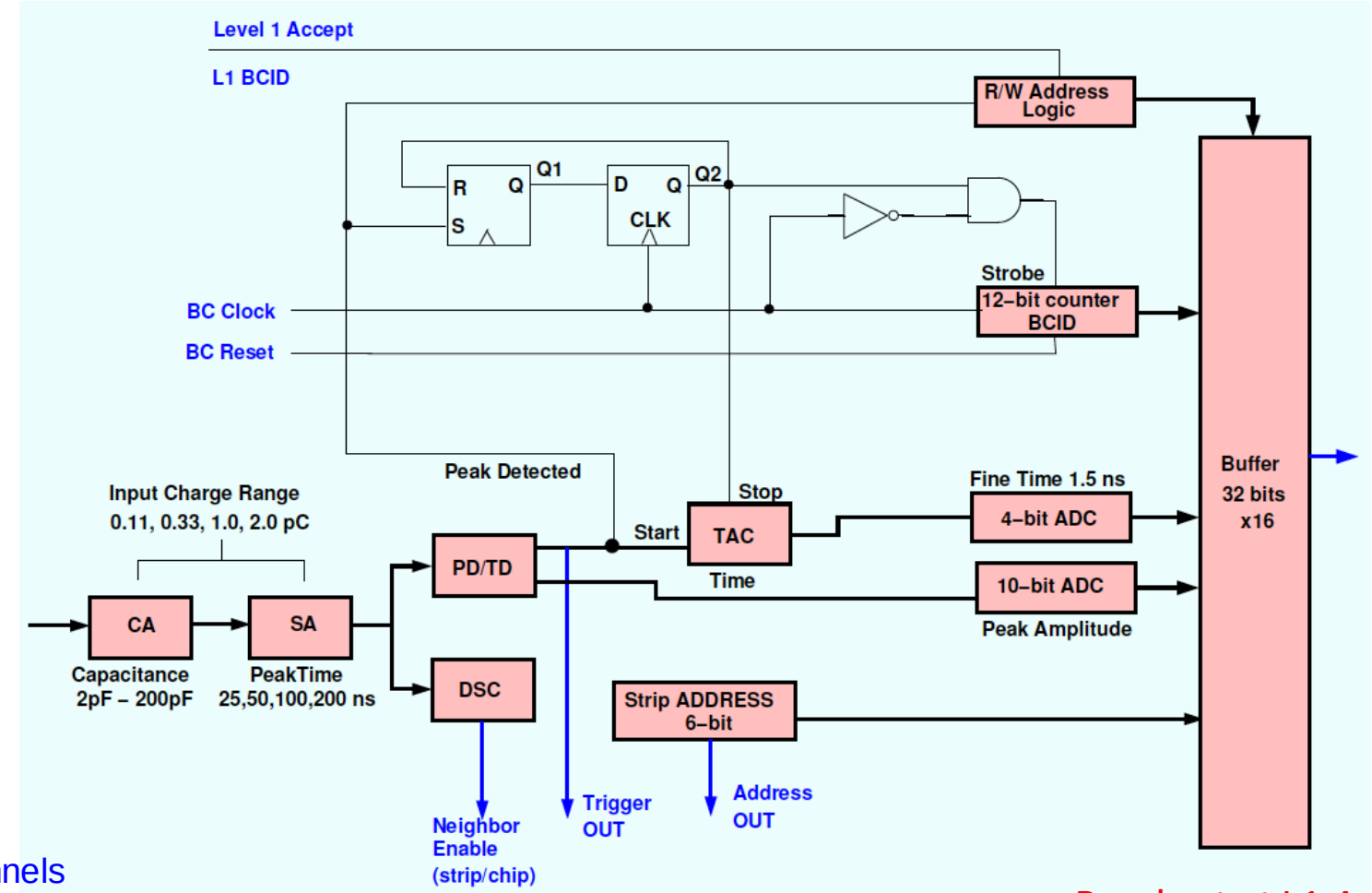
Front End Requirements for the TGC Option



- Determine Position by charge interpolation
- Less sensitive to tanΘ degradation due to near saturated gas gain
- Precision measurement in response to Level 1 accept can be identical to the μ-megas option
- For Trigger, use Discriminator outputs and Time-over-threshold as a measure of charge

- Strip Capacitance ~200-300 pF
- Dynamic Range ~2 pC
- Integration time 25 ns
- LVDS outputs of ALL channels in parallel

Block Diagram of the IC being designed

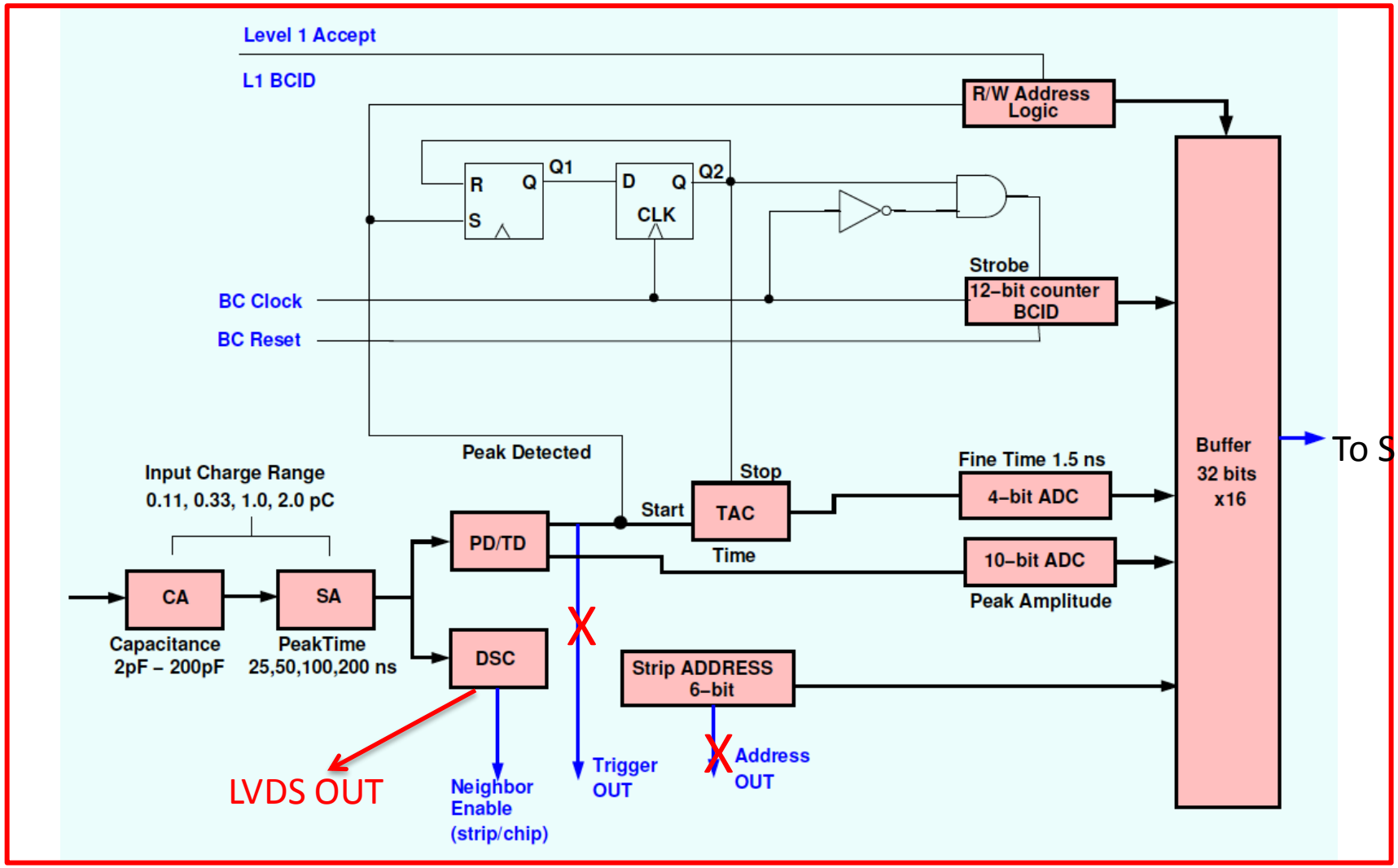


To SRS

- 64 channels
- adj. polarity, adj. gain (0.11 to 2 pC), adj. peaking time (25-200 ns)
- derandomizing peak detection (10-bit) and time detection (1.5 ns)
- real-time event peak trigger and address
- integrated threshold with trimming, sub-threshold neighbor acquisition
- integrated pulse generator and calibration circuits
- analog monitor, channel mask, temperature sensor
- continuous measurement and readout, derandomizing FIFO
- few mW per channel, chip-to-chip (neighbor) communication, LVDS interface

Readout at L1 Accept
No Problem
Zero-suppressed, already digitized, much of DAQ already on Front End IC

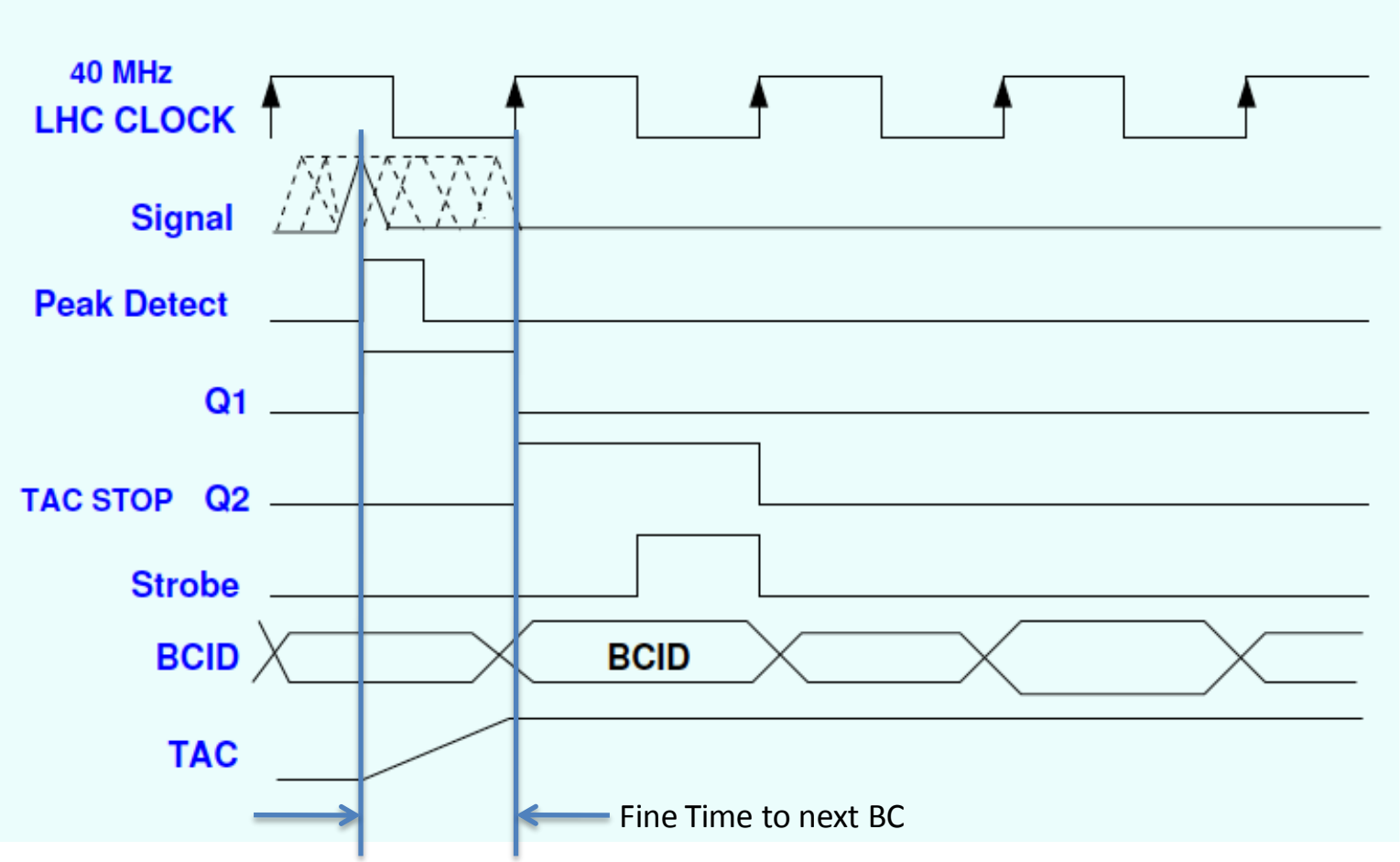
For a TGC-based Trigger/DAQSystem



For TGC there will be fewer (16 or 32) channels with LVDS outputs of individual discriminators

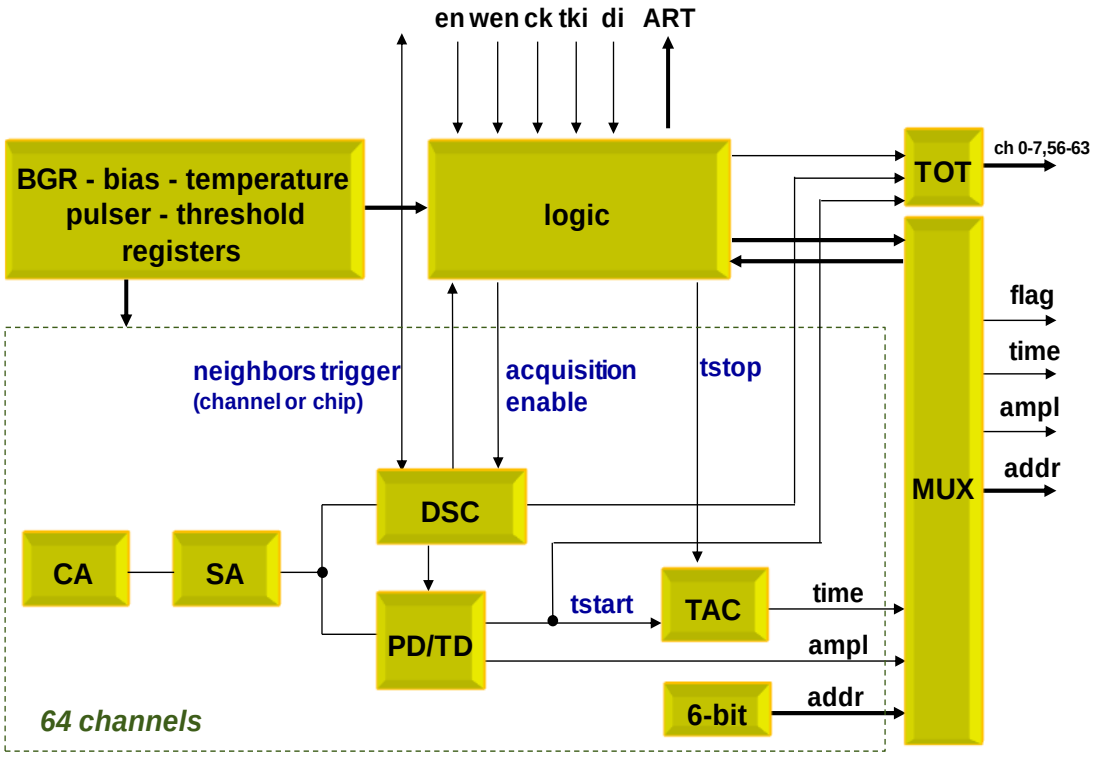
All other features remain the same

Timing Diagram



40 MHz BC clock convenient for LHC but any clock can be used to related hit with trigger accept

Operation and functions



Functions

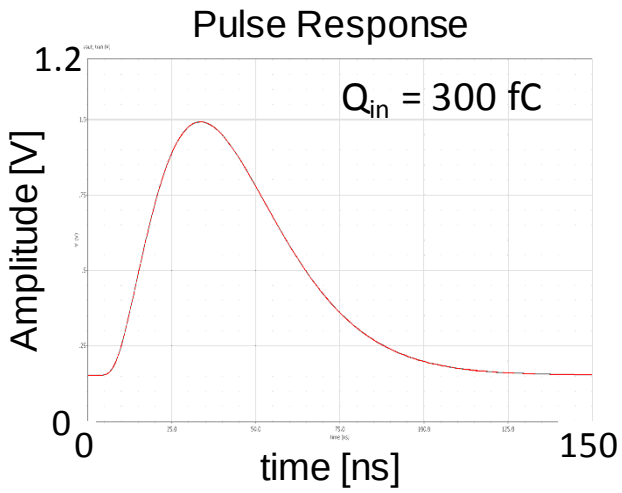
- common
  - temperature monitor
  - pulse generator (10-bit adjustable amplitude)
  - coarse threshold (10-bit adjustable)
  - self-reset option
  - analog monitors
    - analog, trim thresholds, BGR, DACs, temp.
    - analog buffers
- analog section
  - charge amplifier (200pF), high-order DDF shaper
  - adjustable polarity (negative, positive)
  - gain: 0.5, 1, 3, 9 mV/fC (2, 1, 0.33, 0.11 pC)
  - peaktime: 25, 50, 100, 200 ns
  - test capacitor, channel mask
- discriminator
  - trimmer (4-bit adjustable, 1mV)
  - sub-hysteresis pulse processing option
  - neighbor logic on channels and chips (ch0, ch63)
- peak detector multiphase
- time detector
  - TAC ramp (selectable 100, 200, 500, 1000 ns)
  - start at peak-found
  - stop selectable (ena-low or stp-low)
- ART
  - address of the first event in real time
  - selectable at first threshold or at first peak
  - self-resets in 40ns
  - fflag indicates event
  - address available at fa0-fa5
- timing per channel
  - available for channels 0-7 and 56-63
  - selectable between ToT and TtP
- readout
  - flag at first peak indicates events to readout
  - sparse with smart token passing (skips empty chan.)
  - amplitude available at pdo
  - timing available at tdo
  - address available at a0-a5

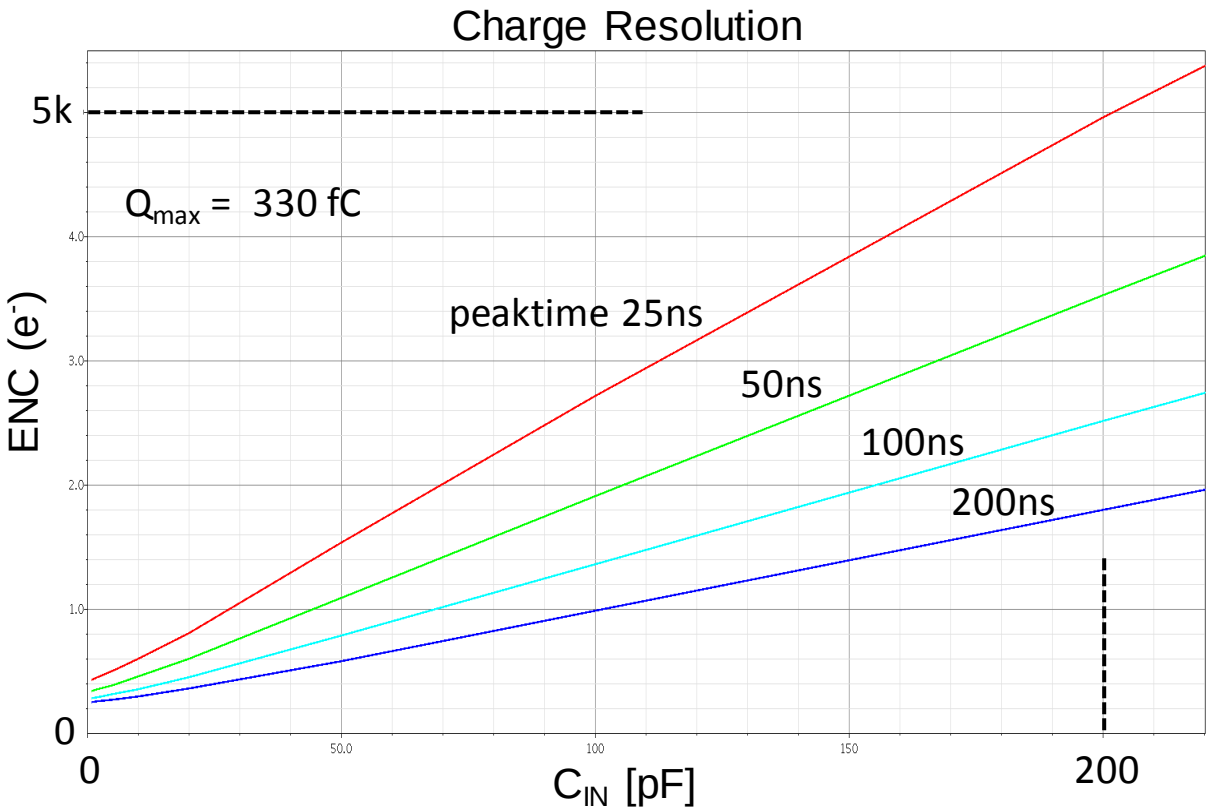
Modes of operation

- acquisition: events are detected and processed (amplitude and timing)
  - charge amplification, discrimination, peak- and time-detection
  - address in real time (ART) of the first event
  - direct timing (ToT or TtP) per channel for channels 0-7 and 56-63
- readout: sparse mode with smart token passing (amplitude, timing, addr.)
- configuration: access to global and channel registers

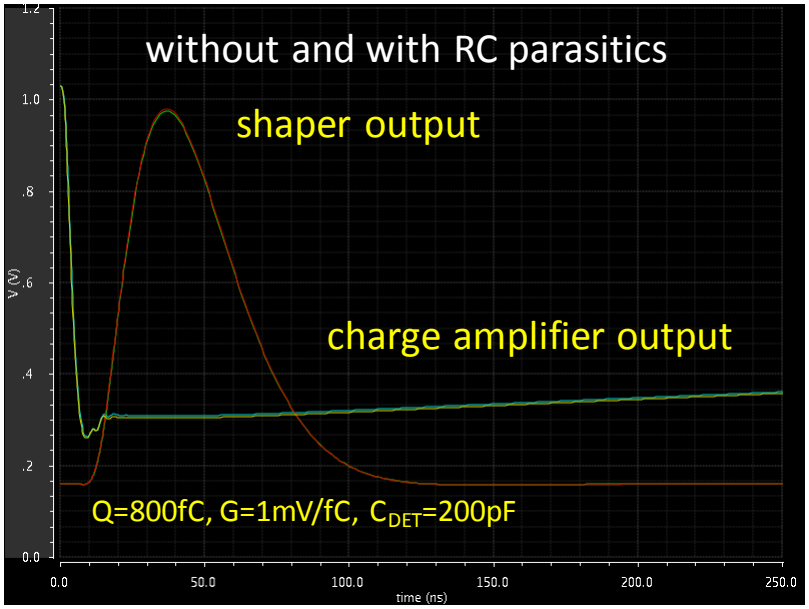
VMM1 IC SPICE Simulation performance

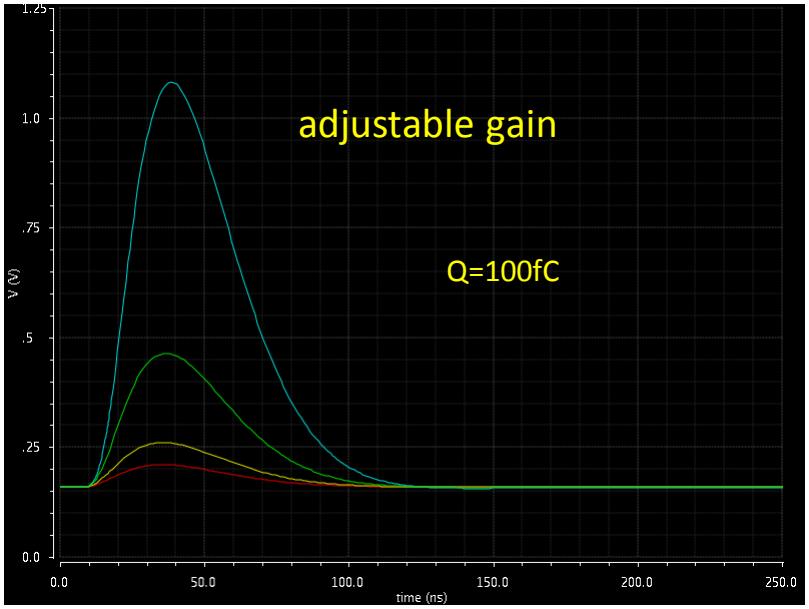
Analog section:
transistor-level simulations
power ≈ 4 mW

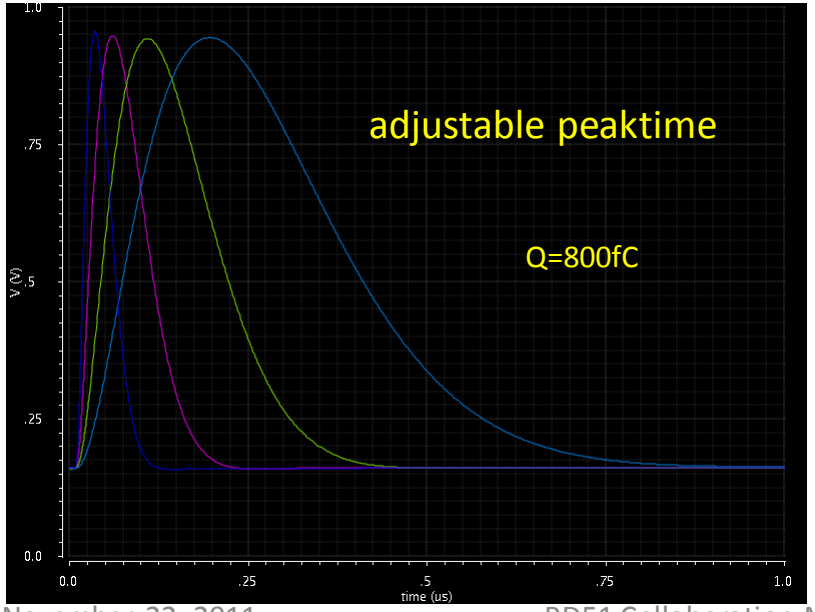


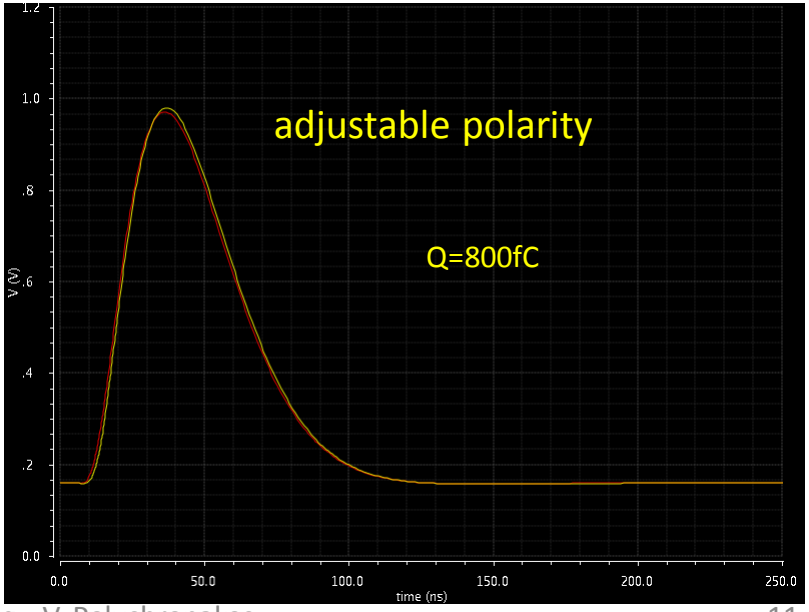


Analog section - simulations 2/2



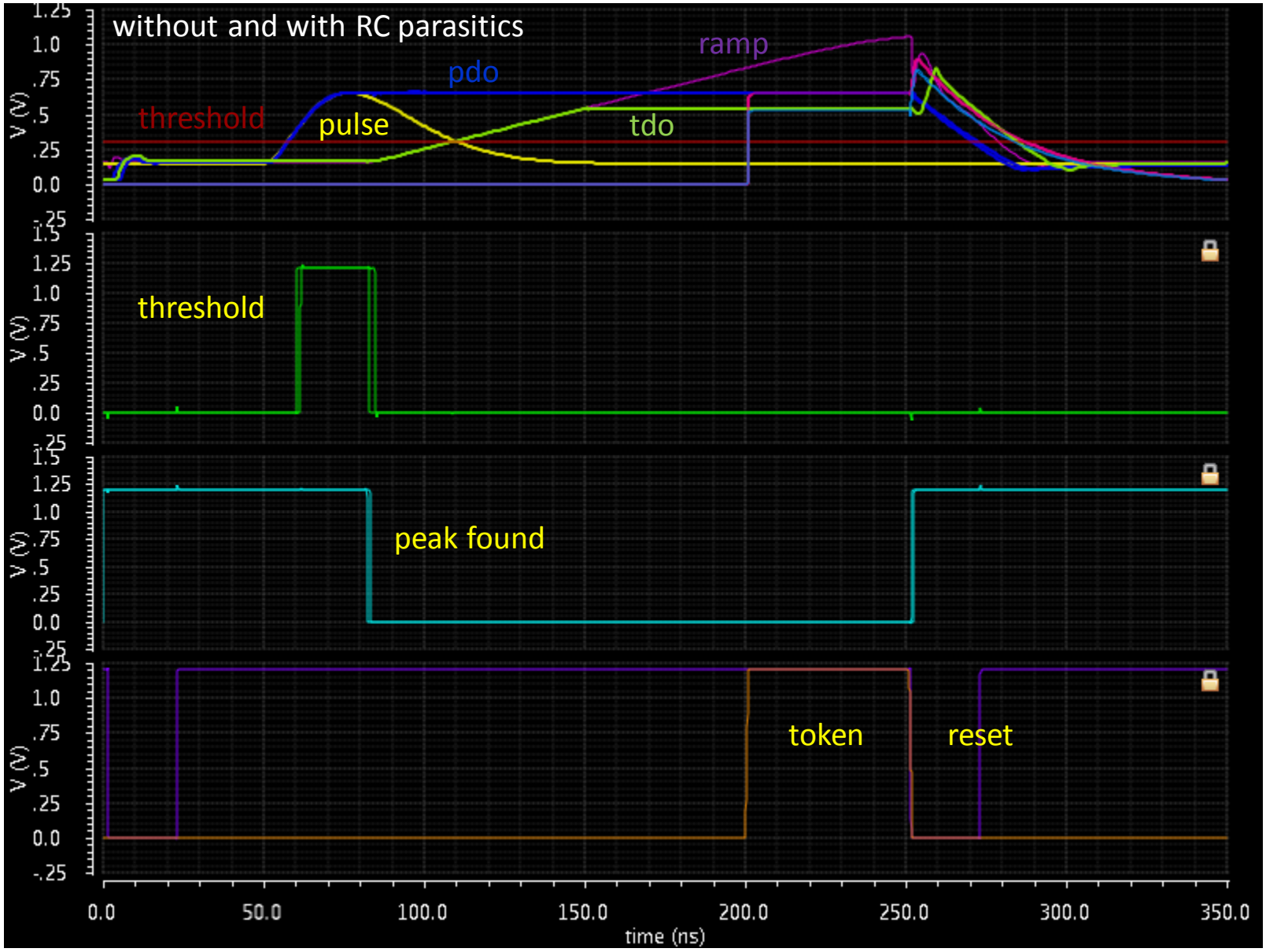






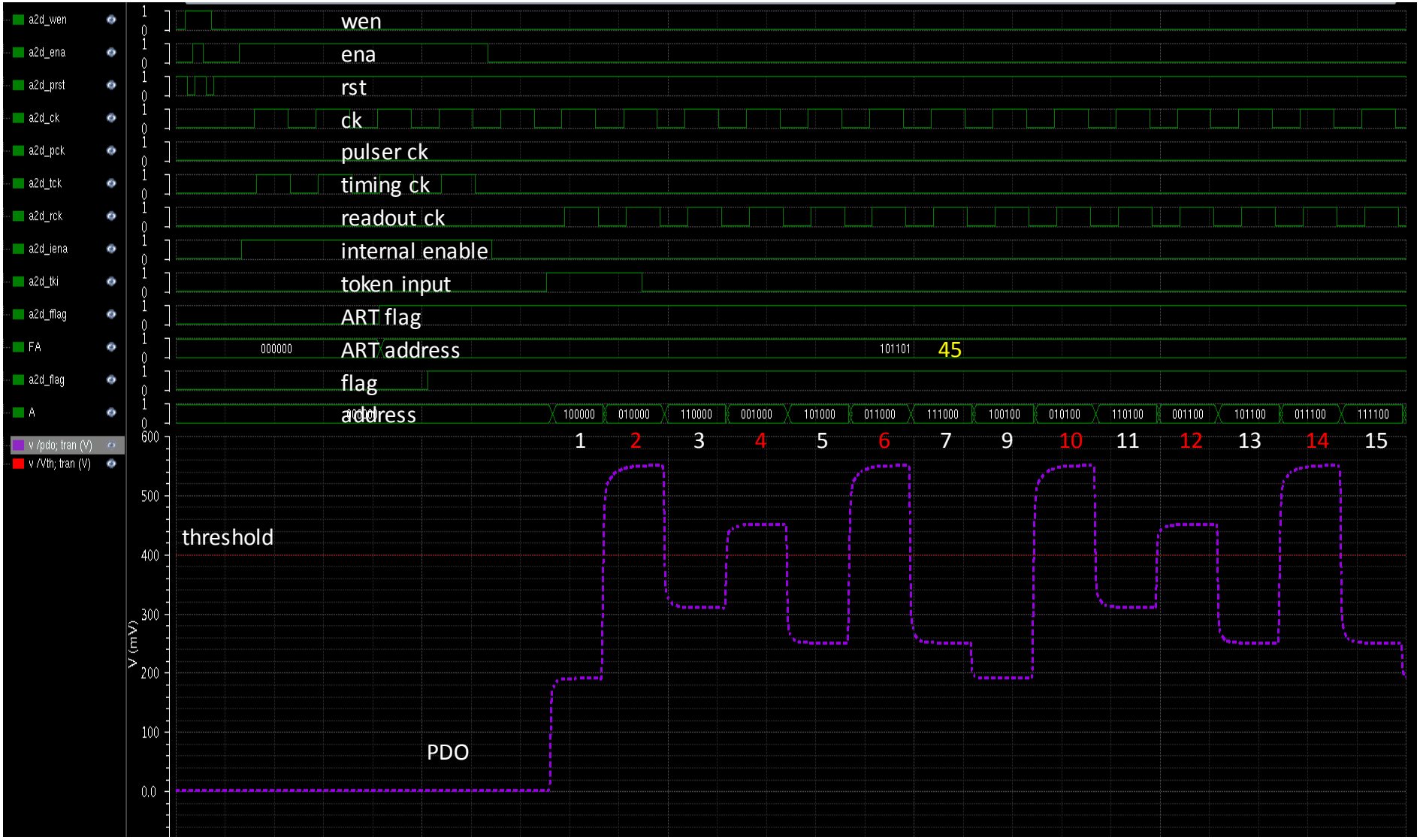
Performance of Peak Detector for Different Amplitudes

Peak and time detectors - simulations



TAC stop signal at 150ns (not visible); timing at peak found (low time walk)

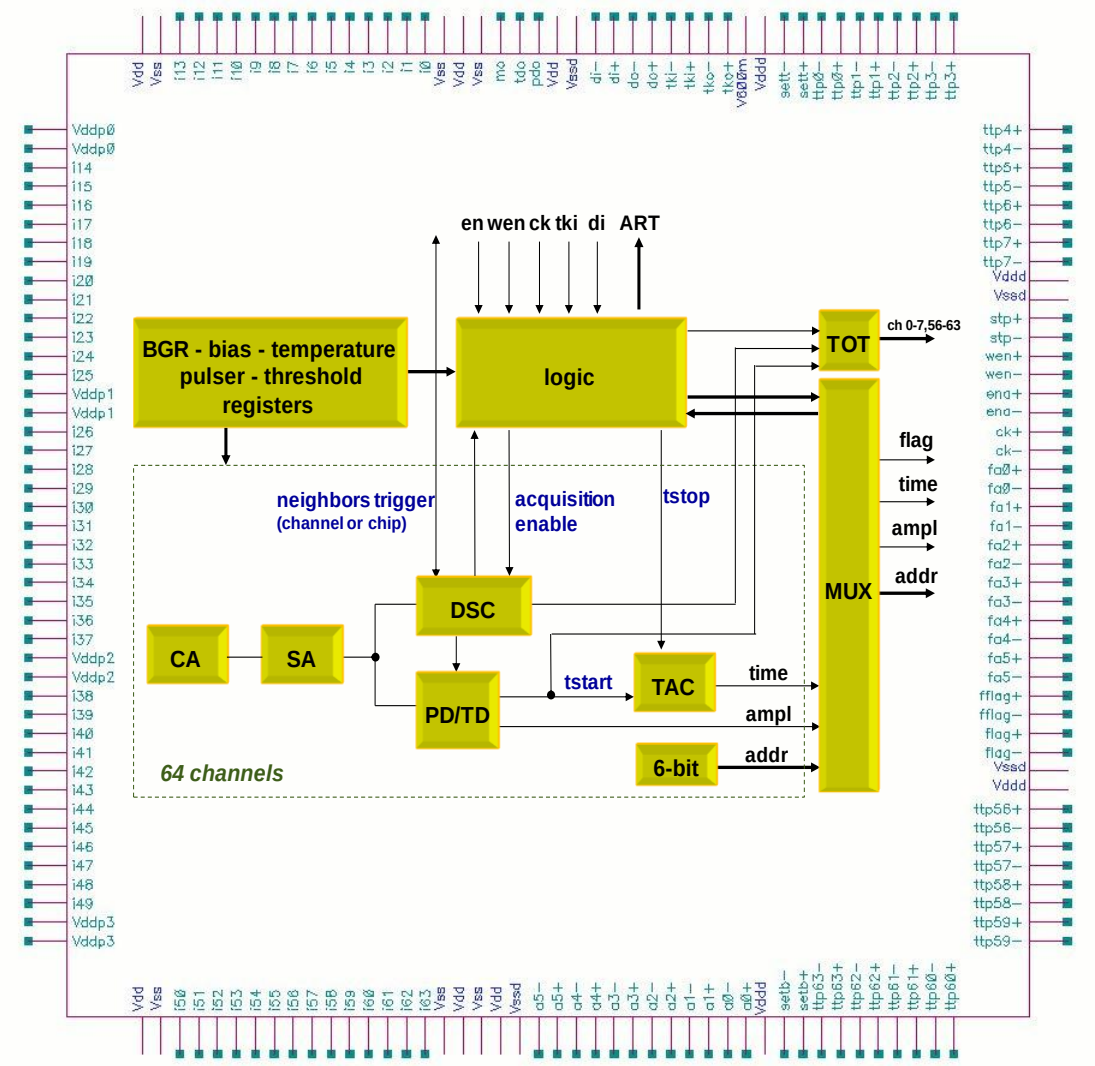
System-level simulations 2/2



channels 2, 4, 6, 10, 12, 14 exceed threshold; neighbors are collected

channel 45 hits 2 ns earlier than others (ART)

Pinout



Pinout

- 176 pins (44 each side)
- Vdd,Vss: analog supplies 1.2V and grounds 0V
- Vddd, Vssd: digital supplies 1.2V and grounds 0V
- Vddp0-Vddp3: charge amplifier supplies 1.2V
- V600m: reference for LVDS 600mV

- i0-i63: analog inputs, ESD protected
- mo: monitor multiplexed analog output
- pdo: peak detector multiplexed analog output
- tdo: time detector multiplexed analog output

- flag: event indicator
- a0-a5: multiplexed address, tristated (driven with token)
- ttp0-ttp7 and ttp56-ttp63: ToT or TtP

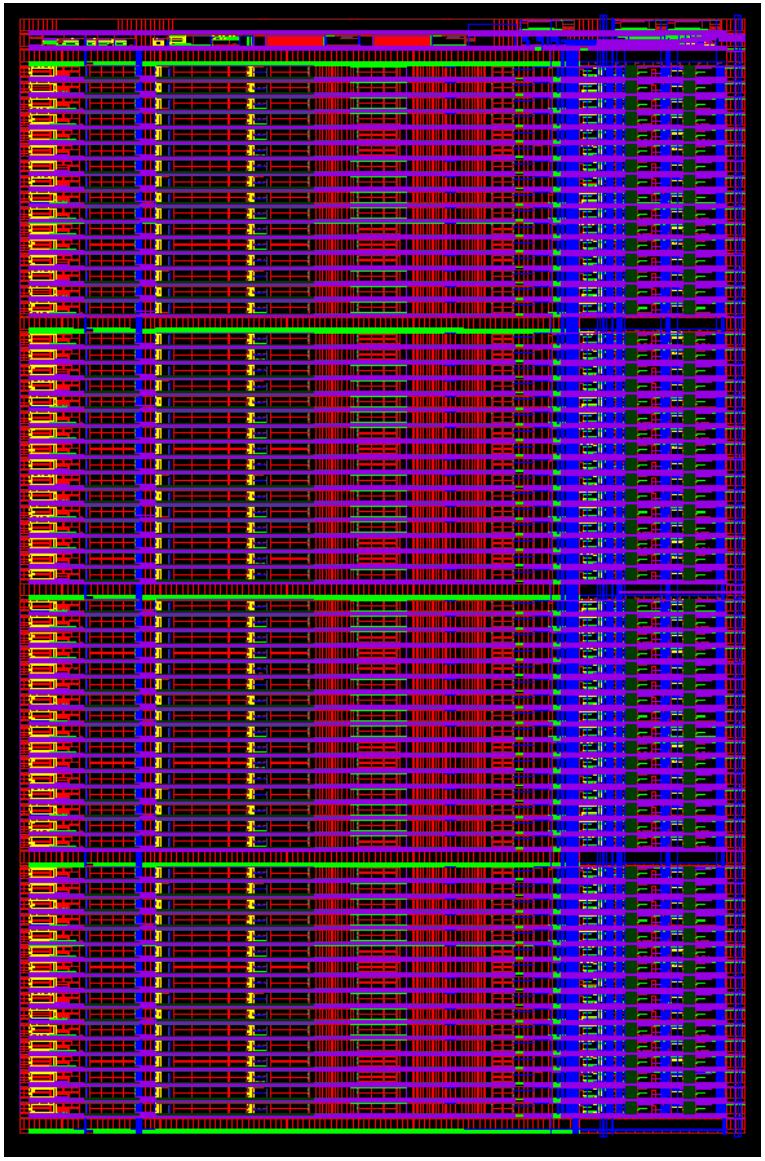
- fflag: ART event indicator
- fa0-fa5: ART address output

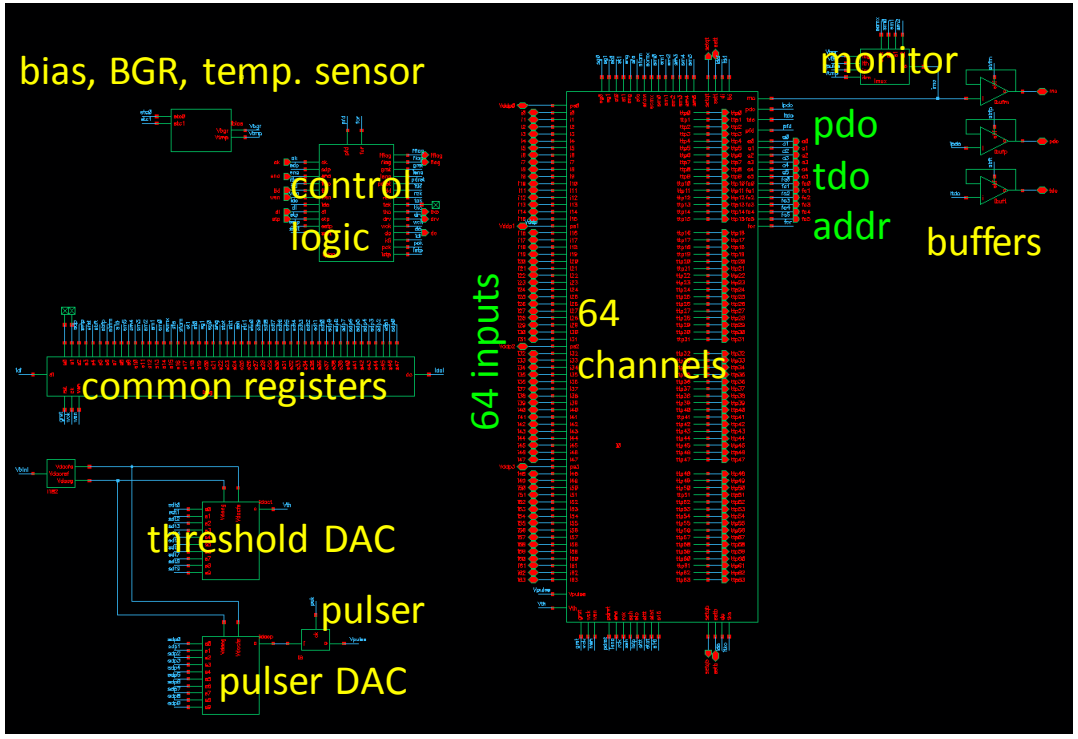
- stp: timing stop
- sett, setb: ch0, ch63 neighbor chip triggers (bi-directional)

- ena: acquisition enable
  - ena high, wen low: acquisition mode
  - ena low, wen low: readout mode
  - ena pulse, wen high: global reset
- wen: configuration enable
  - wen high: configuration mode
  - wen pulse: acquisition reset
- ck: clock
  - in acquisition mode ck is counter clock
  - in readout mode ck is readout clock
  - in configuration mode ck is writein clock

- tki, tko: token input and output (3/2 clock wider)
- di, do: data configuration input and output (1/2 clock shifted)
  - in acquisition mode di is pulser clock

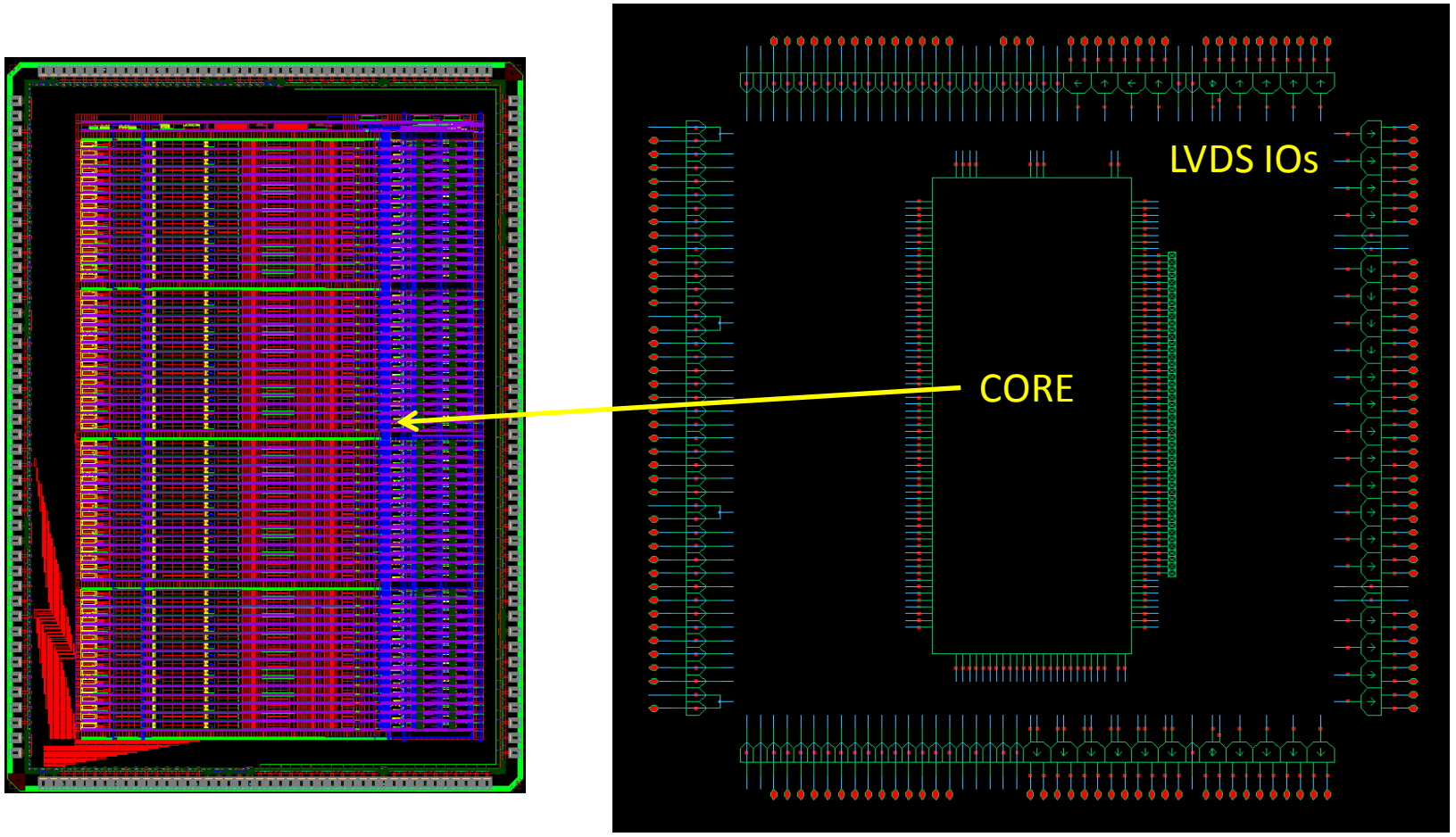
Core





- size 4.7 mm x 7.1 mm
- five banks of MOSCAP filters on bias lines
- power dissipation ~ 300 mW

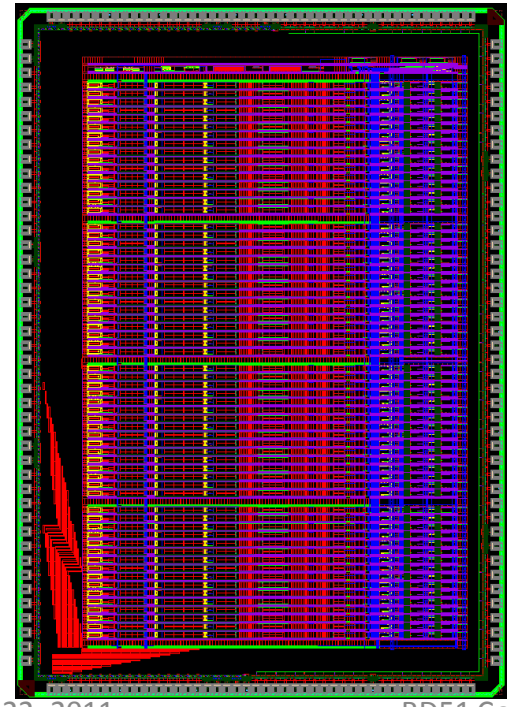
Top level



- size 5.9 mm x 8.4 mm

Schedule and status

	scheduled	completed
Analog section	Jan 2011	February 2011
Peak/time section	March	April
Common circuitry	April	May
Digital sections	May	July
Physical layout	July	October
Fabrication	September	**Queued for November 7th**



- technology IBM 8RF CMOS 130 nm
- size 5.9 mm x 8.4 mm (~50mm²)
- pads count 176, package LQFP 176
- fabrication cost (MPW MOSIS) ~ $150k
- next available runs:
  - November 7th, 2011
  - February 6th, 2012

Latest News: Prototypes to be shipped February 27

Summary

- VMM1 first version of front end IC for the Muon New Small Wheels
- Data driven, peak and amplitude detection, on-chip ADC and derandomizing buffers result in efficient DAQ with low data volume (essentially a “DAQ in a chip”)
- Prototype has all Basic Functionality for both μ–Megas and TGC
- Has all 64 channels (16 for the TGC option) as required for the final version
- This is important for demonstrating the critical trigger functions
- Production expected 2014(?)

Extra Slides