FDF

Cologne Chip

# GateMate™ FPGA

## A European 28nm FPGA with an Open-Source Toolchain and Radiation Qualification Results


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# Company Overview

1994 Founding year of **Cologne Chip Designs GmbH**

1996 Presentation of world's first single-chip-solution for ISDN

2000 Rebranding to **Cologne Chip AG** and sales in millions of units after annual growth rates by 100%

2007 Establishment of the **XHFC-Series** with open access to drivers and software; part of Linux Kernel since v. 2.6.27

2012

2020 Introduction of a new product line: **GateMate FPGA**


**> 30 Years**

Experience in Semiconductor Business

Certified Quality

**100 %**

Same-Day Deliveries from stock in Cologne

designed and manufactured in Germany

Reliable Supply Chain

# Agenda

1. Introduction to GateMate FPGA

   Architecture & Toolchain, Available Boards

2. Toolchain Hands-on

   Simulation, Synthesis, Implementation, Run Hardware

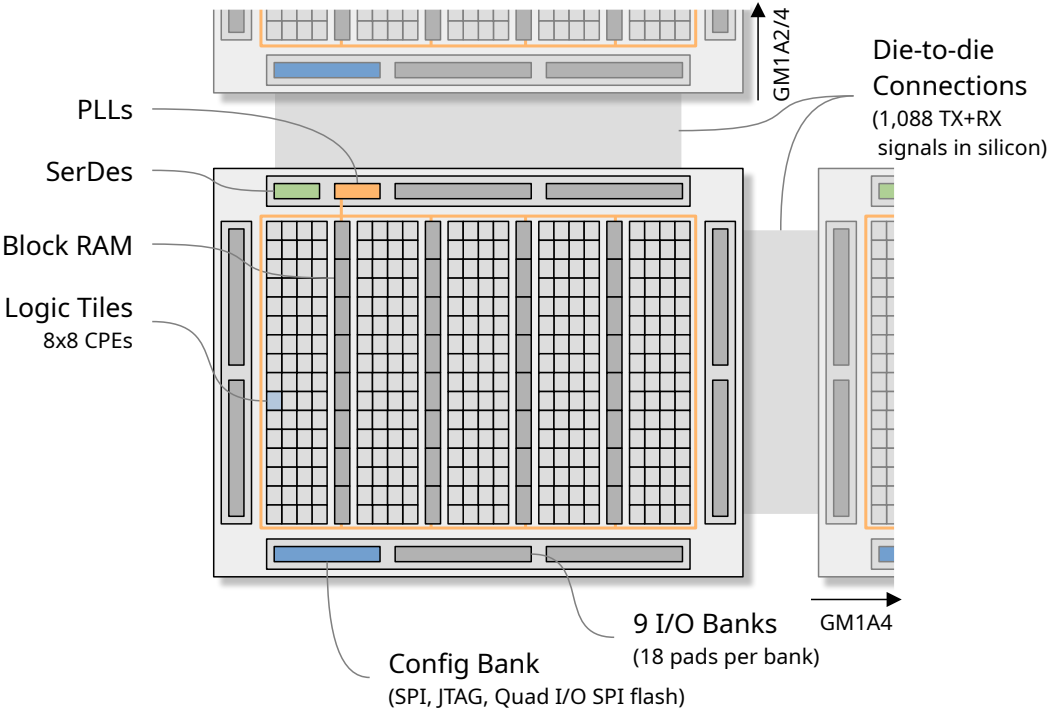
3. Radiation Qualification

   Test Setups & Results

# GateMate FPGA

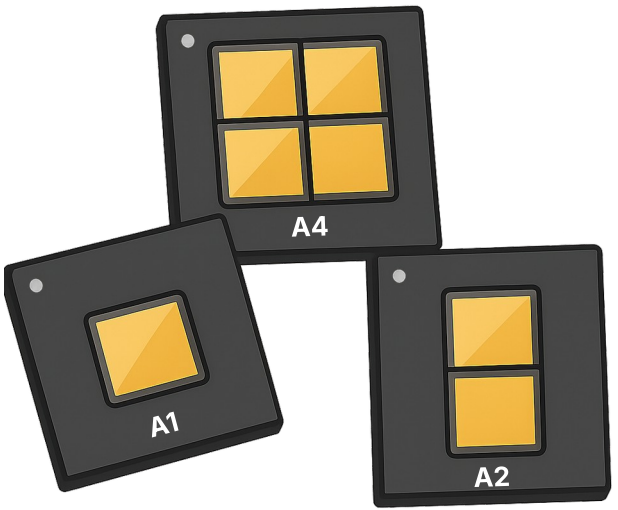
## Features at a glance

- **Globalfoundries™ 28nm SLP** process (Fab 1 Dresden, Germany)
- **20,480 programmable elements** per FPGA-die
  - 8 inputs or 4+4 inputs + 2 flip-flops
  - 2-bit full adder or 2x2-bit multiplier
- All 162 GPIO configurable as single-ended or LVDS differential pairs with DDR support (**MIPI D-PHY compatible**)
- 32x 40 Kbit RAM cells (Total 1,280 Kbit)
- 4 Clock Generators (PLLs)
- **5 Gbit/s SerDes** Controller
- Temperature range from **-40°C to +125°C**
- Core voltage from 0.9V to 1.1V
  I/O voltage from 1.2V to 2.5V (3.3V proven)
- **Open Source Toolchain** using yosys and nextpnr
- A1, A2, A4: Patented Multi-Die concept



# GateMate FPGA Series

## Feature Summary by Device



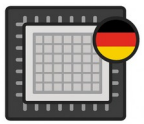

- ✔ Patented Technology
- ✔ Pin compatible

| Device | CPEs | FFs | Block RAM | | PLL | SerDes | GPIO | | Package |
|---|---|---|---|---|---|---|---|---|---|
| | | | 20K | 40K | | | Single-ended | Diff. Pairs (LVDS) | |
| ★ **A1** | 20,480 | 40,960 | 64 | 32 | 4 | 1 | 162 | 81 | 324 FBGA 15x15 mm |
| ★ **A2** | 40,960 | 81,920 | 128 | 64 | 8 | 2 | 162 | 81 | 324 FBGA 15x15 mm |
| ★ **A4** | 81,920 | 163,840 | 256 | 128 | 16 | 4 | 154 | 77 | 324 FBGA 15x15 mm |
| ... | | | | | | | | | |
| **A25** | 512,000 | 1,240,000 | 1600 | 800 | 100 | 25 | tba | tba | tba |

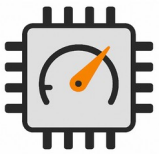
★ Mass Production ★ Engineering Samples in Q1/2026

# GateMate FPGA

## Features at a glance



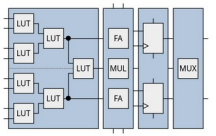
28nm
Made in Germany



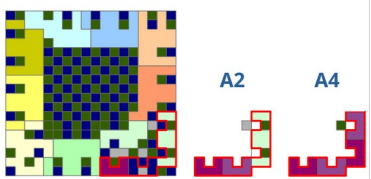
Instant-on
Configuration

Wide Temperature
Range (-40°C - 125°C)

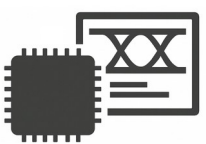
Bitstream
Scrubber




Innovative LUT
Architecture



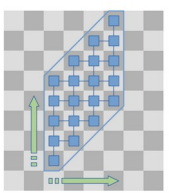

Easy Integration &
Pin Compatibility



High-speed
Serial Interfaces

Open Toolchain
and Ecosystem

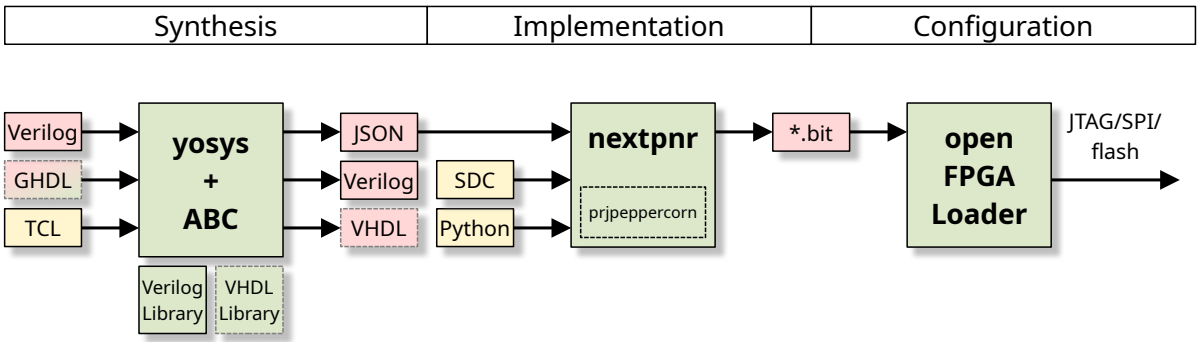
Tested in Rad-Hard
Environments

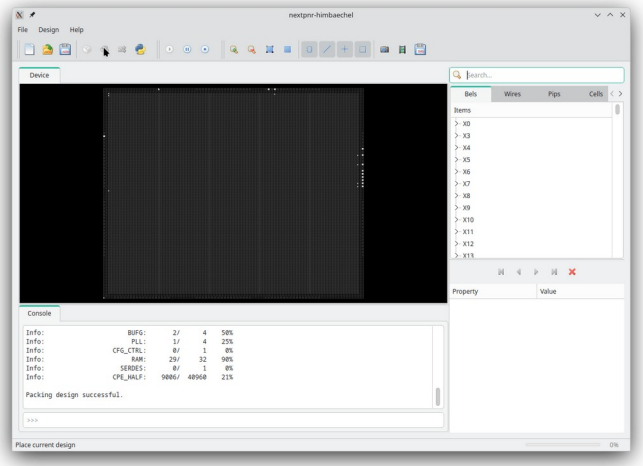


Flexible
Multipliers

# Toolchain

## Open-Source at Every Step



OSS CAD Suite (Daily Builds)
(~500MB, darwin-arm64, darwin-x64, linux-arm64, linux-x64, windows-x64)

# GateMate FPGA

## Central Programming Element

### Combinatorical

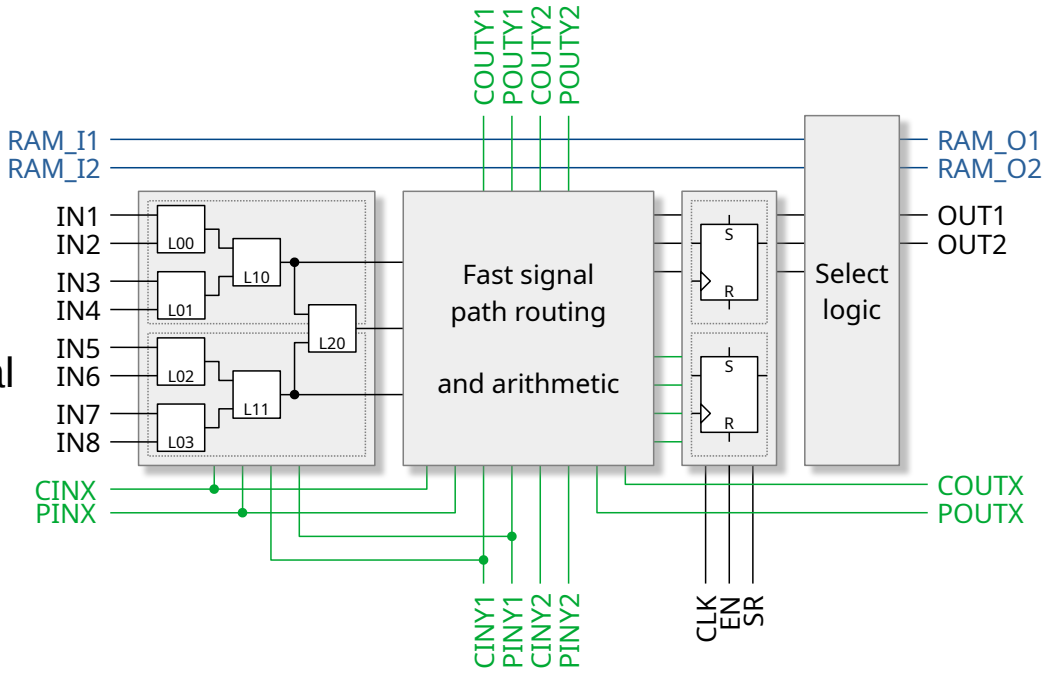
- 8-input function with LUT2-tree
- 2 independent 4-input functions
- 4+2 inputs for MUX-4 function

### Arithmetic

- 1-bit or 2-bit full adder, horizontal or vertical
- 2x2-bit multiplier, expandable to any size

### Sequential

- 2 Flip-flops or latches
  with initialization during configuration



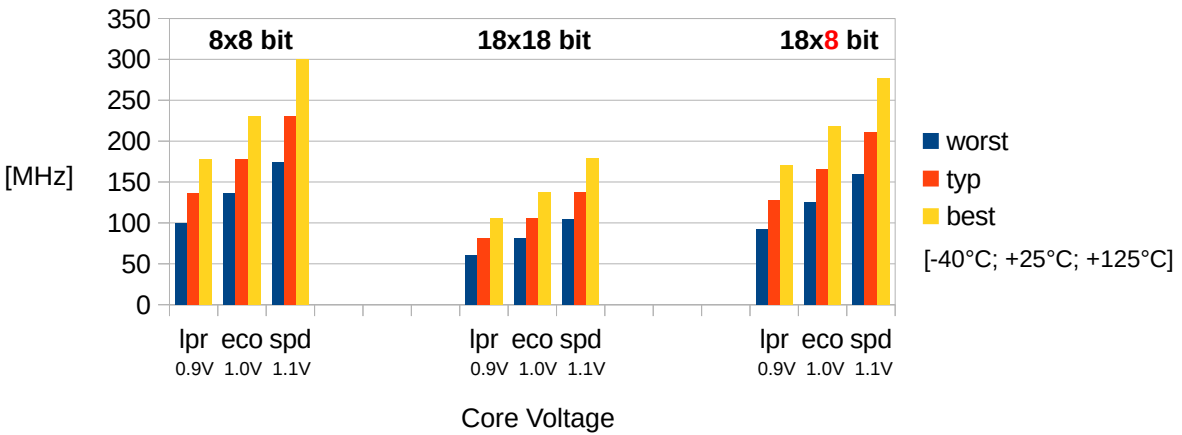
# CPE Multipliers

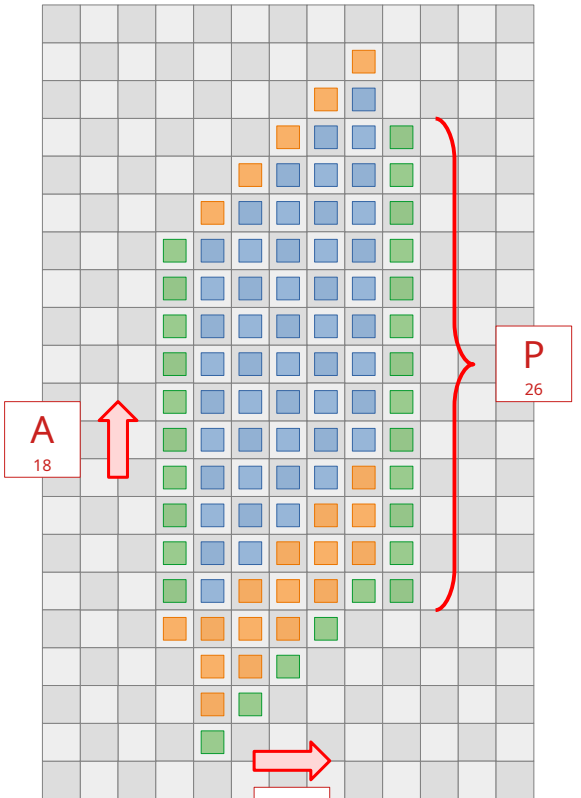
## Arbitrarily Scalable Multipliers

- No fixed placement in CPE array
- Optional input and output pipeline stages

## Performance

- B-vector determines critical path:



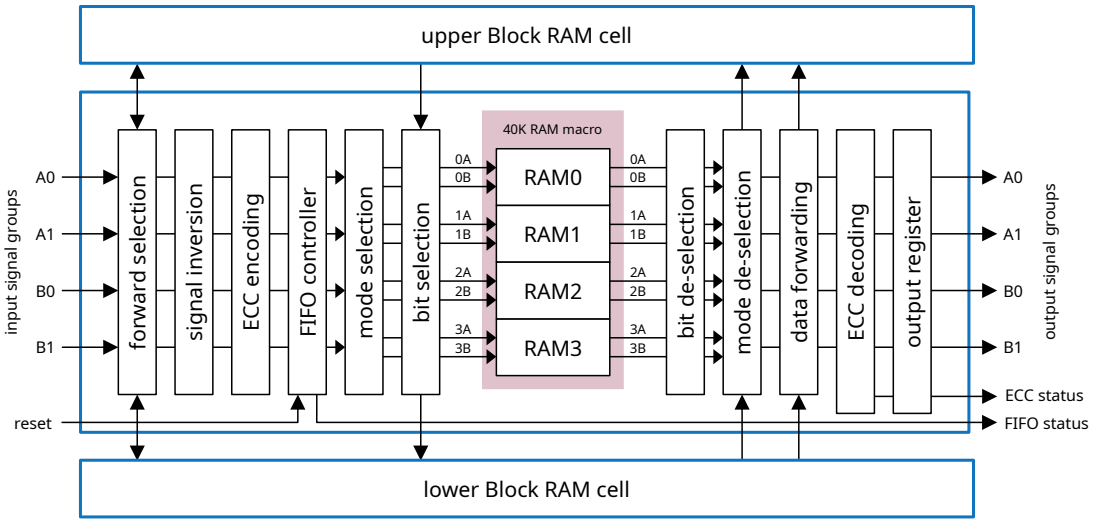

18x8 bit mult w/ in- and output pipeline

# GateMate FPGA

## Block RAM

### Configurations

- Single 40K cell or
- Two independent 20K cells
- True Dual Port (up to 40 inputs)
- Simple Dual Port (up to 80 inputs)
- FIFO (sync. or async.)
- Error Checking and Correcting

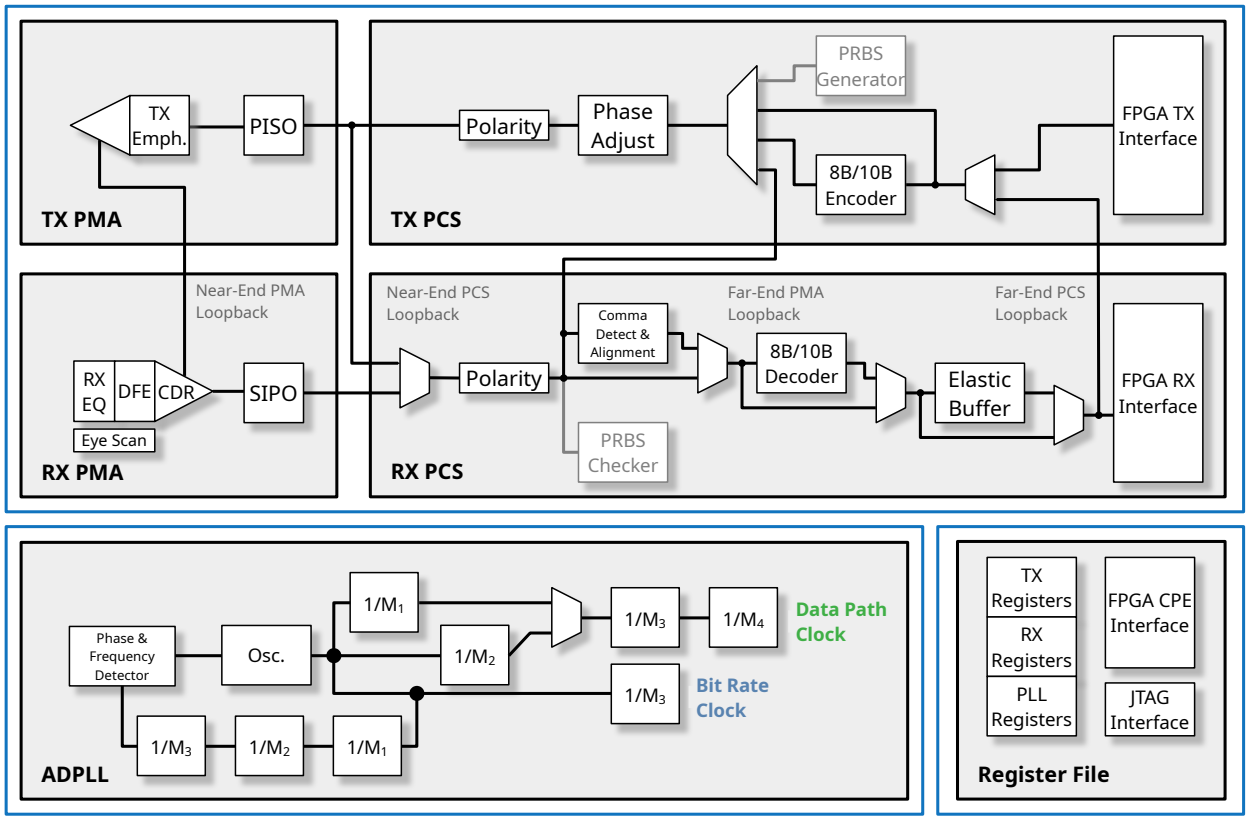


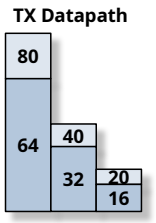

### Signal Forwarding

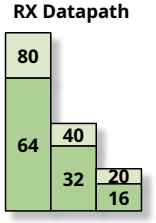
- All cells vertically connected
- Reduces routing overhead

# GateMate FPGA

## 5 Gbit/s Serializer/Deserializer (SerDes)




| | Bitrate Clock [MHz] | |
|---|---|---|
| # | 100M refclk | 125M refclk |
| 1 | 300 | 375 |
| 2 | 400 | 500 |
| 3 | 450 | 563 |
| 4 | 500 | 625 |
| 5 | 600 | 750 |
| 6 | 750 | 938 |
| 7 | 800 | 1,000 |
| 8 | 900 | 1,125 |
| 9 | 1,000 | 1,250 |
| 10 | 1,200 | 1,500 |
| 11 | 1,250 | 1,563 |
| 12 | 1,500 | 1,875 |
| 13 | 1,600 | 2,000 |
| 14 | 1,800 | 2,250 |
| 15 | 2,000 | 2,500 |
| 16 | 2,400 | 3,000 |
| 17 | 2,500 | 3,125 |
| 18 | 3,000 | 3,750 |
| 19 | 3,200 | 4,000 |
| 20 | 3,600 | 4,500 |
| 21 | 4,000 | 5,000 |
| 22 | 4,800 | 6,000 |
| 23 | 5,000 | 6,250 |
| 24 | 6,000 | 7,500 |
| 25 | 6,400 | 8,000 |
| 26 | 8,000 | 10,000 |
| 27 | 10,000 | 12,500 |

In Spec. | Not in Spec.

# GateMate Evaluation Board

## Interfaces

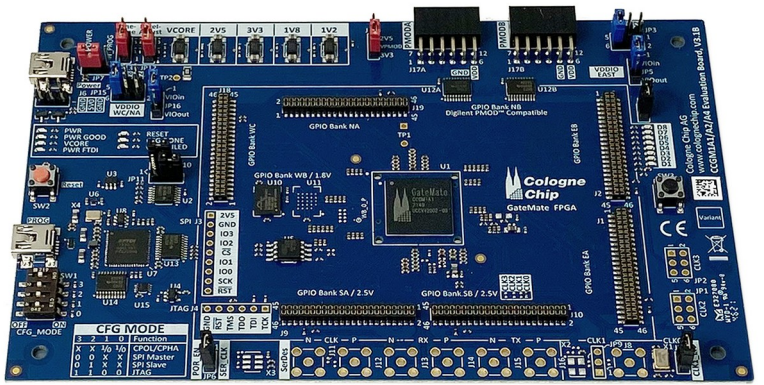
- Six I/O banks + access to SPI/JTAG signals
- Two standard 12-pin Pmod™ compatible connectors
- One high-speed SerDes RX, TX + CLK channel via SMA
- Configuration via flash or on-board USB to SPI/JTAG bridge

## Memory

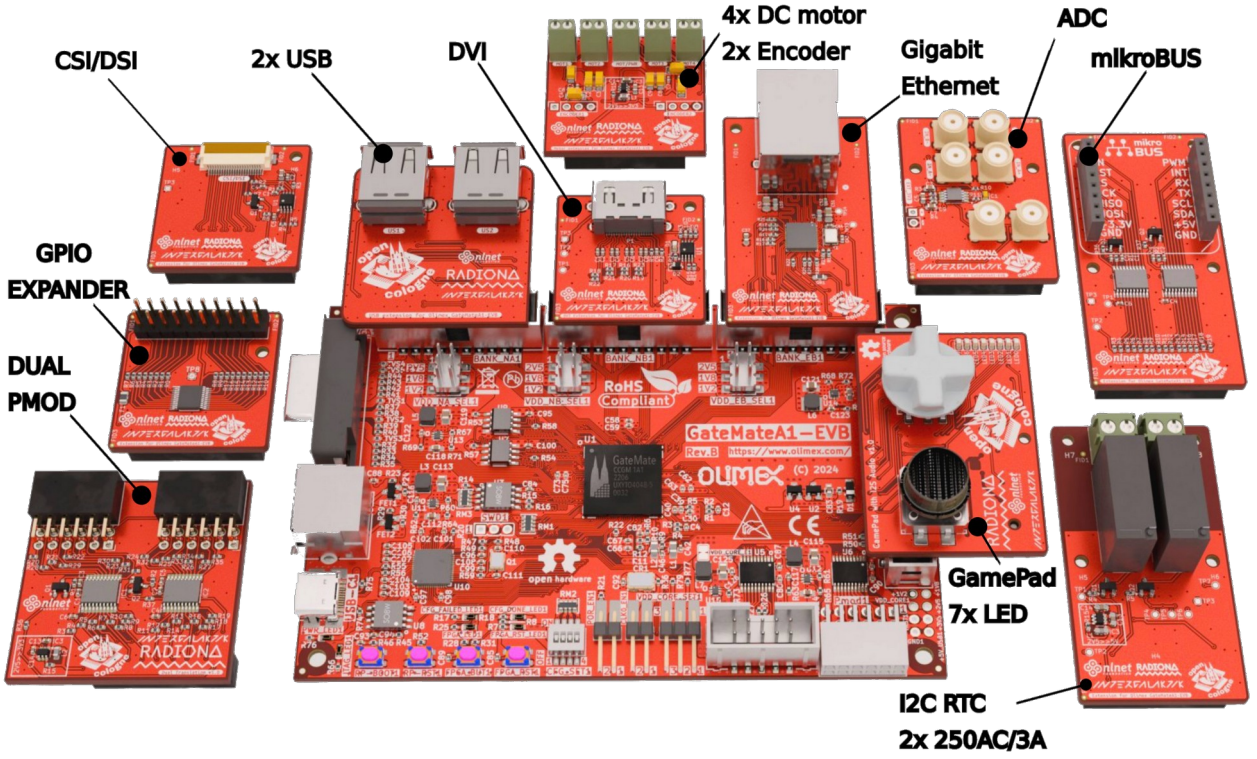
- 64 Mbit Quad-I/O SPI flash
- Up to two HyperBus modules (HyperRAM / HyperFlash)

## Power

- User-selectable core and I/O voltages



# Olimex GateMate A1-EVB



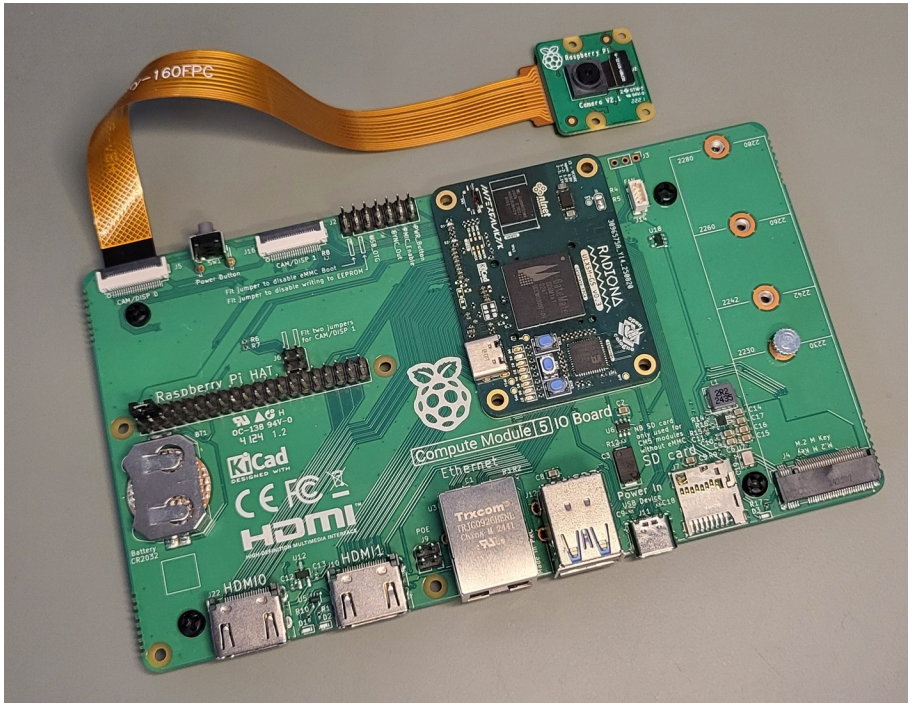

🌐 GateMate A1-EVB at Olimex
🌐 Extensions Repository

# ULX5M-GS

## Raspberry Pi compatible Compute Module

### Features

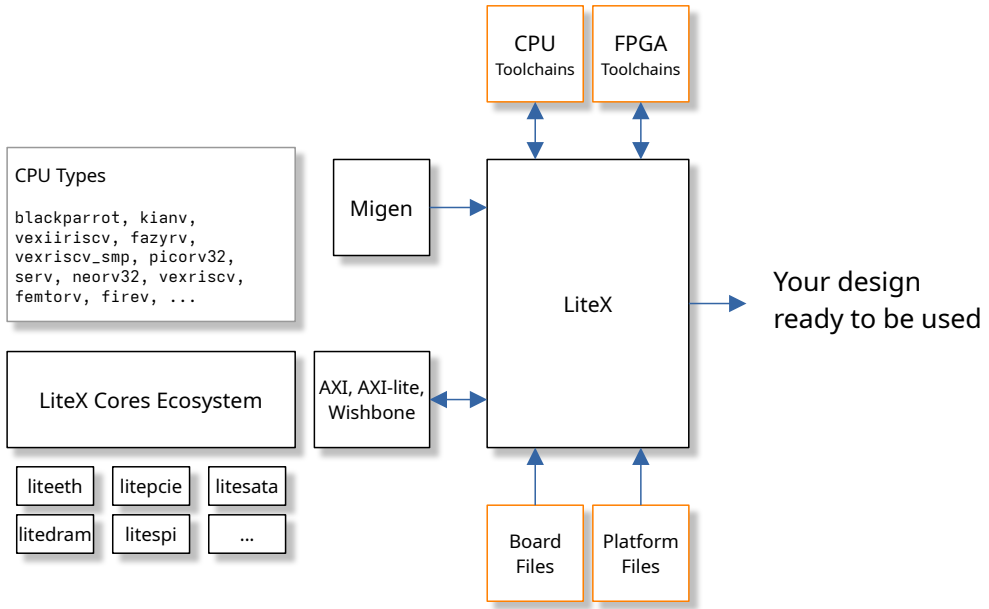
- PCIe interface
- USB interface (DFU bootloader)
- SDRAM memory
- Gigabit ethernet interface
- 2x MIPI interfaces
- 1x HDMI interface
- Raspberry Pi GPIO, SD card, ...




🌐 ULX5M-GS Repository at GitHub

# Massive IP Catalogue: LiteX

## „Build your hardware, easily!“




| Name | Build Status | Description |
|---|---|---|
| LiteX-Boards | ci passing | Boards support |
| LiteDRAM | ci passing | DRAM |
| LiteEth | ci passing | Ethernet |
| LitePCIe | ci passing | PCIe |
| LiteSATA | ci passing | SATA |
| LiteSDCard | ci passing | SD card |
| LiteICLink | ci passing | Inter-Chip communication |
| LiteJESD204B | ci passing | JESD204B |
| LiteSPI | ci passing | SPI/SPI-Flash |
| LiteScope | ci passing | Logic analyzer |

[1] https://github.com/enjoy-digital/litex

# GateMate Tools Action

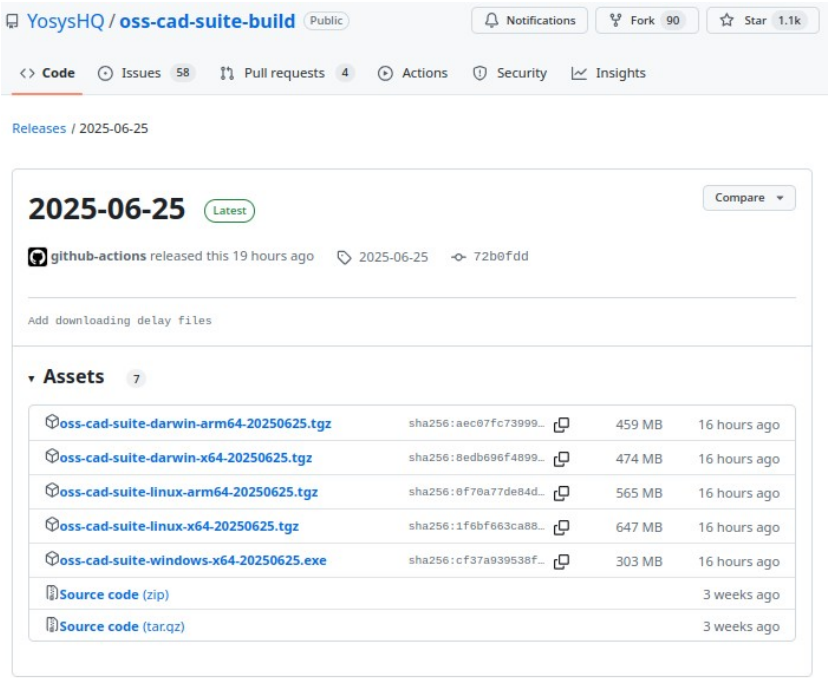
## Hands-on

# Installation: The Easy Way

## Pre-build with oss-cad-suite

- Daily builds available on GitHub
- Runs on ARM64, Linux, Windows and Mac
- Contains *all* tools, including simulators etc.

- Certainly the best option to start!




https://github.com/YosysHQ/oss-cad-suite-build/releases/

# Synthesis: yosys

https://github.com/YosysHQ/yosys

```
$ yosys
    -l <logfile>.log                # path to logfile
    -p '
        read_verilog <input>.v;     # your design files
        synth_gatemate              # synthesis pass for GateMate
            -top <topmodule>        # top module name
            -luttree                # use LUT-tree mode for nextpnr
            -nomult                 # disable multiplier support (will be added soon)
            -nomx8                  # disable MUX8 support
            -json <netlist>.json    # output netlist
      '
```

# Implementation: nextpnr

https://github.com/YosysHQ/nextpnr

```
$ nextpnr-himbaechel
    --json <netlist-file>.json      # input netlist from synthesis
    --device CCGM1A1                # can be CCGM1A1 or CCGM1A2
    -o ccf=<constraints-file>.ccf   # input constraints file
    -o out=<output-file>.txt        # output bitfile (human readable!)
    --router router2                # always use router2!
    --gui                           # optional: user interface mode
```

```
$ gmpack
    --crcmode <mode>                # optional: crc behaviour (check, ignore, unused)
    --background                    # optional: enables background reconfiguration
    <output-file>.txt               # human-readable bitfile from nextpnr
    <output-file>.bit               # bitfile for GateMate
```

# Programmer: openFPGALoader

https://github.com/trabucayre/openFPGALoader

```
$ openFPGALoader
    --index-chain 0         # device no. in the chain - optional
    --freq 10M              # programmer speed, max. 30M
    -b gatemate_evb_spi     # board: can be gatemate_evb_spi or gatemate_evb_jtag
    <your-cfg-file>.bit
```

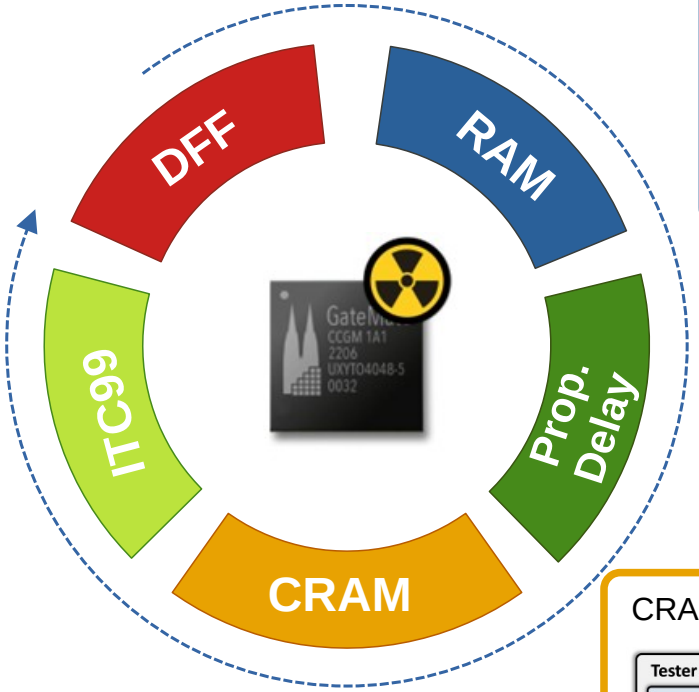
```
Jtag frequency : requested 6.00MHz    -> real 6.00MHz
Load SRAM via JTAG: [==================================================] 100.00%
Done
Wait for CFG_DONE DONE
```

# Radiation Qualification

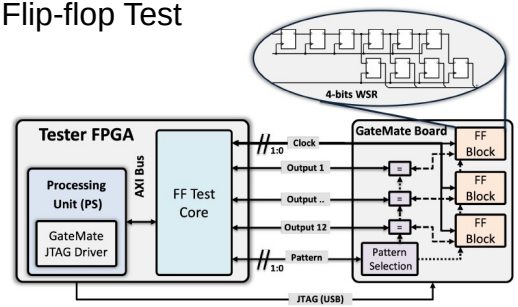
## How to qualify a FPGA for radiation-hard environments?

# SEE & TID Test Structures

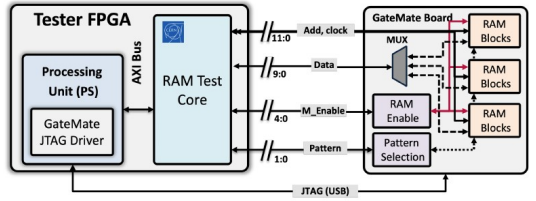
## Single event effects / Total ionization dosis



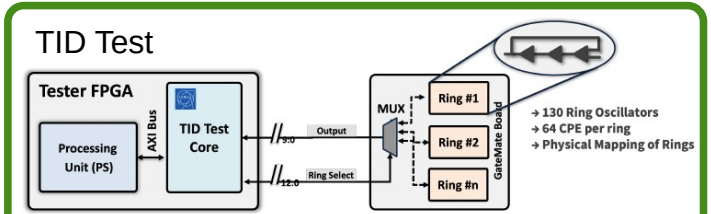

### Flip-flop Test



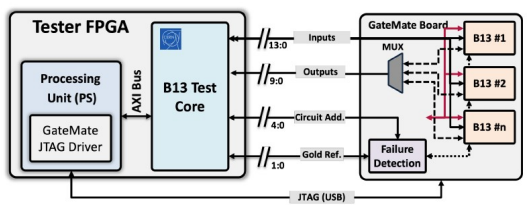

### RAM Test



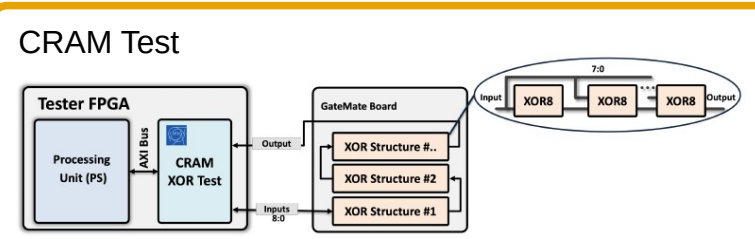

### TID Test




### ITC99 Test



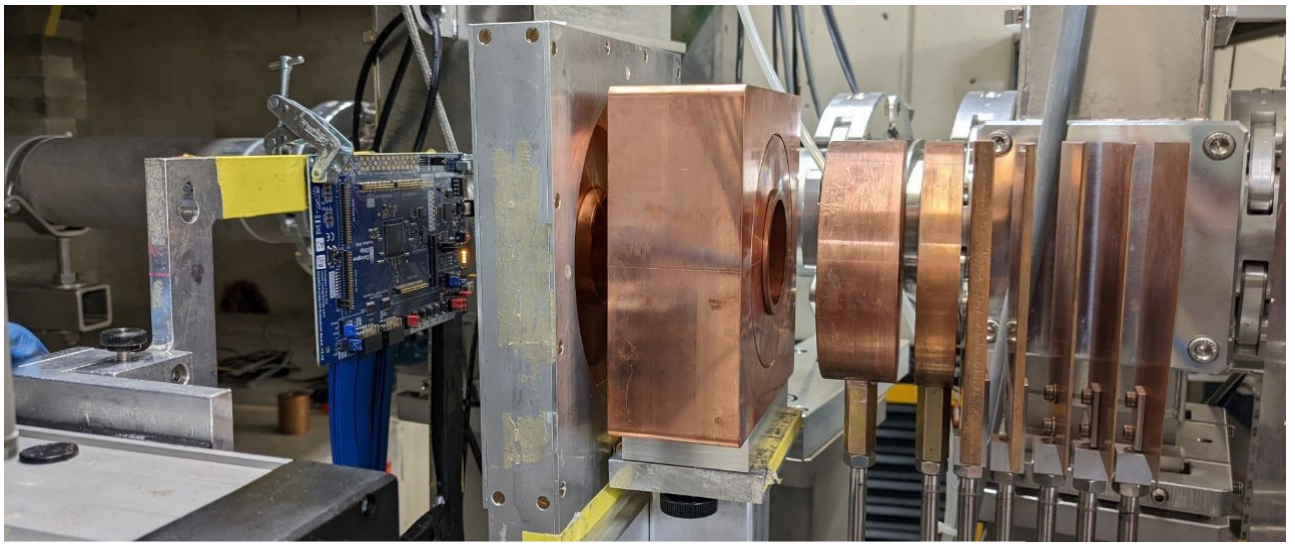

### CRAM Test




https://www.nsrec.com/technical-program-2024-thursday/

# SEE Test Setup

## at Paul Scherrer Insitut (PSI)

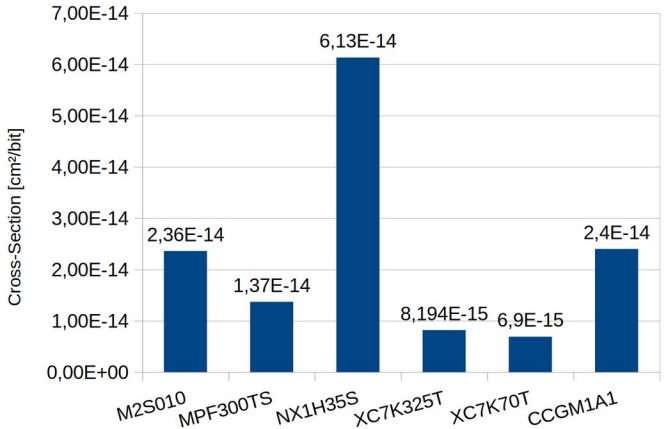


Proton Beam Setup @ PSI

# SEE Test Results

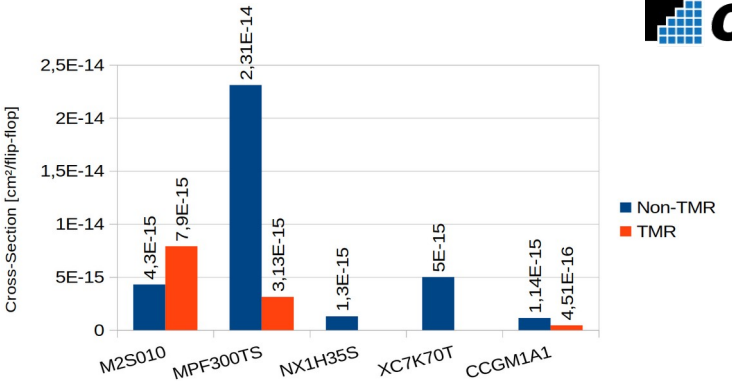
## at Paul Scherrer Insitut (PSI)

Results <u>without</u> bitstream scrubber

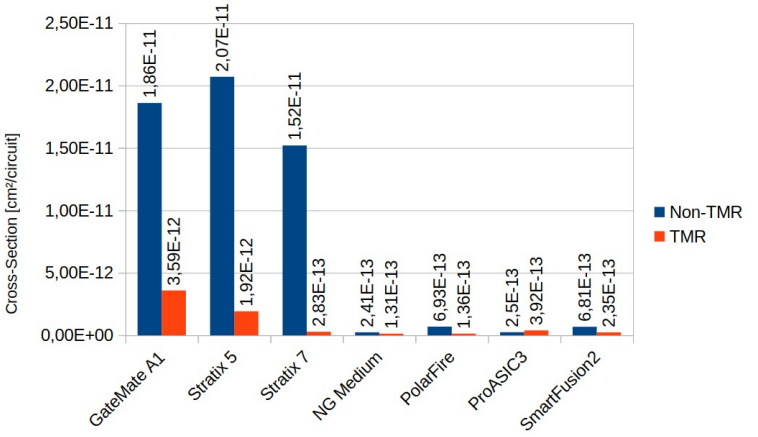



Comparison of BRAM test results *

(new results from heavy-ion testing show much better cross-section)




Comparison of flip-flop test results



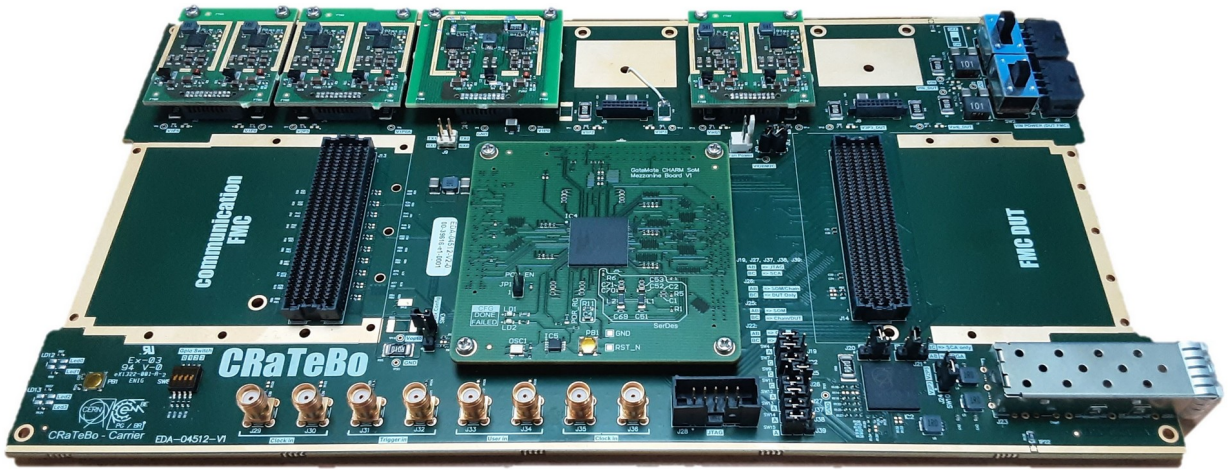

Comparison of ITC99 test results

🌐 Radiation Qualification of the Cologne Chip GateMate A1 FPGA

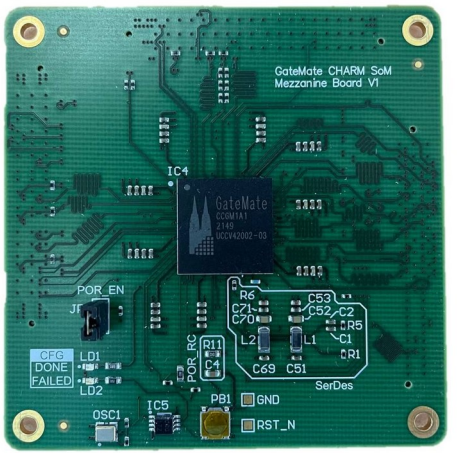
# CraTeBo System on Module

## For TID Tests at CHARM

Entire Evaluation Board
exposed during TID test

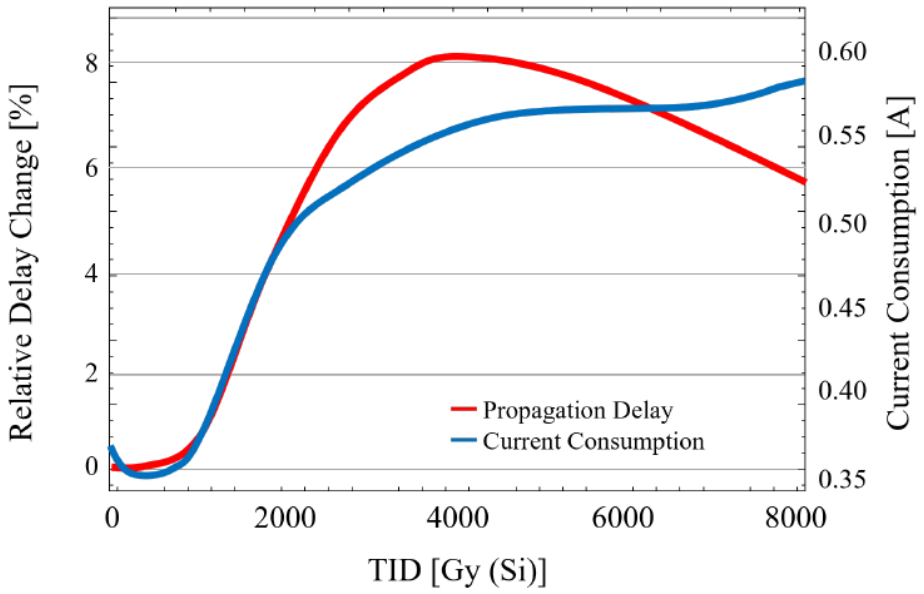



CERN’s Radiation-hardened CraTeBo Platform



# TID Test Results

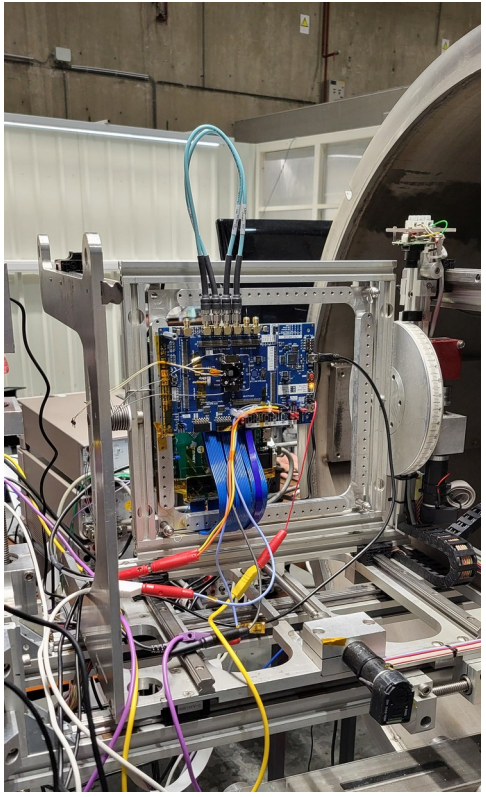
## at CHARM Irradiation Infrastructure (CERN)



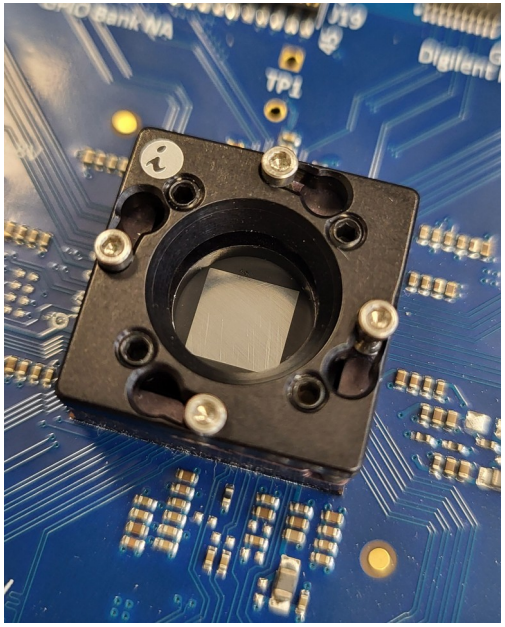

- No degradation up to **1kGy**
- Good correlation b/w propagation delay increase and current consumption increase up to **4kGy**
- Good robustness to TID

# Heavy Ion Test (Latch-up)

## at UCL Belgium



Heavy Ion Beam Setup @ UCL



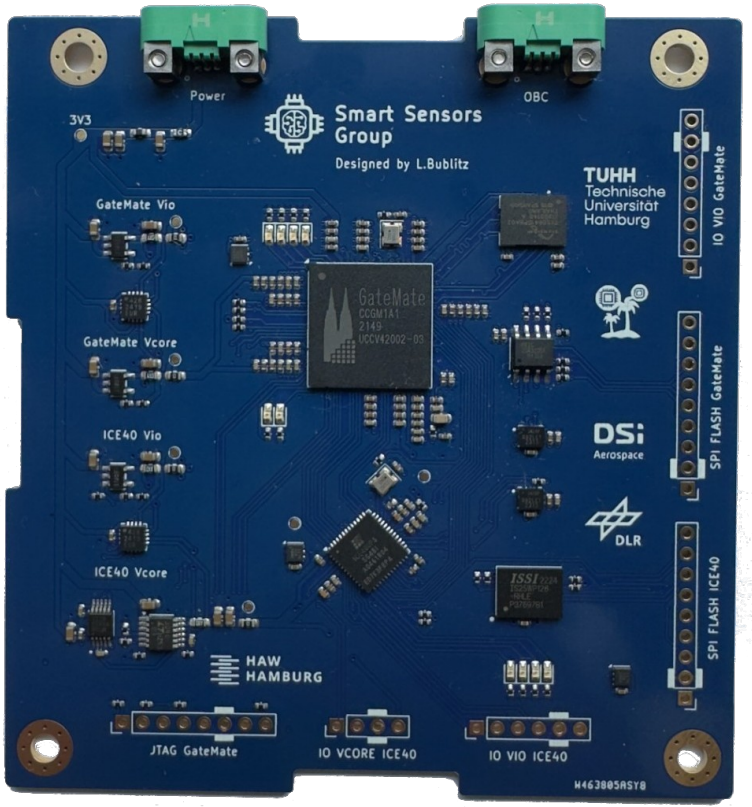
GateMate FPGA in socket after sanding

**Results published soon**

# GateMate in Space

## Space Technology made at HAW Hamburg

- **PLUTO** small satellite by HAW + TUHH Hamburg
- Launch in autumn 2025, in orbit for at least a year
- Experiments: Undervolting
- Reconfigurable from earth




News Article HAW Hamburg

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