Contribution ID: **27** Type: **not specified**

General purpose, high-performance and energy-efficient x86 based computing with Many-Core Technologies (TFLOPS on a chip)

Thursday, 3 May 2012 11:00 (45 minutes)

As we see Moore's Law alive and well, more and more parallelism is introduced to all computing platforms on all levels of integration and programming to achieve higher performance and energy efficiency. We will discuss the new Intel(r) Many Integrated Core (MIC) architecture for highly-parallel workloads with general purpose, energy efficient TFLOPS performance on a single chip. We will also discuss the journey to ExaScale including technology trends for high-performance and look at some of the R&D areas for HPC at Intel.

Presenter: CORNELIUS, Herbert